320MHz Digital Phase Lock Loop

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Abstract

DPLLs (Digital Phase Locked Loop) are commonly used in communications systems. As part of an investigation into RFID technology, a DPLL suitable for low-cost, low-power applications is designed and layed out out in a 0.5μm CMOS process. It consists of a phase frequency detector, charge-pump filter, current-starved VCO, and a frequency divider. It is designed to operate using a reference signal between 20MHz and 46MHz producing an output signal between 160MHz and 368MHz. The DPLL is part of a three chip RFID transceiver systems and generates additional signals (10MHz, 0.625MHz and lock enable) for use in the system.

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Acknowledgments

The author would like to thank Professor David Kotecki and fellow students Alma Delić-Ibukić, Zhineng Zhu and Roman Shugaye for their assistance and encouragement during this project.

Chapter 1

Introduction

1.1 Overview

Radio frequency identification (RFID) technology is rapidly growing field. With companies like Walmart requiring their supplier to adopt RFID technology the demand for these devices has increase dramatically. Other organization, such as the US Government, are interested in more advanced RFID devices able to store more information or interface with sensors.

The purpose of this project was to develop knowledge and technology suitable to RFID tags. An RFID tag, in its basic form, is device capable of transmitting a identification sequence to an RFID reader. An RFID tag is suitable for replacing tradition bar codes. The main advantage of RFID tags is the ability to be read at distance without a direct line of sight.

1.2 Digital Phase Locked Loop (DPLL)

A DPLL is a device often used in communications systems for clock recovery and/or synchronization. For an RFID application a DPLL is used to create an on-chip carrier frequency from a transmitted reference. This eliminates the need for a precision on chip oscillator or the use of a crystal oscillator. In addition clock signals can be derived from the carrier frequency. There are four basic parts of a PDLL.

- Phase Detector
- Filter

- Voltage Controlled Oscillator
- Frequency Divider

A block diagram of the basic components of a DPLL is shown in **Figure 1.1 on page 2**.

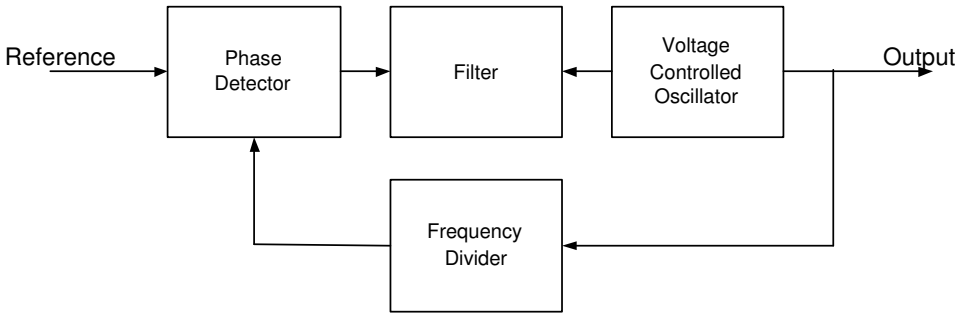

Figure 1.1: DPLL Block Diagram

1.2.1 Phase Detector

A phase detector has an output proportional to the phase difference between an signal generatored on-chip and a external reference signal. This output is used to correct the phase difference.

1.2.2 Filter

A filter is typically needed between the phase detector and voltage controlled oscillator to achieve the desired lock characteristics.

1.2.3 Voltage Controlled Oscillator

A voltage controlled oscillator (VCO) has a oscillatory output with a frequency proportional to an input voltage. The VCO allows the on-chip frequency to vary. In DPLL applications this feature allows the VCO to be used a feedback look to sync with (or lock on) to the reference signal (or a multiple thereof).

1.2.4 Frequency Divider

A frequency divider enables the frequency of the VCO to be some multiple of the reference signal. This allows a relatively low frequency reference signal to create a much higher frequency on-chip frequency.

1.3 Specifications

	Specification	Value
Inputs	reference frequency	40MHz
	positive rail	5V
	negative rail	0V
Outputs	logic enable	0-5V Step, 5us delay
	8x reference frequency	320MHz
	1/4 reference frequency	10MHz
	1/64 reference frequency	0.625MHz

Table 1.1: Specifications

Pin	Pin Name
1	vdd
6	Enable
6	Enable
6	Enable
15	0.624MHz
16	10MHz
20	gnd
22	gnd
30	320MHz
32	T_ VCO_ OUT
36	NAND
37	B
38	A
40	vdd

Table 1.2: Pin Out

1.4 Limitations

The current design is limited is several areas. Due to the process used as well as design choices, the maximum operating frequency of the PLL in simulation is 368 MHz. Experimental performance is expected to be somewhat less than this. The

Chapter 2

Circuit Design

2.1 Basic Logic Blocks

2.1.1 Inverter

Figure A.1 on page 29 shows a standard CMOS inverter. The width of the PMOS device is double that of the NMOS device to obtain approximately matched current capabilities. The NMOS device is a minimum sized device for this process yielding the smallest matched inverter.

2.1.2 2 Input NAND

Figure A.4 on page 32 shows a standard 2 input CMOS NAND gate. The gate is sized to match the performance of a minimum sized inverter.

2.1.3 3 Input NAND

Figure A.3 on page 31 shows a standard 3 input CMOS NAND gate. The gate is sized to match the performance of a minimum sized inverter.

2.1.4 4 Input NAND

Figure A.4 on page 32 shows a standard 4 input CMOS NAND gate. The gate is sized to match the performance of a minimum sized inverter.

2.1.5 D-Latch

Figure A.8 on page 36 shows a 9-transistor TSPC (true single phase clock) d-latch suitable for frequency division applications. The basic layout

of the d-latch is taken from *CMOS Circuit Design, Layout, and Simulation* [RBB98].

2.2 Comparator

Figure A.14 on page 42 shows a simple comparator that is needed with the enable circuit to provide hystereses. This is necessary to eliminate the sensitivity of the enable output to rail voltage variations.

2.3 Phase Frequency Detector (PFD)

A standard PFD design shown in **Figure A.12 on page 40** is used for the phase detector of the DPLL. As its name suggests, a phase frequency detector response both to phase differences and frequency differences. A PFD has several desirable characteristics. It will not lock onto harmonics of the reference signals and it has no ripple once the loop is locked. The major downside is that the PFD is an edge triggered circuit, making is susceptible to noise. The circuit works by creating a pulse on the up_bar output if the positive edge of the reference signals leads the on-chip signals and a pulse on the down_bar output if the order is reversed. These outputs then need to be combined and averaged by a filter to controlled the VCO.

2.4 Charge-Pump Loop Filter

The use of a PFD type phase detector necessitates a filter than can produce a relativity slowly varying output from the two outputs of the PFD. The two common types of filter for this applications are the tri-state filter and the charge-pump filter. As shown in **Figure A.13 on page 41**, a charge-pump filter is chosen for the DPLL. The benefits of the tri-state filter include zero static power dissipation and simplicity. By adding a small biasing current to the tri-state filter and altering the layout of the passive components, a charge-pump filter is constructed. A charge-pump filter produces less phase error in the overall system by allowing narrower pulses from the PFD to affect the VCO. The basic layout of the charge-pump filter is taken from *CMOS Circuit Design, Layout, and Simulation* [RBB98]. The charge-pumps works by charging the two capacitors up when it receives an up pulse from the PFD and discharges the capacitors when it receives a down pulse from the PFD. The RC network is designed to integrate these pulses such that the VCO sees a relatively slowly varying signal.

2.5 Voltage Controlled Oscillator (VCO)

A 5-stage current-starved voltage controlled oscillator is used to create the on-chip frequency. The design is take from *CMOS Circuit Design, Layout, and Simulation* [RBB98]. It consists of two major parts, a voltage controlled current source and a ring oscillator constructed of current starved inverters. The current source serves to limit the current through the inverters and change the frequency at which the ring oscillates. **Figure A.11 on page 39** shows a schematic of the VCO.

2.6 Frequency Divider A

A frequency divider is needed to divide the output of the VCO by a factor of 8. This is needed to create the desired 320 MHz signal from an easily generated test signal (40MHz). **Figure A.9 on page 37** shows a schematic of this divider.

2.7 Frequency Divider B

A second frequency divider is required to provide additional frequencies (nominally 10MHz and 625KHz)for use on the sequence generator and multiplexer components of the RFID system. **Figure A.10 on page 38** shows a schematic of this divider.

2.8 Enable

The purpose of this circuit is to trigger external circuity once the DPLL has 'locked'. The circuit consists of an RC circuit that begins to charge once a reference signal is input. A comparator is tripped once the voltage on the capacitor reaches roughly 3 volts. The circuit creates an approximately 5 microsecond delay before driving the enable pin high, signaling the sequence generator chip in the RFID system to turn on and begin transmitting. A schematic of the enable circuit is show in **Figure A.15 on page 43**.

2.9 6-Stage Digital Output Buffer

A buffer is needed to drive off-chip loads at the VCO frequency. The buffer is designed to drive a load of up to 40pF at up to 500 MHz. A 6-stage buffer

with a minimum sized first stage with each stage thereafter increasing in size by a factor of 5 is used. The schematic of the bugger is shown in **Figure A.7 on page 35**.

2.10 4-Stage Digital Output Buffer

A buffer is needed for he 10MHz, 0.625MHz and Enable outputs. The buffer is designed to drive a load of up to 40pF at up to 10 MHz. A 4 stage buffer with a minimum sized first stage with each stage thereafter increasing in size by a factor of 5 is used. This buffer was integrated into the padset (final layout beneath the power rings) to minimize area usage. The schematic of the buffer is shown in **Figure A.6 on page 34**.

2.11 2-Stage Digital Output Buffer

A 2 stage buffer is used in several locations within the circuit to reduce loading and increase fanout. The schematic for this buffer is shown in **Figure A.5 on page 33**.

2.12 Block Diagram

Figure 2.1 shows a block diagram of the complete DPLL circuit.

2.13 Test Circuits

Several test circuits are included on chip to evaluate component performance as well as assist in any troubleshooting.

2.13.1 2 Input NAND

This test circuit consists of a minimum sized NAND gate (**Figure A.5 on page 33**) with a 4 stage output buffer (**Figure A.6 on page 34**). It is intended as a simple test for major processing and/or packaging issues.

2.13.2 VCO

The test VCO circuit includes a VCO (**Figure A.11 on page 39**) and a 6 stage output buffer (**Figure A.7 on page 35**). It is intended to test the performance of the VCO.

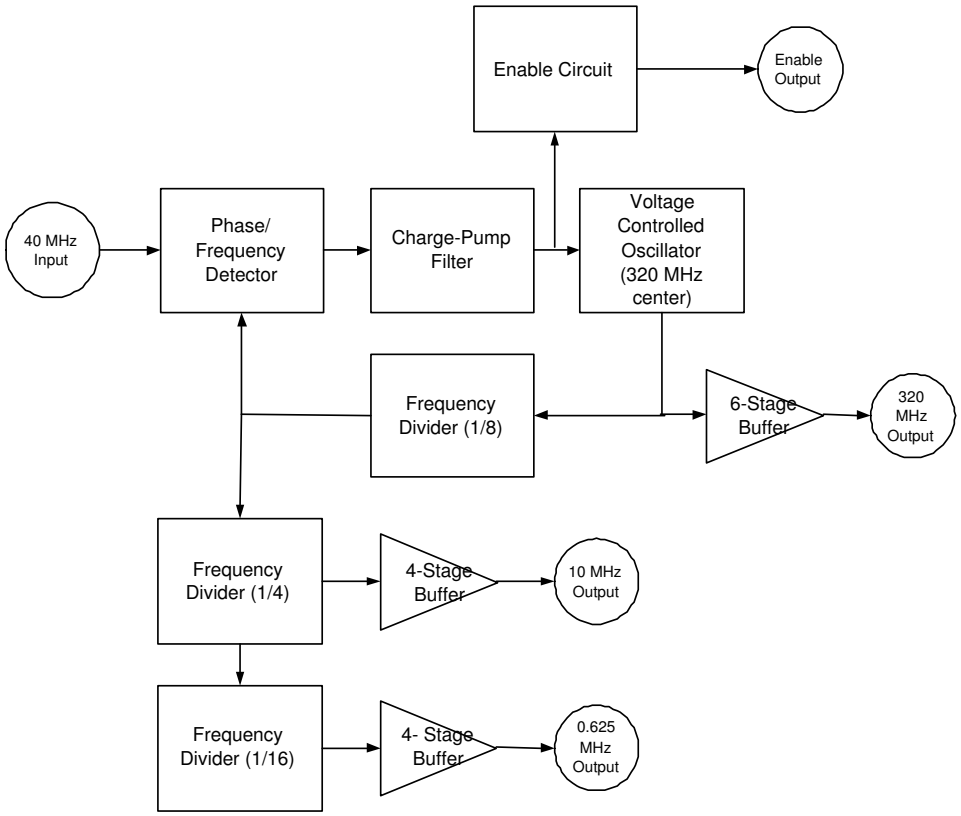

Figure 2.1: DPLL Block Diagram

2.13.3 Frequency Divider A

A test frequency divider (**Figure A.9 on page 37**) with a 4-stage output buffer (**Figure A.6 on page 34**) is included on chip to evaluate the performance of the frequency divider design.

2.14 Design Trade Offs

Power usage is critical for RFID tags. The vast majority of RFID will be passive, receiving all the power necessary to operate from an RF signal. This DPLL is designed as an active component, requiring a power source such as a battery to operate. Battery operation requires low power consumption. This is achieved using CMOS design techniques, minimizing the device size, minimizing the number of devices, and avoiding circuits designs with standby power when able. In addition this circuit has a standby mode. When no reference signal is being applied, the VCO input is driven low. This causes the VCO to stop oscillating. Without the VCO oscillating, the circuit current draw is dramatically reduced, leaving only leakage currents, the comparator biasing currents, and the charge-pump biasing currents. Allowing the VCO to stop oscillating does increase the lock time which is acceptable in this application considering the decrease in power usage.

Chapter 3

Circuit Performance

3.1 VCO

Figure 3.1 on page 11 shows the output waveform of the VCO with a 2.5V dc input. This simulation is performed using the analog extracted file generated from the VCO layout (**Figure B.12 on page 57**) and includes parasitic capacitors. The frequency of the output is 270MHz.

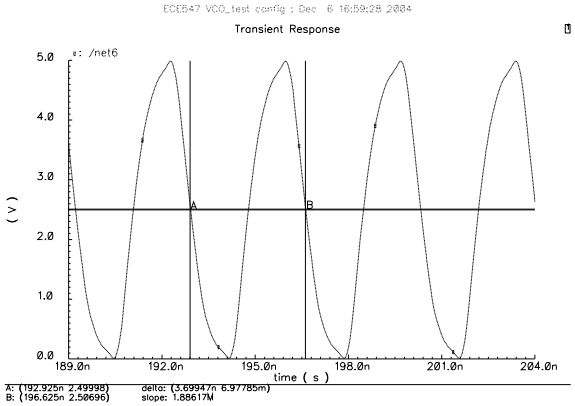

Figure 3.1: VCO Simulation, 2.5V input

Figure 3.2 on page 12 shows the output frequency of the VCO versus

the input voltage. This simulation is performed using the analog extracted file generated from the VCO layout (**Figure B.12 on page 57**) and includes parasitic capacitors.

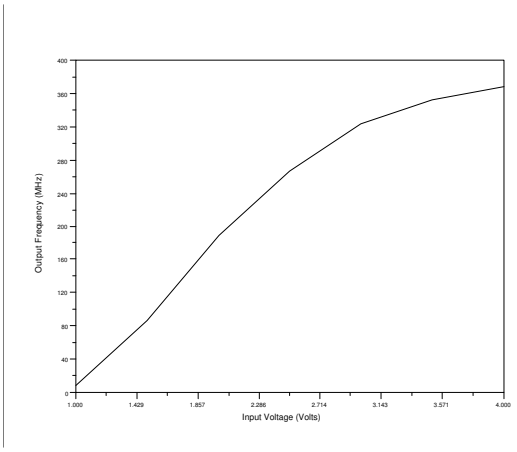

Figure 3.2: VCO Output Frequency vs. Input Voltage

3.2 Enable

Figure 3.3 on page 13 shows the output the output of the enable circuit with a simulated input. This simulation is performed using the analog extracted file generated from the Enable layout (**Figure B.16 on page 61**) and includes parasitic capacitors. The simulated delay is 5.14 microseconds.

3.3 PFD

Figure 3.4 on page 13 shows the output of the PFD with a 40MHz reference signal and a simulated 50MHz signal from the frequency divider A. This simulation is performed using the analog extracted file generated from the PFD layout (**Figure B.13 on page 58**) and includes parasitic capacitors. The up_bar waveform is essentially a constant high voltage and the down_bar output has significant pulses (both outputs are normally high). This will drive voltage input to the VCO down, causing it to slow and eventually lock onto the reference signal.

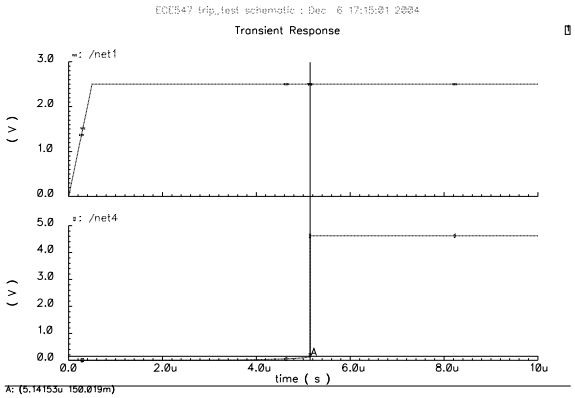

Figure 3.3: Enable Circuit Simulation, input top & output bottom

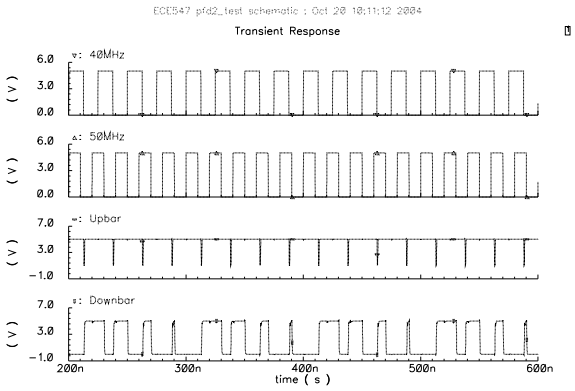

Figure 3.4: PFD Simulation, 40MHz and 33.3MHz inputs

3.4 Divider

Figure 3.5 on page 14 shows the output of the frequency divider with a 320MHz square wave input. This simulation is performed using the analog extracted file generated from the DiverA layout (**Figure B.10 on page 55**) and includes parasitic capacitors. The output waveform has a frequency of 40MHz, 1/8 of the input frequency.

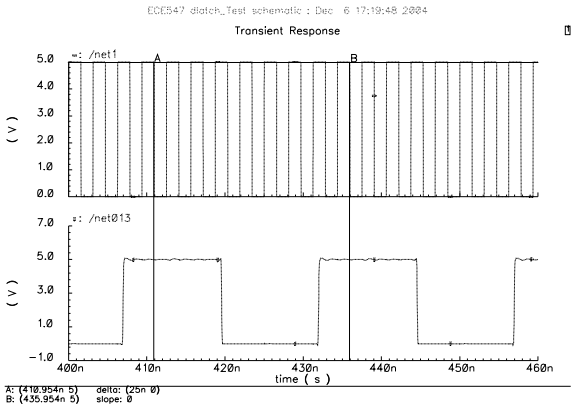

Figure 3.5: 1/8 Frequency Divider Simulation, 320MHz input

Chapter 4

Physical Design

Physical layouts for each piece of the DPLL can be found in **Appendix B on page 45**.

4.1 Component Layout Consideration

Component layouts are kept as compact and rectangular as possible to minimize die area. Individual components (excluding the 4 stage buffer, 6 stage buffer, and enable circuit) are surrounded by a grounded cage. This cage consists of a metal1 ring connected to the substrate, a metal2 ring connected to metal1 and a metal3 plane covering the entire component. The metal3 plane connects to the metal2 ring and acts as the ground contact for the component. A gap is opened up in the metal2 to allow signal and vdd connections to the components. The purpose of this cage is to minimize coupling between components.

The 4 stage digital buffer is located within a pad macro. This location, beneath the vdd and gnd rings, allows the buffer to be added to an output line without taking up any addition area with the guard rings.

4.2 Floor planning

As the circuitry for the DPLL does not require even half the available die area, there was considerable flexibility in the final layout. The main circuit is kept as far away from the 6 stage buffer as possible. A large row of decoupling capacitors (capacitors tied between gnd and vdd) between the

buffers and the rest of the circuit acts as a barrier strip. Additional decoupling capacitors are present in the corners of the chip. The total on-chip decoupling capacitance is roughly 265pF. This large decoupling capacitance is needed due to the 320MHz digital buffers, which draw large amounts of current during switching. The 6 stage buffer can draw enough current to pull down the voltage on the vdd rail and potentially cause problems with the other circuits on the chip. The large decoupling capacitance reduces the amount that the rails 'bounce' to a manageable level. The layout attempts to keep signal wires short wherever possible and to minimize the capacitive coupling between signals lines.

Chapter 5

Verification

5.1 DRC

The DRC (design rule check) tool was used to ensure that each circuit component, as well as the whole chip, meet the design rules for the 0.5μm AMI process used to fabricate the DPLL. Fill rule and antenna rule compliance was estimated visually.

5.2 LVS

The LVS (layout versus schematic) tool was also employed to ensure that the various component layouts matched their respective schematics. The entire chip was likewise tested. This insures that the components and the wiring in both the schematic and layout match. LVS results are shown below.

CDS: LVS version 4.4.6 06/24/2003 17:52 (cds11607)
Like matching is enabled.
Net swapping is enabled.
Fixed device checking is enabled.
Using terminal names as correspondence points.

count (layout)

234	nets
14	terminals
45	res
294	cap
765	pmos

782	nmos

count (schematic)

199	nets
14	terminals
10	res
4	cap
161	pmos
178	nmos

Terminal correspondence points

1	0.625MHz
2	10MHz
3	320MHz
4	A
5	B
6	ENABLE
7	NAND
8	REF
9	T_DIVID_IN
10	T_DIVID_OUT
11	T_VCO_IN
12	T_VCO_OUT
13	gnd!
14	vdd!

The net-lists match.

	layout	schematic
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	1886	353
total	1886	353
nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	234	199
total	234	199

5.3 Full Chip Simulation

Several full chip simulations were run to ensure that the circuit was functional, met specifications, and did not show aberrant behavior. These simulations included the analog extracted chip, external load capacitors and RLC models for the power pins.

Figure 5.1 on page 19 shows the simulated output of the 320MHz pin with a 40pF load capacitor. The reference signal for this simulation is a 40MHz square ware.

Figure 5.2 on page 20 shows the simulated output of the 10MHz pin with a 20pF load capacitor. The reference signal for this simulation is a 40MHz square ware.

Figure 5.3 on page 20 shows the simulated output of the 0.625MHz pin with a 20pF load capacitor and the Enable pin with a 3pF load capacitor. The reference signal for this simulation is a 40MHz square ware.

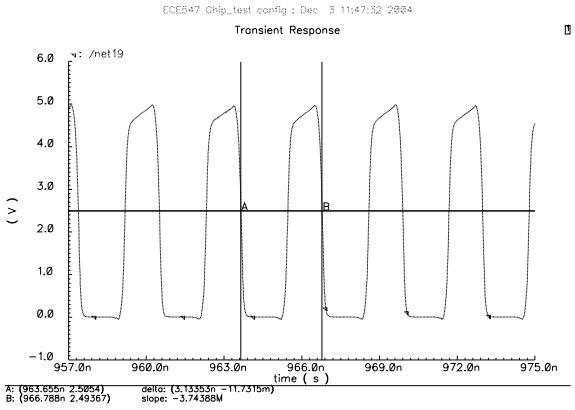

Figure 5.1: 320MHz Output, 40pF load

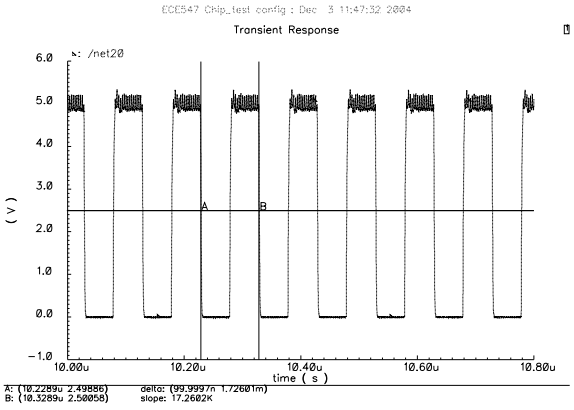

Figure 5.2: 10MHz output, 20pF load

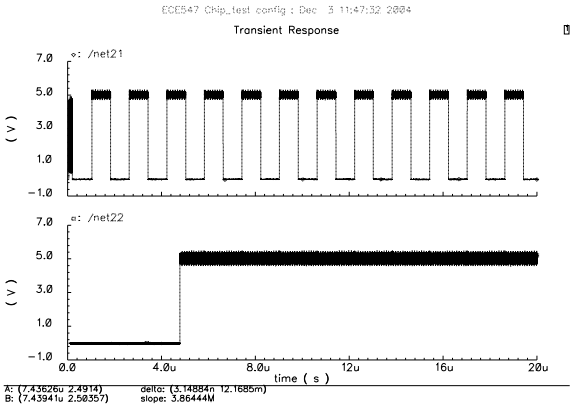

Figure 5.3: 0.625MHz output (top), Enable output (bottom)

5.4 Discussion

Figures **5.1** through **5.3** indicate that the DPLL performs well at 320MHz. Additional testing shows that the DPLL functions at up to 368MHz and as low as 160MHz. Lower frequencies should be possible but have not been simulated. The upper frequency is set by the highest frequency at which the VCO will oscillate. At 320MHz the system dissipates a total of 45mW. With no reference input the system dissipates less than 5mW.

Chapter 6

Experimental Results

6.1 Testing

6.1.1 Functional Logic Test

A NAND gate has been including on chip for testing basic chip functionality. **Table 6.1** shows the pin configuration needed to perform this test. The output should be the logical NAND of the inputs. This test can be performed at DC or frequencies up to roughly 10MHz.

	Pin Name	Pin Number	Value
Inputs	A	38	0V or 5V
	B	37	0V or 5V
	vdd	40	5V
	gnd	20	0V
Output	NAND	36	NAND(A,B)

Table 6.1: NAND Gate Test

6.1.2 Frequency Divider Test

A test frequency divider is included on chip to test for circuit functionally and performance. It is a copy of the frequency divider used to create a 40MHz signal from the nominal 320MHz signal of the VCO when locked. It consists of three d-latches and a 4 stage output buffer and divides the input signal down by 8. Since the 4 stage buffer is only intended for applications up to 10 MHz, an input signal should be less than 80 MHz. **Table 6.2** shows the pin configuration needed to perform this test.

	Pin Name	Pin Number	Value
Inputs	T_ DIVID_ IN	8	0-5V square wave
	vdd	40	5V
	gnd	20	0V
Output	T_ DIVID_ OUT	9	1/8 input frequency

Table 6.2: 1/8 Frequency Divider Test

6.1.3 VCO Test

A test voltage controlled oscillator (VCO) circuit is included to test the functionality and performance of the VCO and 6-stage buffer. In this test the input voltage to the VCO is varied from roughly 1V to 4V and the corresponding output frequency is recorded. **Table 6.3** shows the pin configuration needed to perform this test.

	Pin Name	Pin Number	Value
Inputs	T_ VCO_ IN	10	1-4V DC
	vdd	2	5V
	vdd	40	5V
	gnd	20	0V
	gnd	22	0V
Output	T_ VCO_ OUT	32	0-5V Square wave proportional to input voltage

Table 6.3: VCO Test

6.1.4 DPLL Lock Range Test

The goal of this test is to find the minimum and maximum frequencies at which the DPLL will lock. An input range of 10MHz to 50MHz should cover the operating range. **Table 6.4** shows the pin configuration needed to perform this test.

6.1.5 DPLL Lock Time Test

The goal of this test is to find the the time it takes the system to lock using a 40MHz reference signal. To capture the lcok time an oscilloscope should be set to trigger on the first edge/rise of the reference signal and set to capture the output of the 320MHz pin. A capture time of 2 to 3 microseconds should

	Pin Name	Pin Number	Value
Inputs	REF	11	0-5V 10-50MHz Sinusoid
	vdd	2	5V
	vdd	40	5V
	gnd	20	0V
	gnd	22	0V
Outputs	320MHz	32	input frequency x 8
	10MHz	16	input frequency x 1/4
	0.625MHz	15	input frequency x 1/64
			to input voltage

Table 6.4: DPLL Lock Range Test

be sufficient to estimate the lock time with the estimated lock time being defined as the point at which the output is within 2MHz of 320MHz and stable. **Table 6.5** shows the pin configuration needed to perform this test.

	Pin Name	Pin Number	Value
Inputs	REF	11	0-5V 40MHz Sinusoid
	vdd	2	5V
	vdd	40	5V
	gnd	20	0V
	gnd	22	0V
Outputs	320MHz	32	input frequency x 8
	10MHz	16	input frequency x 1/4
	0.625MHz	15	input frequency x 1/64
			to input voltage

Table 6.5: DPLL Lock Time Test

6.1.6 DPLL Enable Test

The goal of this test to to ensure that the enable circuit is functional and provides a delay of roughly 5 microseconds. To capture the delay an oscilloscope should be set to trigger on the first edge/rise of the reference signal. The delay between this and the enable 0V to 5V transition is the delay time. **Table 6.6** shows the pin configuration needed to perform this test.

	Pin Name	Pin Number	Value
Inputs	REF	11	0-5V 40MHz Sinusoid
	vdd	2	5V
	vdd	40	5V
	gnd	20	0V
	gnd	22	0V
Outputs	Enable	6	0-5V Step, 5us delay
	320MHz	32	input frequency x 8
	10MHz	16	input frequency x 1/4
	0.625MHz	15	input frequency x 1/64
			to input voltage

Table 6.6: DPLL Enable Test

Chapter 7

Conclusion

A 320 MHz capable DPLL intended for RFID applications was designed and simulated for a 0.5μm process.

7.1 Improving Performance

There are several areas for improving the performance.

- The VCO is currently limiting the highest lock frequency. Modifying the VCO for higher frequency operation should allow the circuit to operate at frequencies upwards of 500MHz using the current process.
- Redesigning the DPLL for a smaller process should yield significant increases in the maximum lock frequency or could be used to reduce power. This should also yield a smaller device, reducing costs.
- A practical RFID tag needs to be a single chip solution. This eliminates the need for large output buffer with respect to the DPLL circuit. This would dramatically reduce the amount of switching power that the circuit requires.

7.2 Personal Note

It is not entirely clear how much time this project required, though it is undoubtedly in the triple digits if measured in hours. Nonetheless, it has been an enjoyable and valuable learning experience.

7.3 Biography

Patrick Spinney was born in St. Stephens, Canada and attended primary and secondary school in Eastport, Maine. He completed his BS in Electrical Engineering from the University of Maine in May 2004. He is currently a first year graduate student at the University of Maine studying toward a Master of Science in Electrical Engineering with a focus in microelectronics. Patrick is a member of the IEEE and Tau Beta Pi.

Appendix A

Schematics

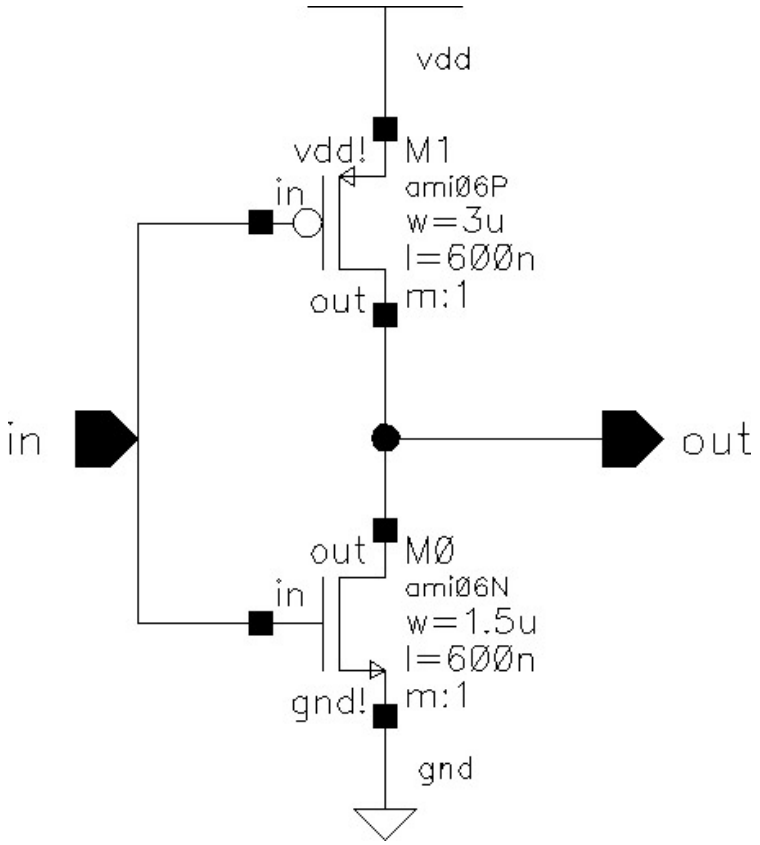

Figure A.1: Minimum Inverter

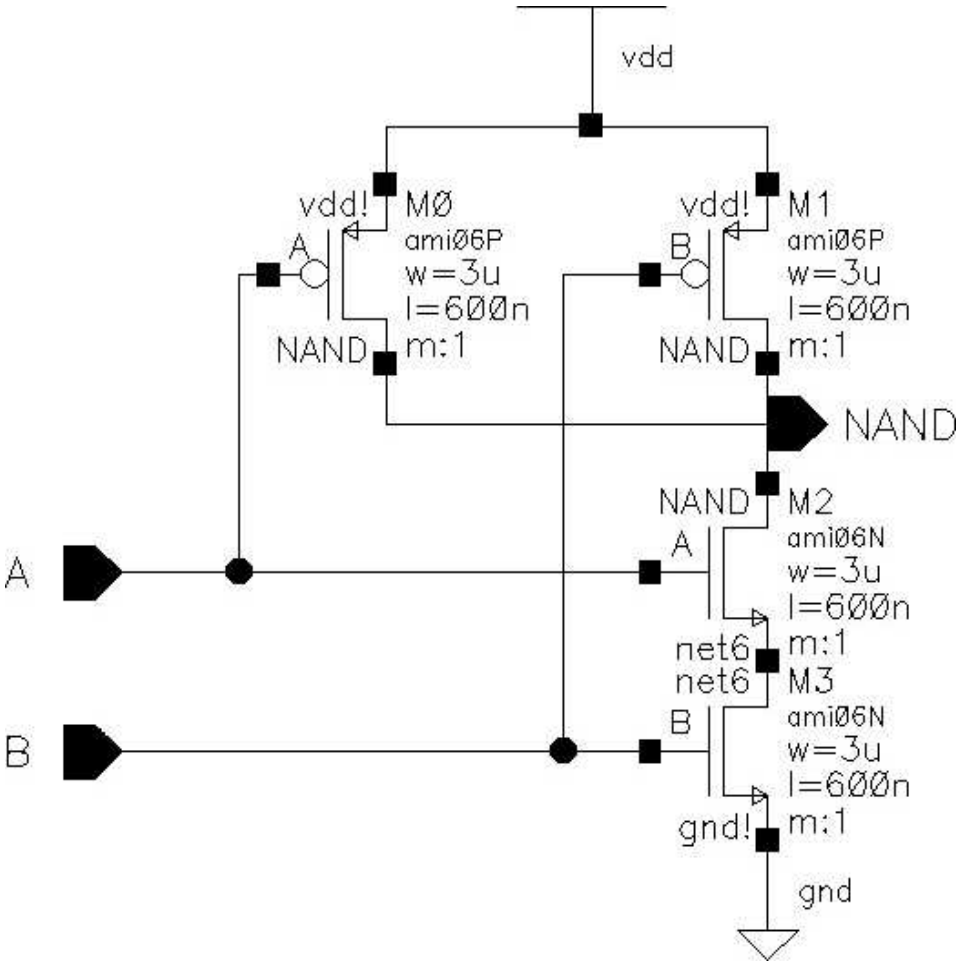

Figure A.2: 2 Input NAND Gate

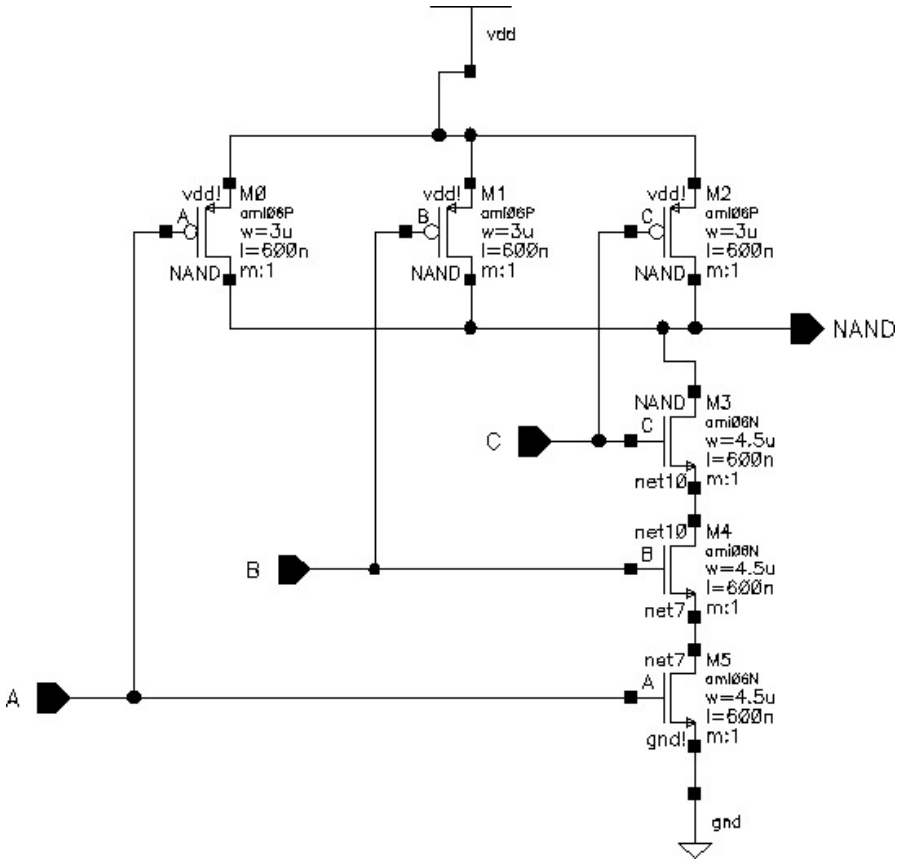

Figure A.3: 3 Input NAND Gate

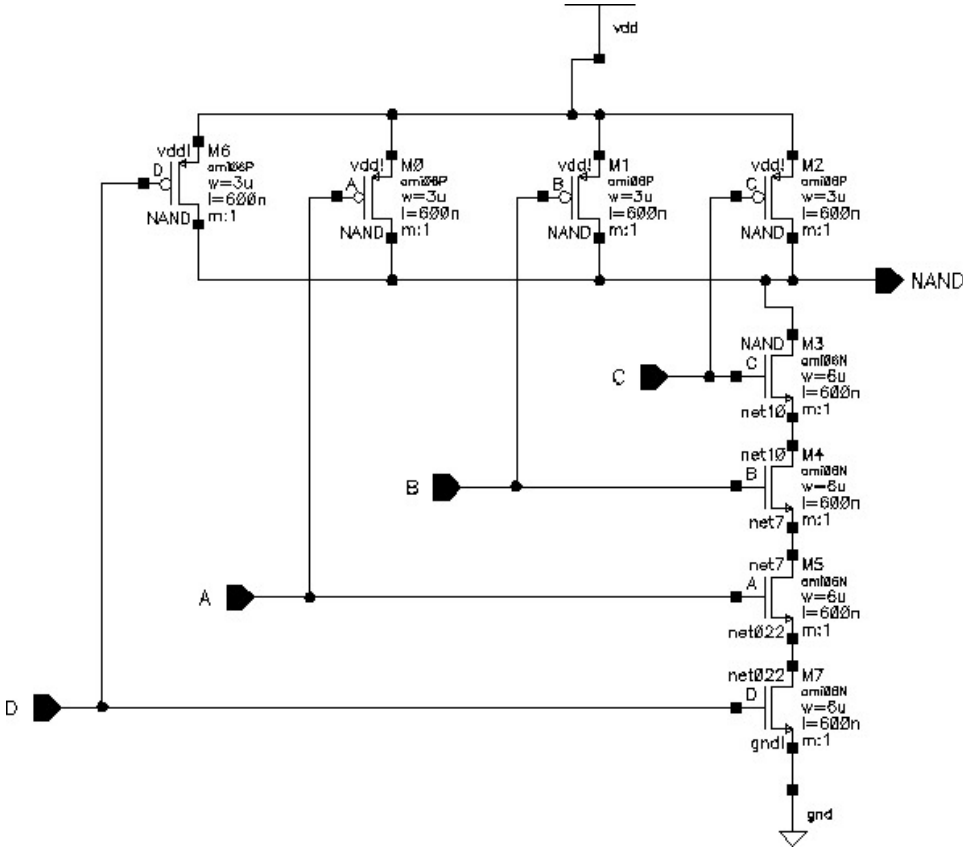

Figure A.4: 4 Input NAND Gate

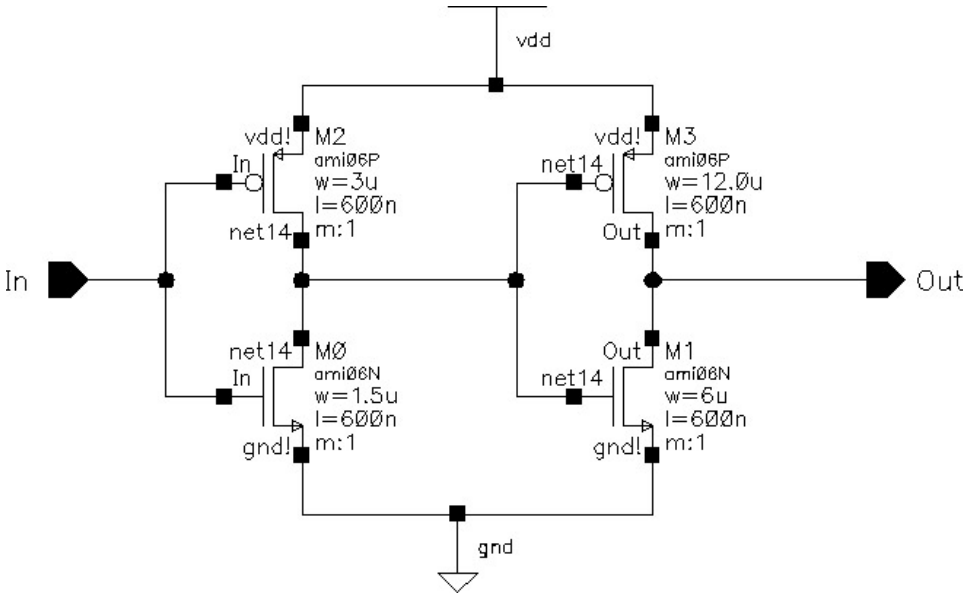

Figure A.5: 2 Stage Buffer

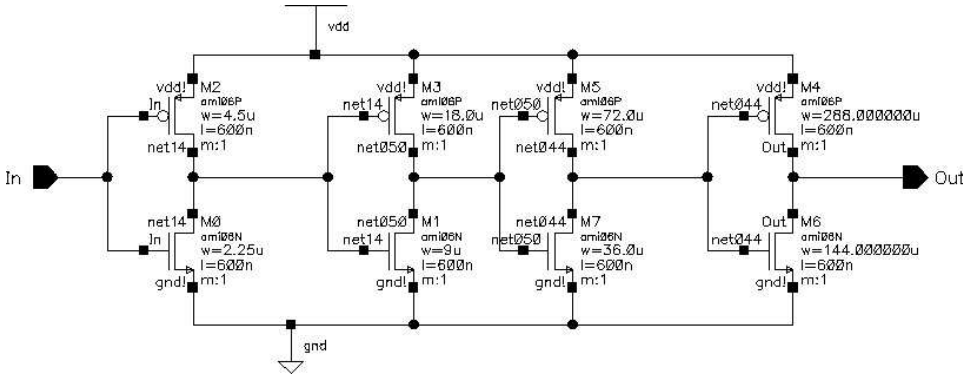

Figure A.6: 4 Stage Buffer

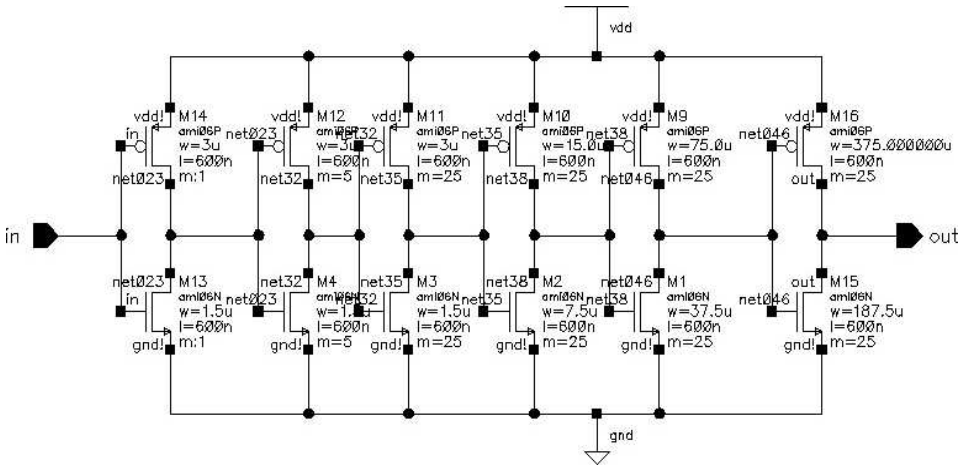

Figure A.7: 6 Stage Buffer

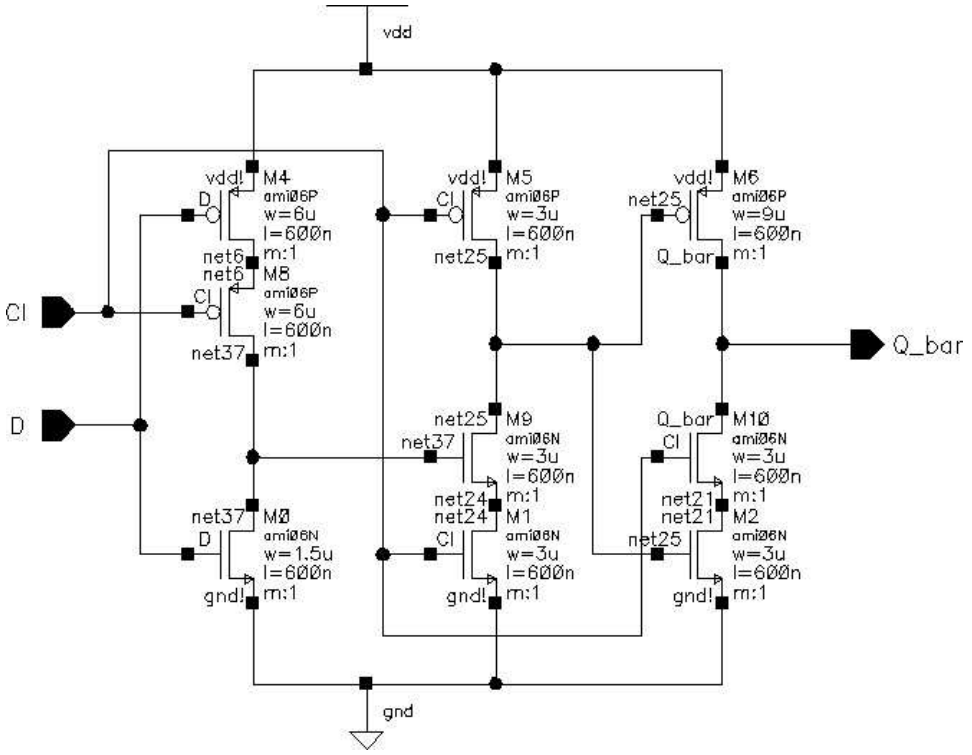

Figure A.8: D-Latch

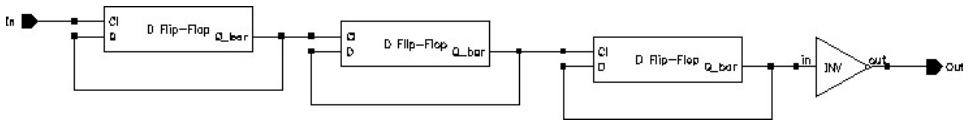

Figure A.9: Divider A

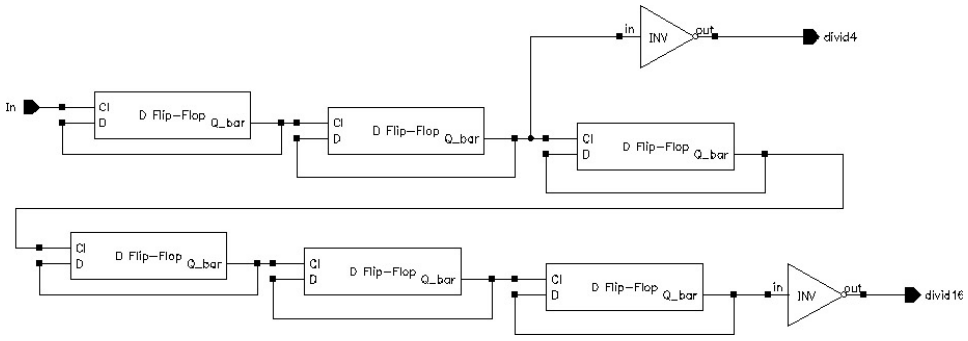

Figure A.10: Divider B

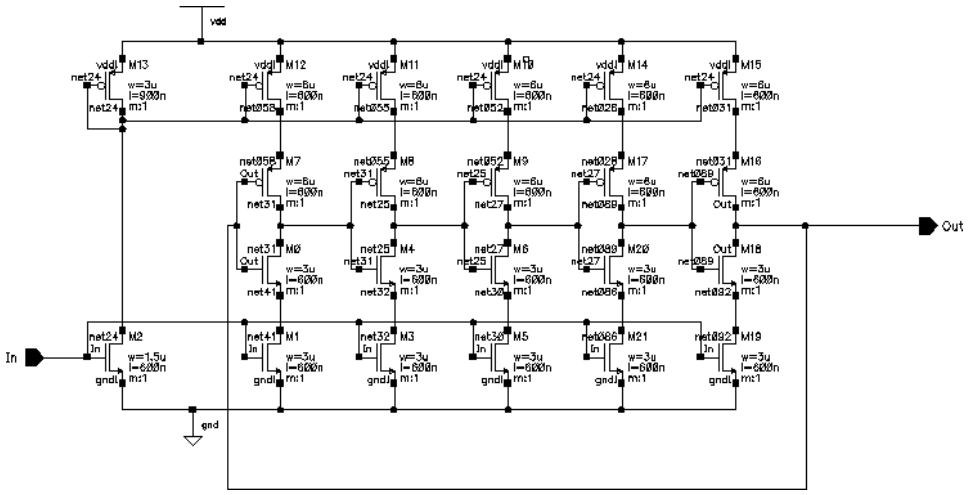

Figure A.11: VCO

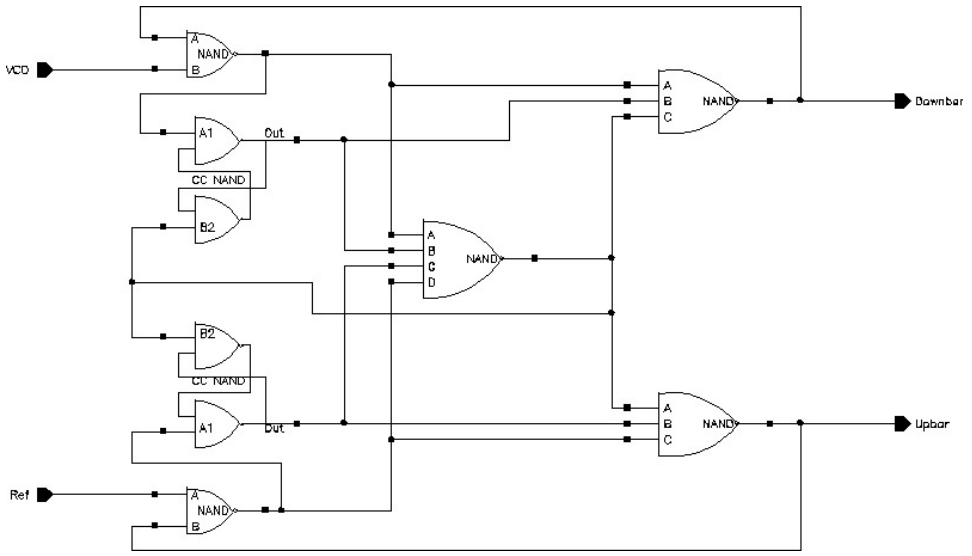

Figure A.12: PFD

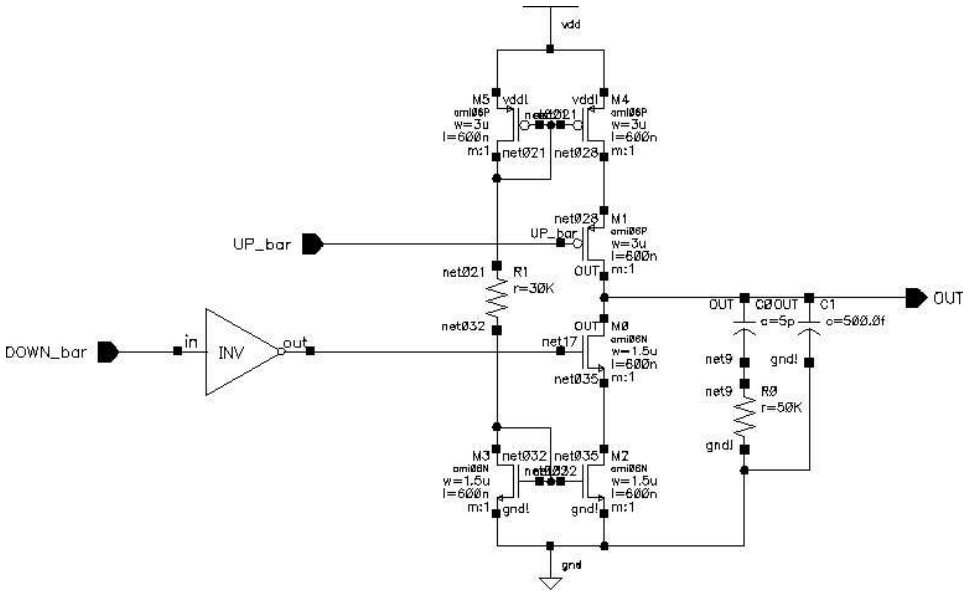

Figure A.13: Charge Pump

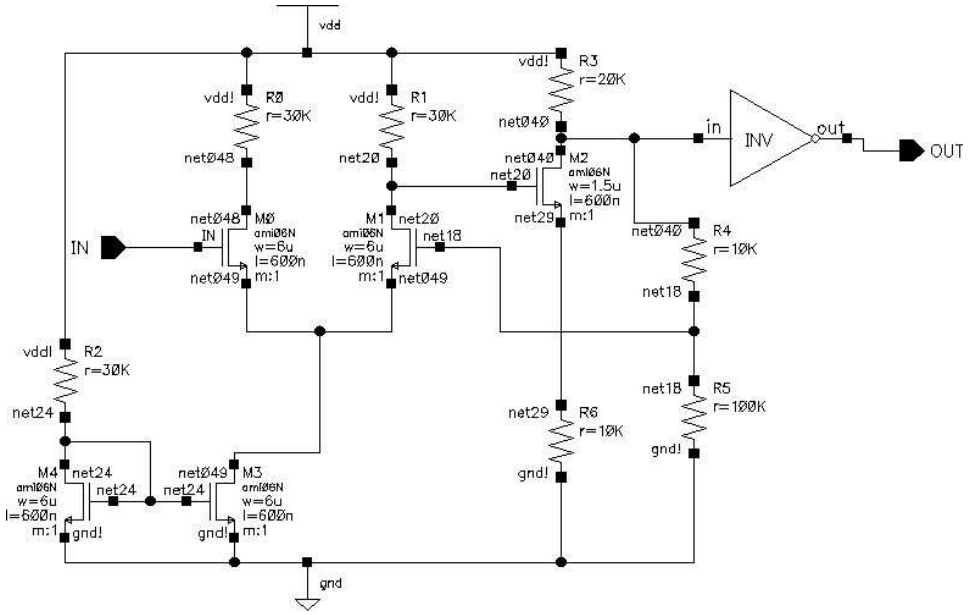

Figure A.14: Comparator

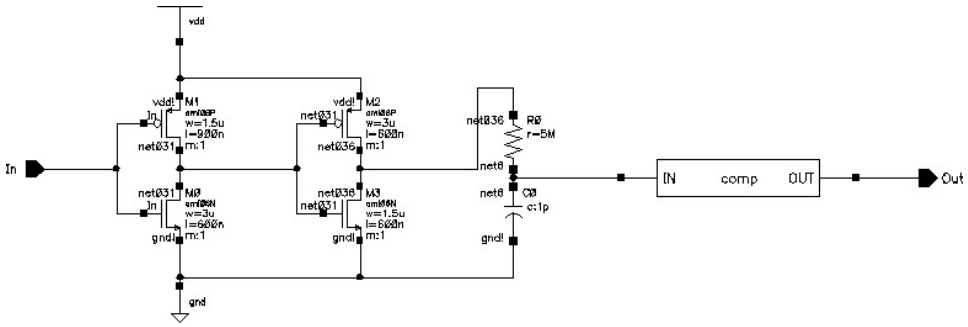

Figure A.15: Enable

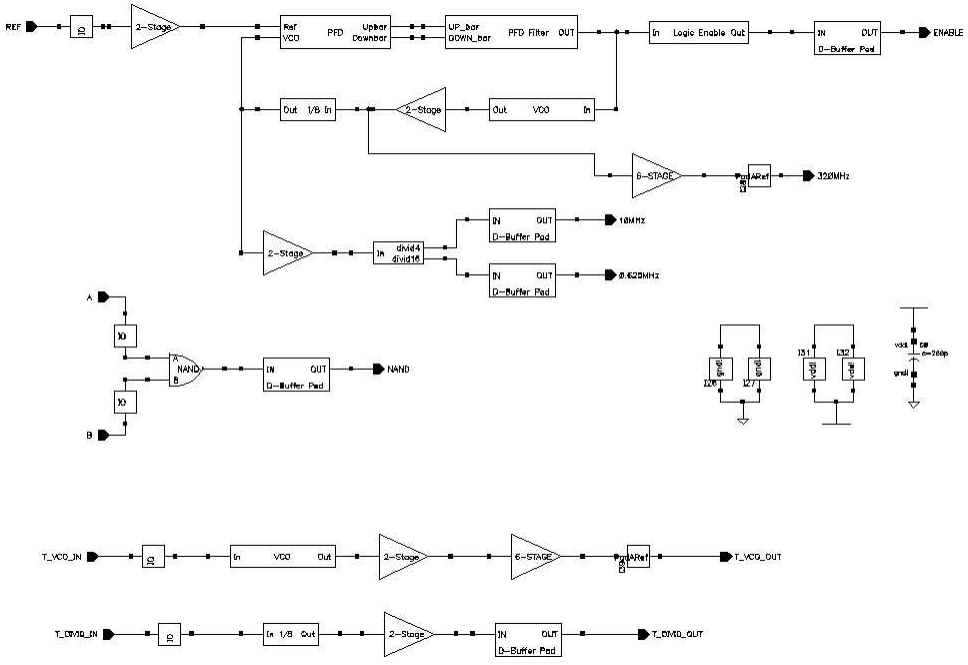

Figure A.16: Complete Chip

Appendix B

Physical Layout

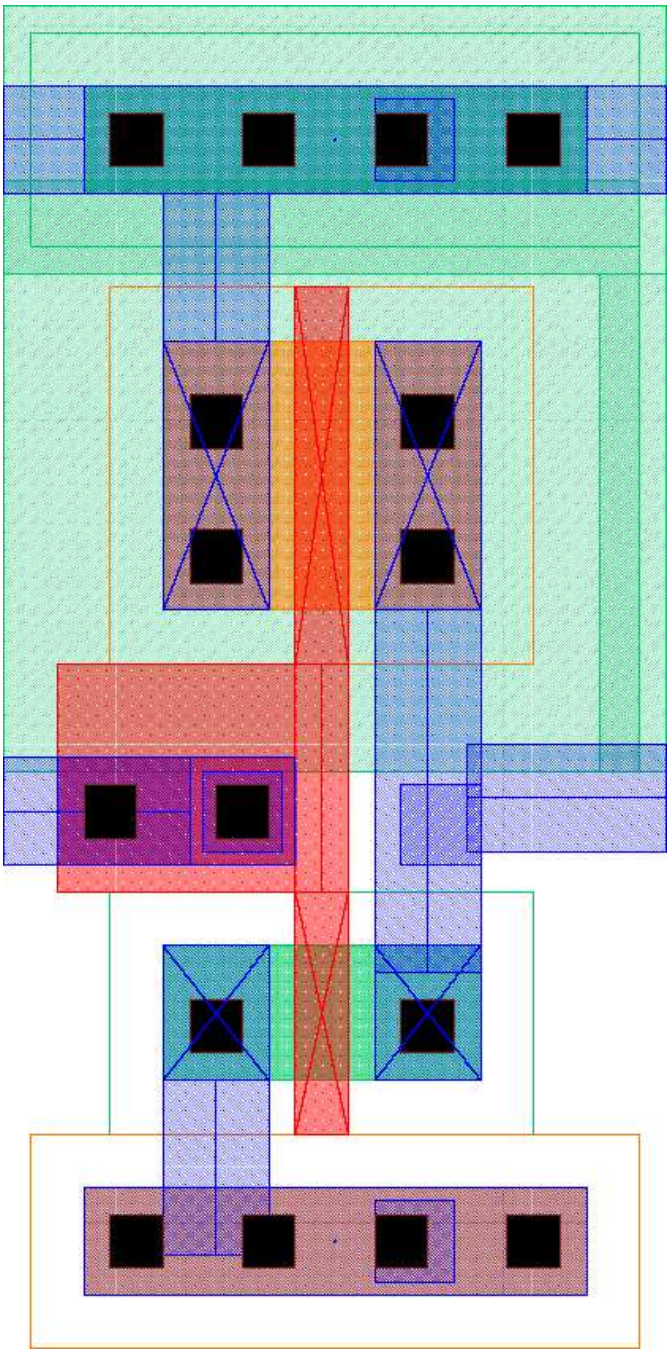

Figure B.1: Minimum Inverter

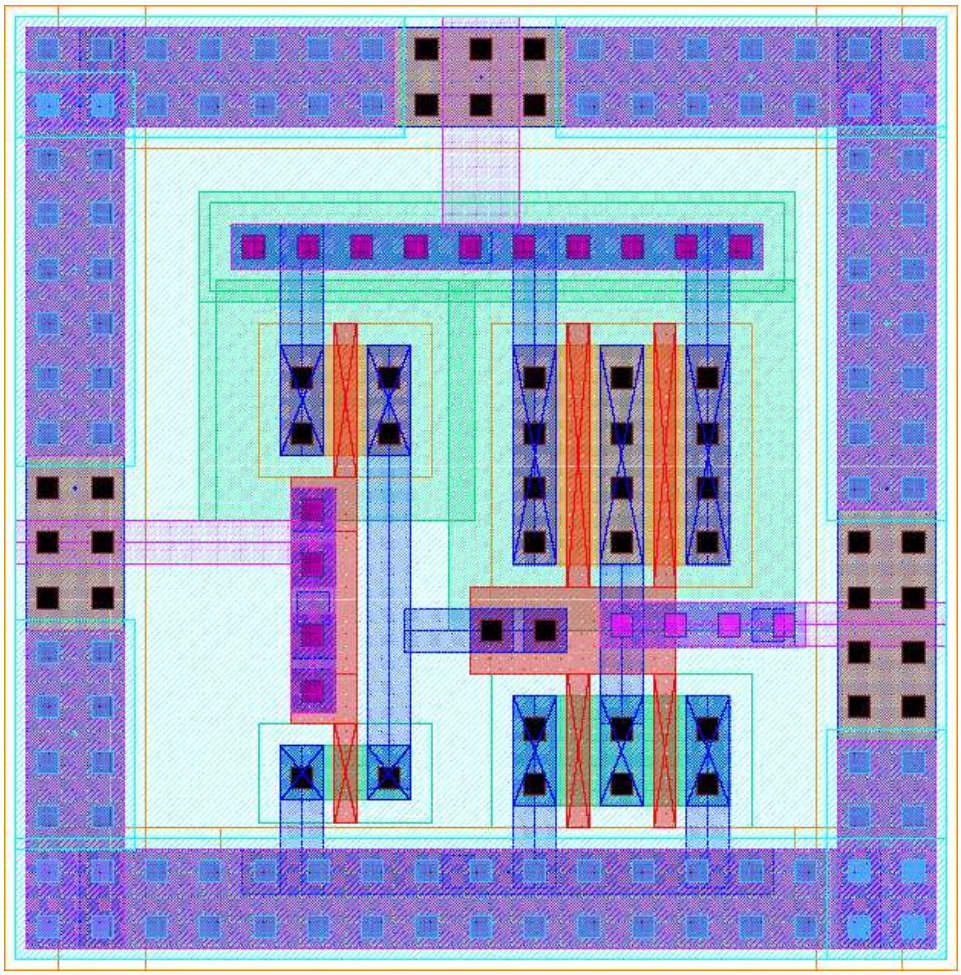

Figure B.2: 2 Input NAND Gate

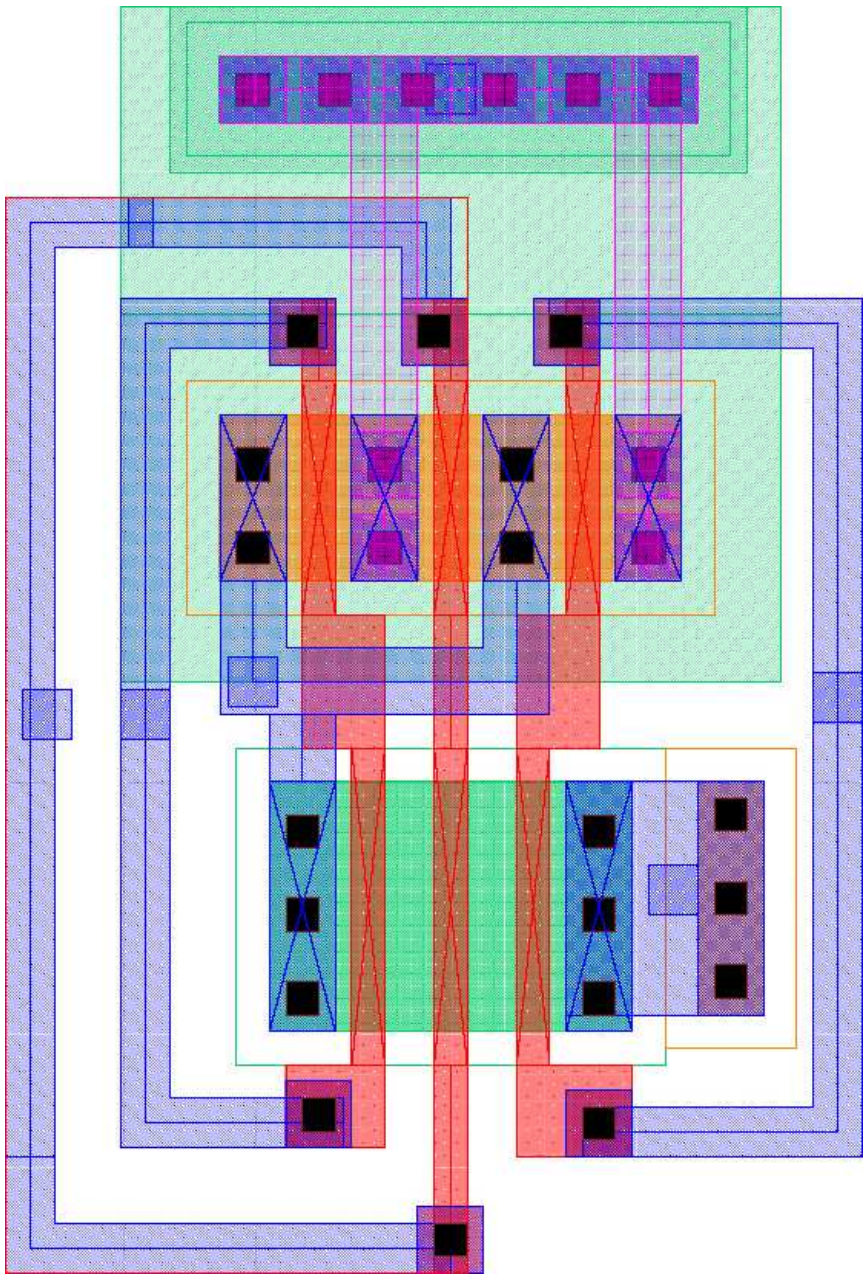

Figure B.3: 3 Input NAND Gate

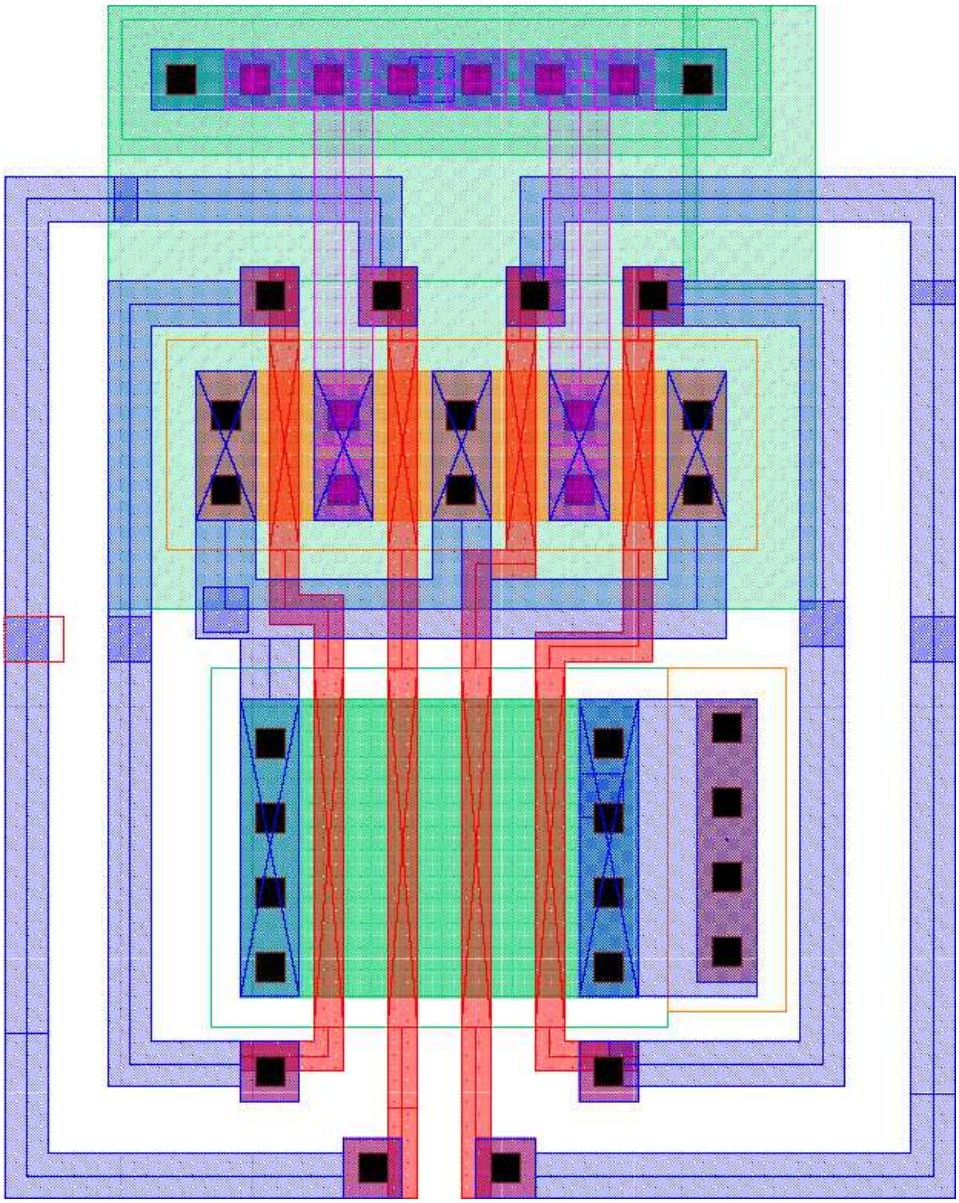

Figure B.4: 4 Input NAND Gate

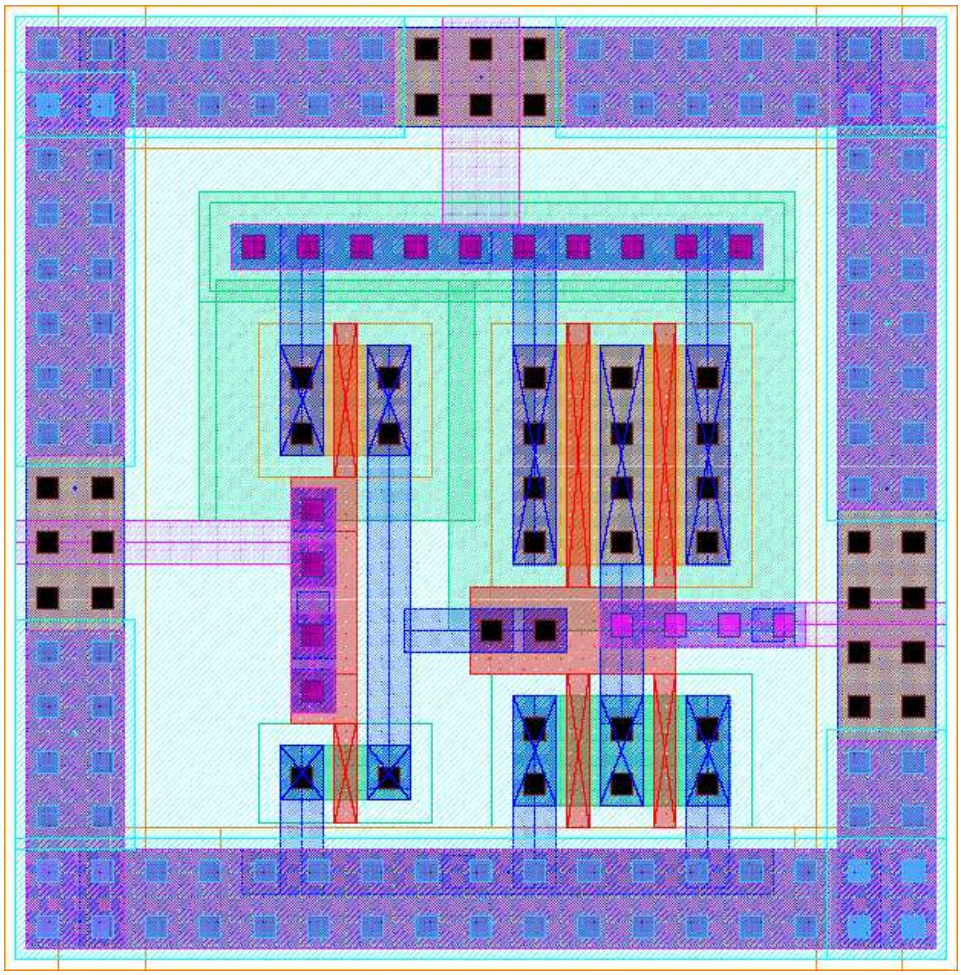

Figure B.5: 2 Stage Buffer

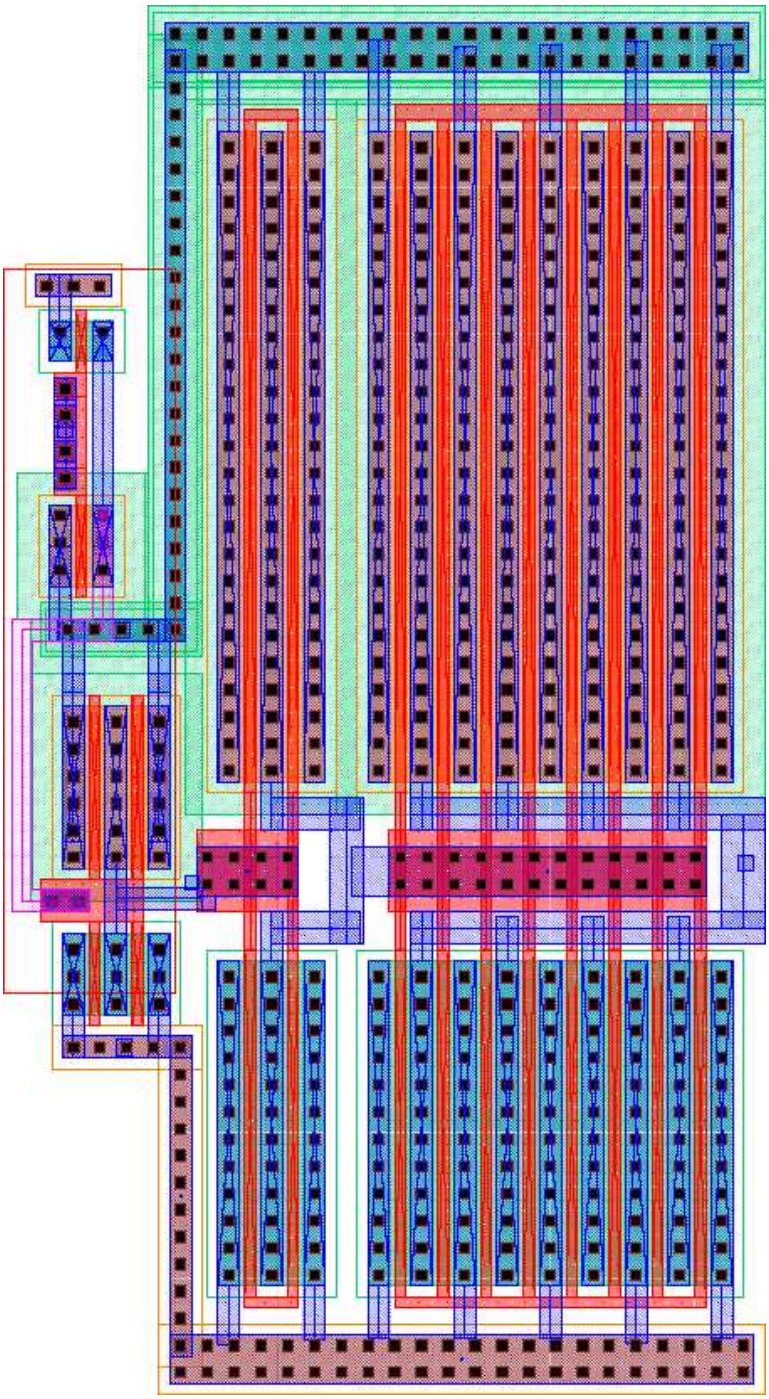

Figure B.6: 4 Stage Buffer

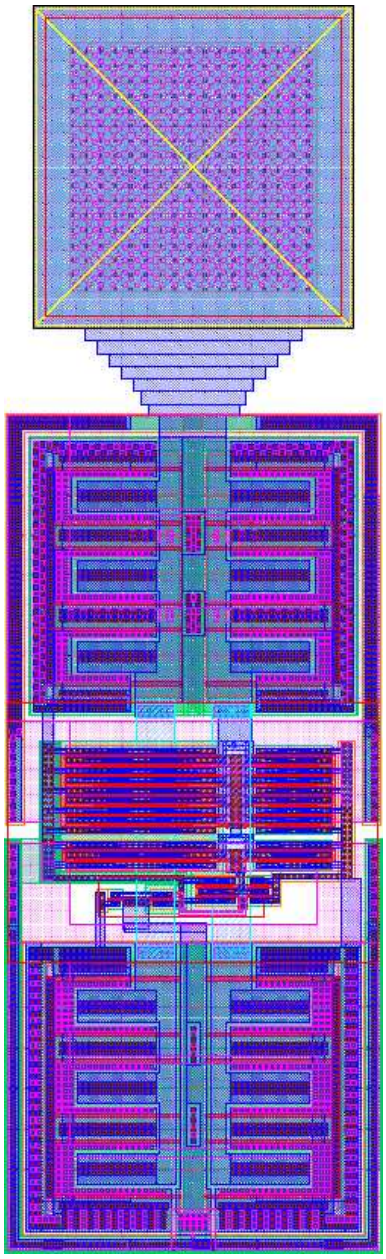

Figure B.7: 4 Stage Buffer within Padset

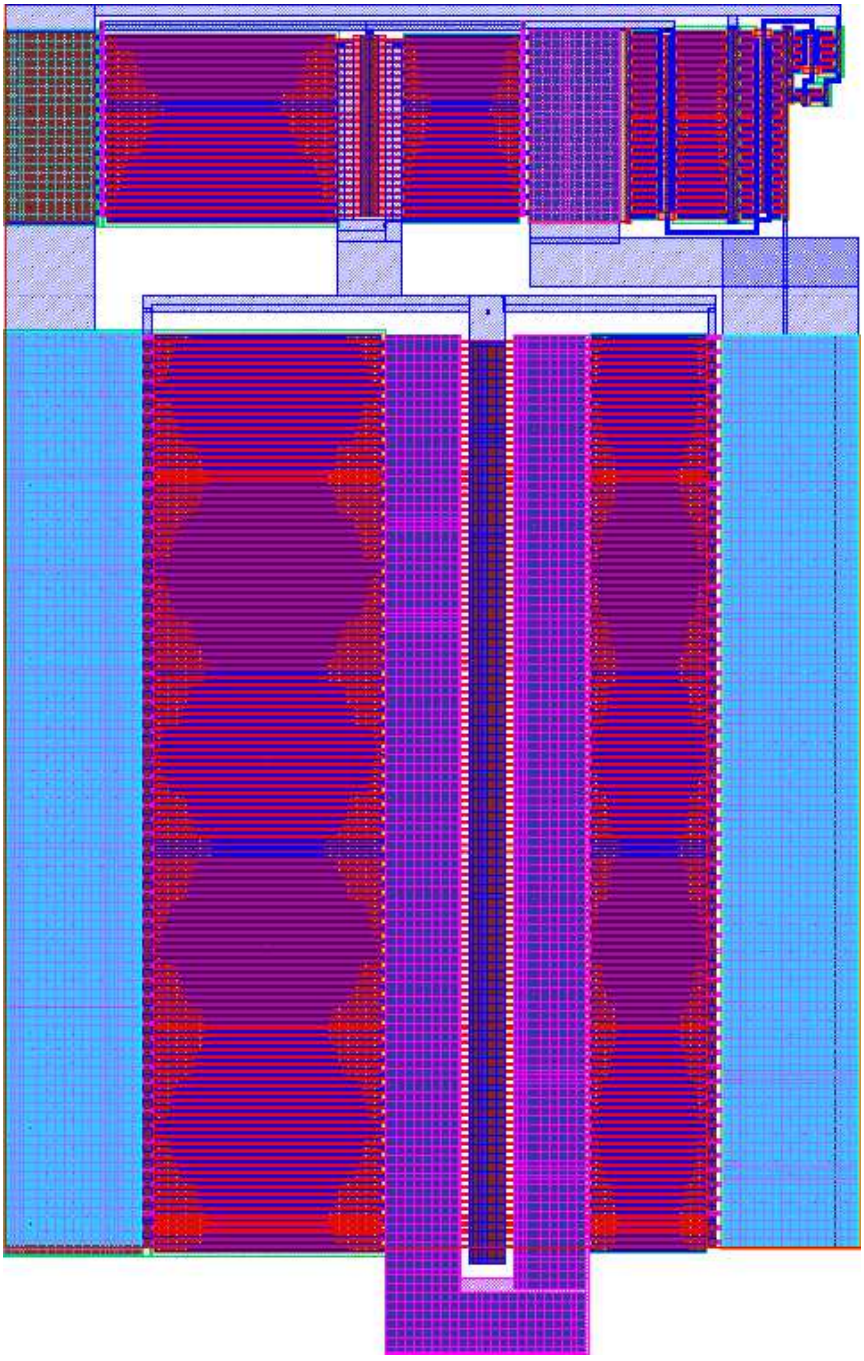

Figure B.8: 6 Stage Buffer

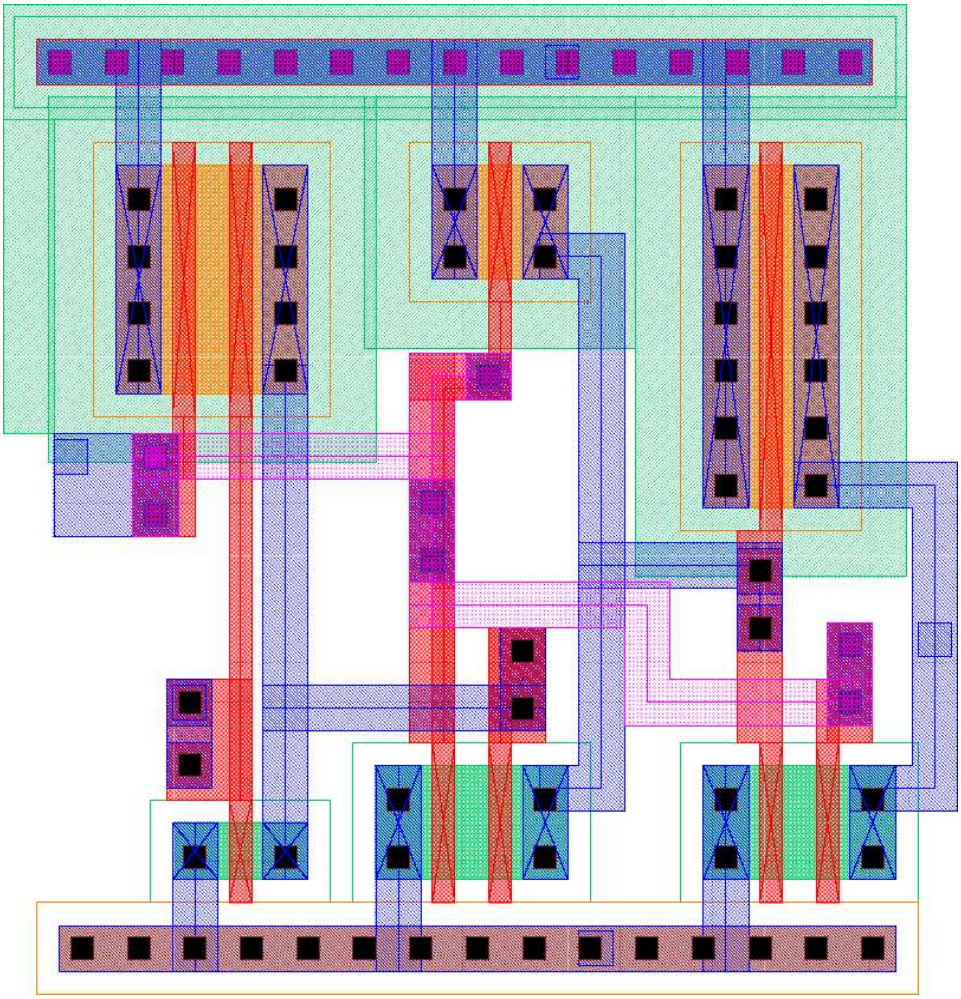

Figure B.9: D-Latch

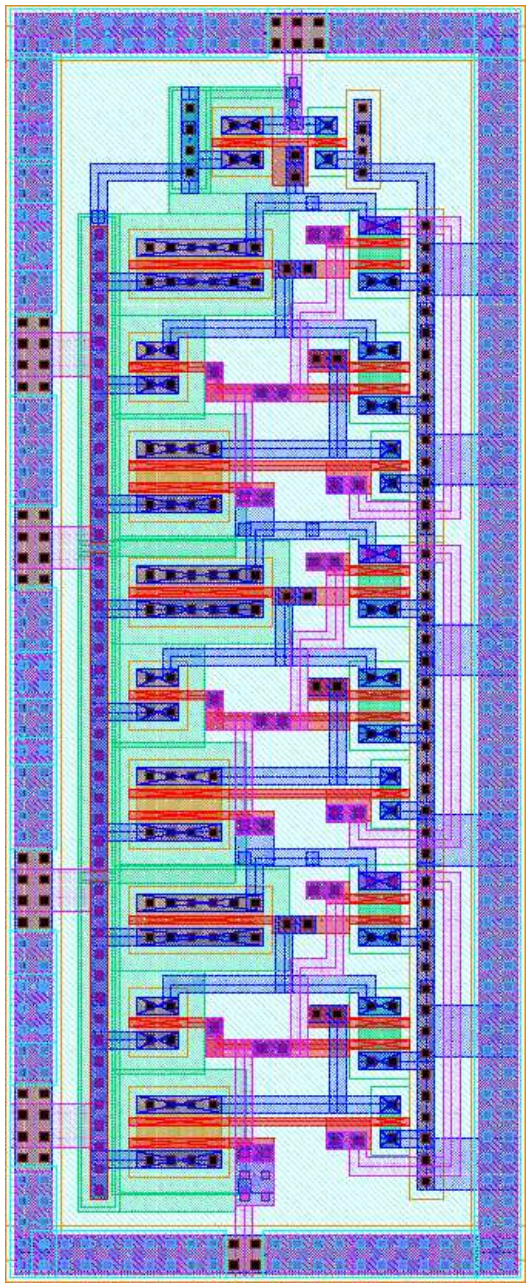

Figure B.10: Divider A

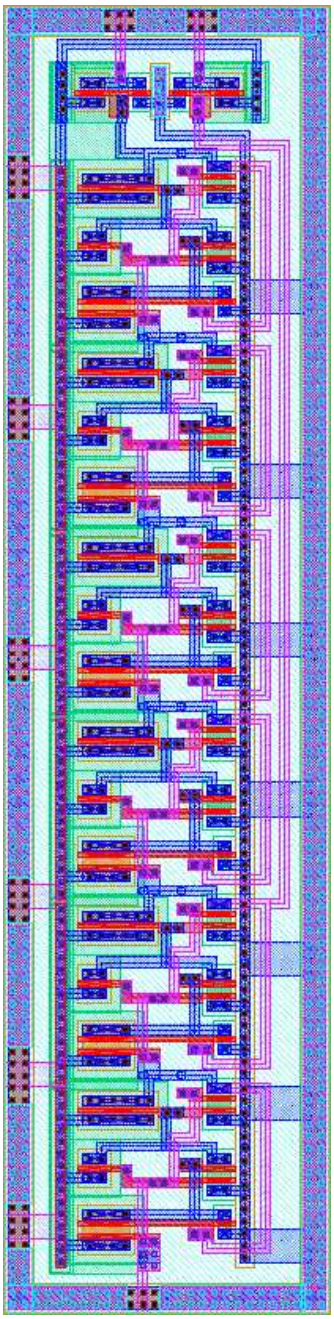

Figure B.11: Divider B

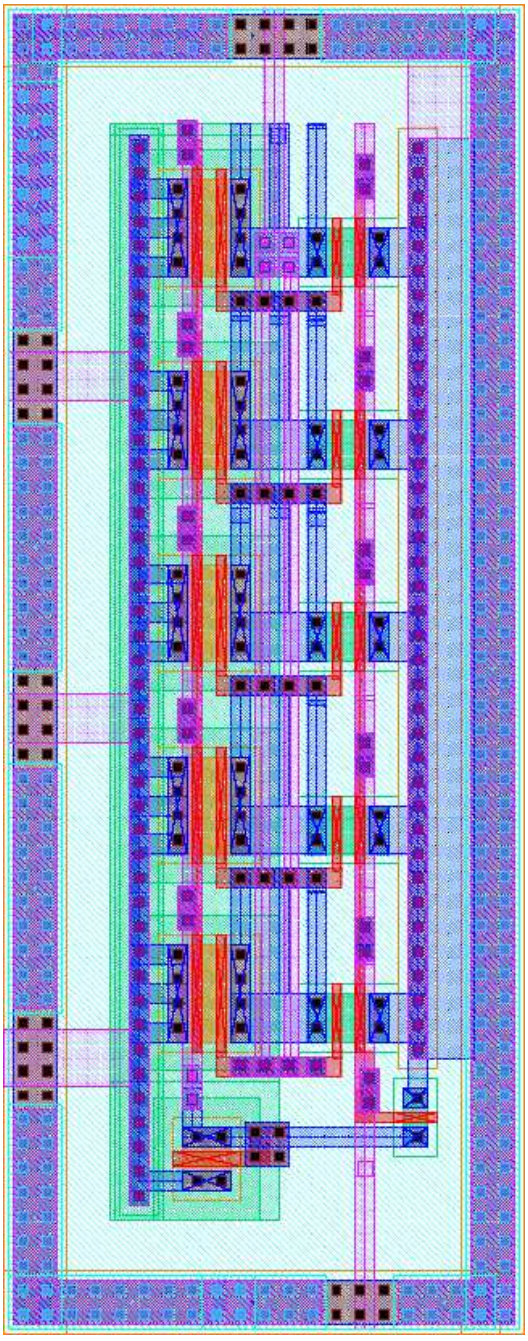

Figure B.12: VCO

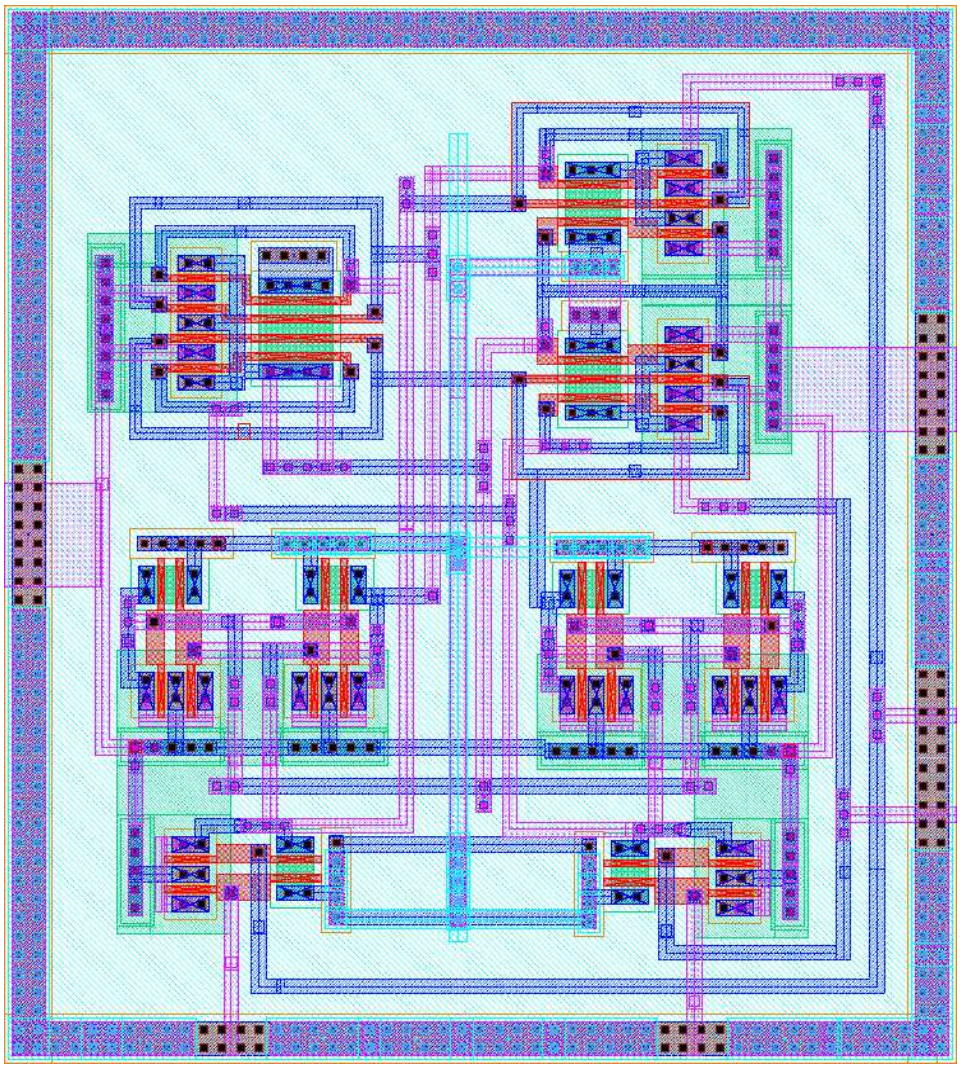

Figure B.13: PFD

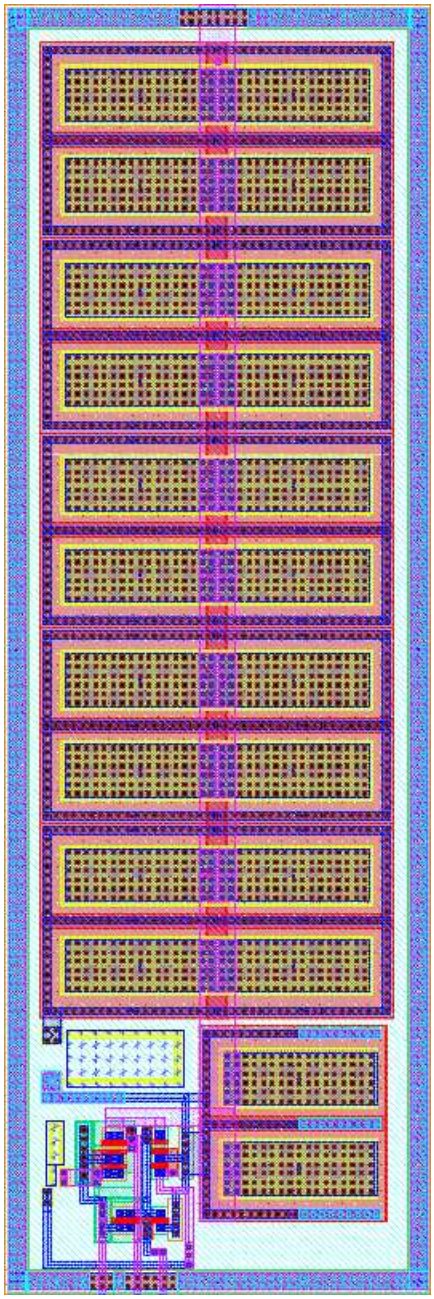

Figure B.14: Charge Pump

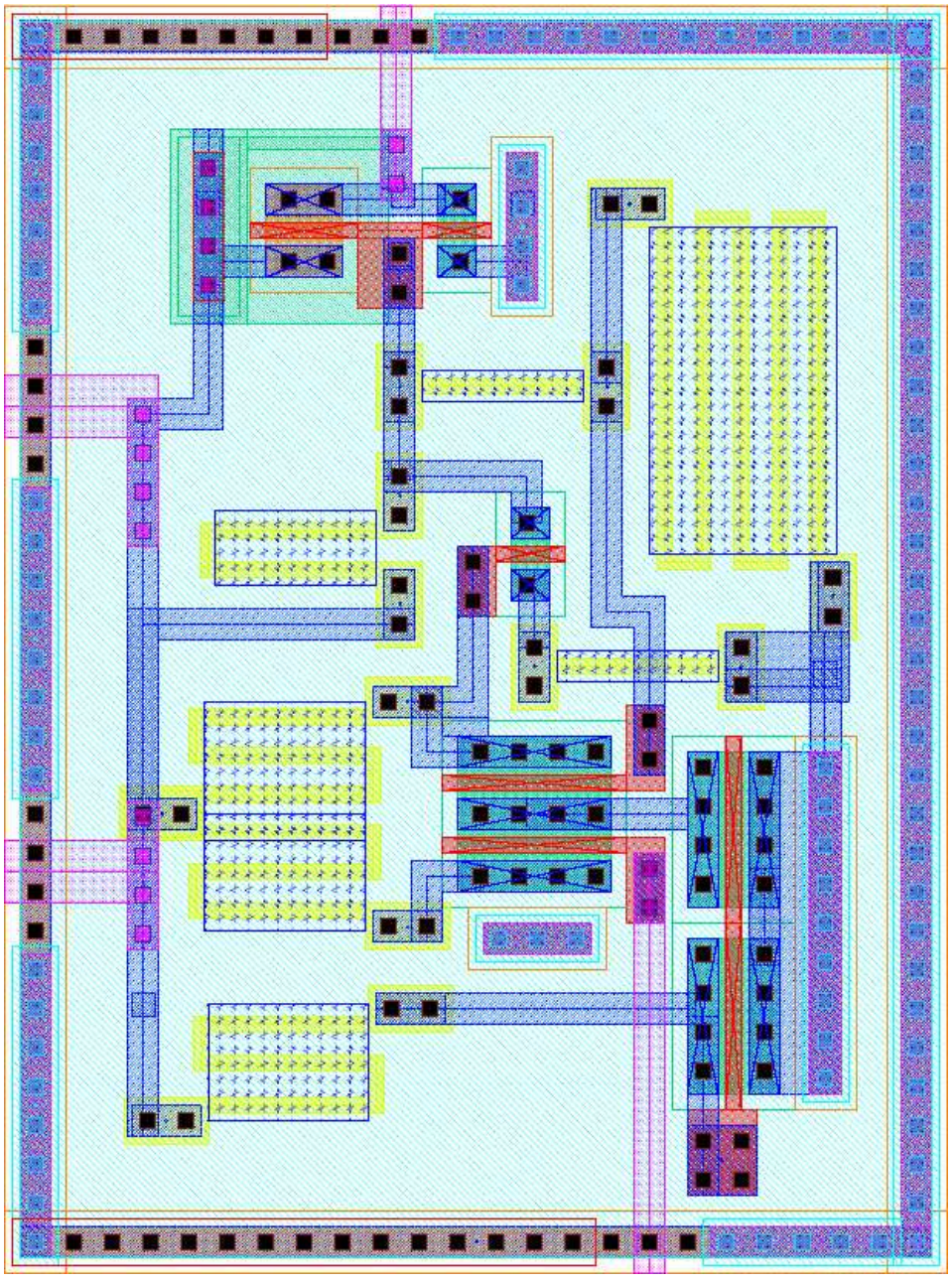

Figure B.15: Comparator

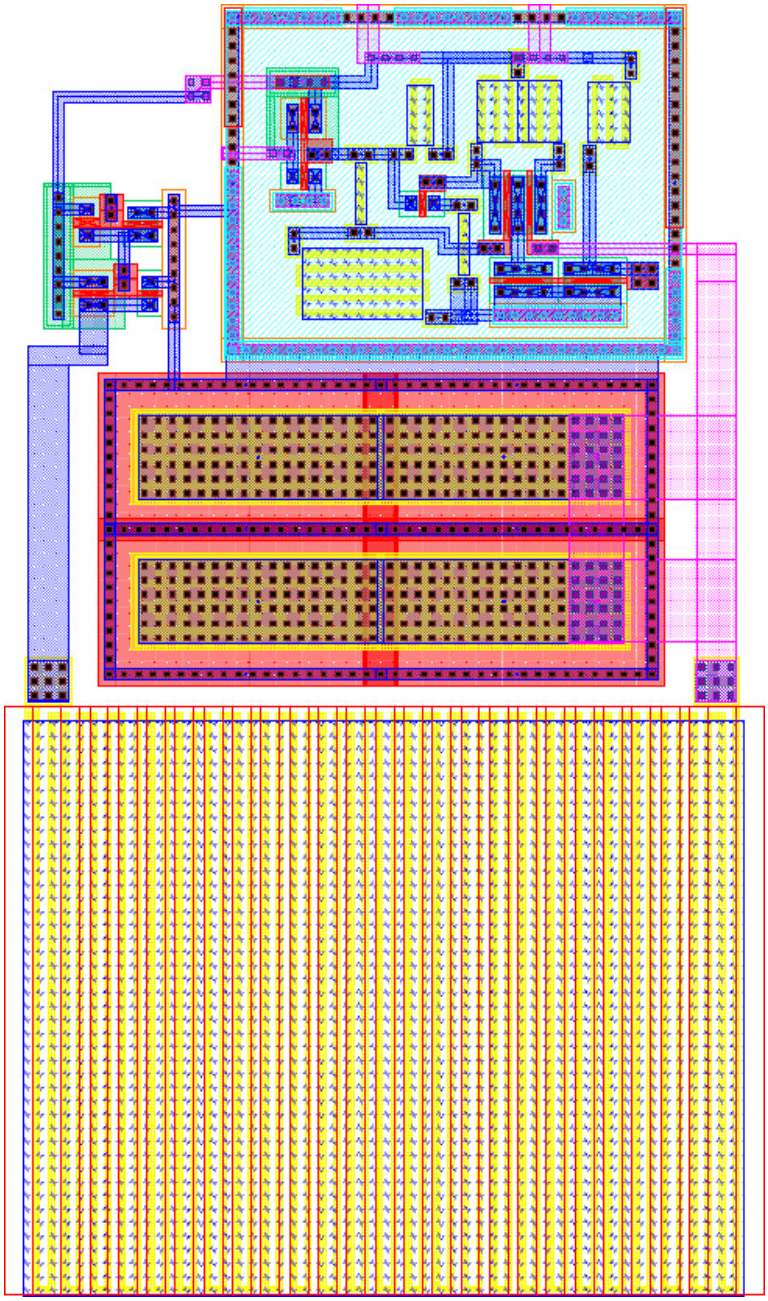

Figure B.16: Enable

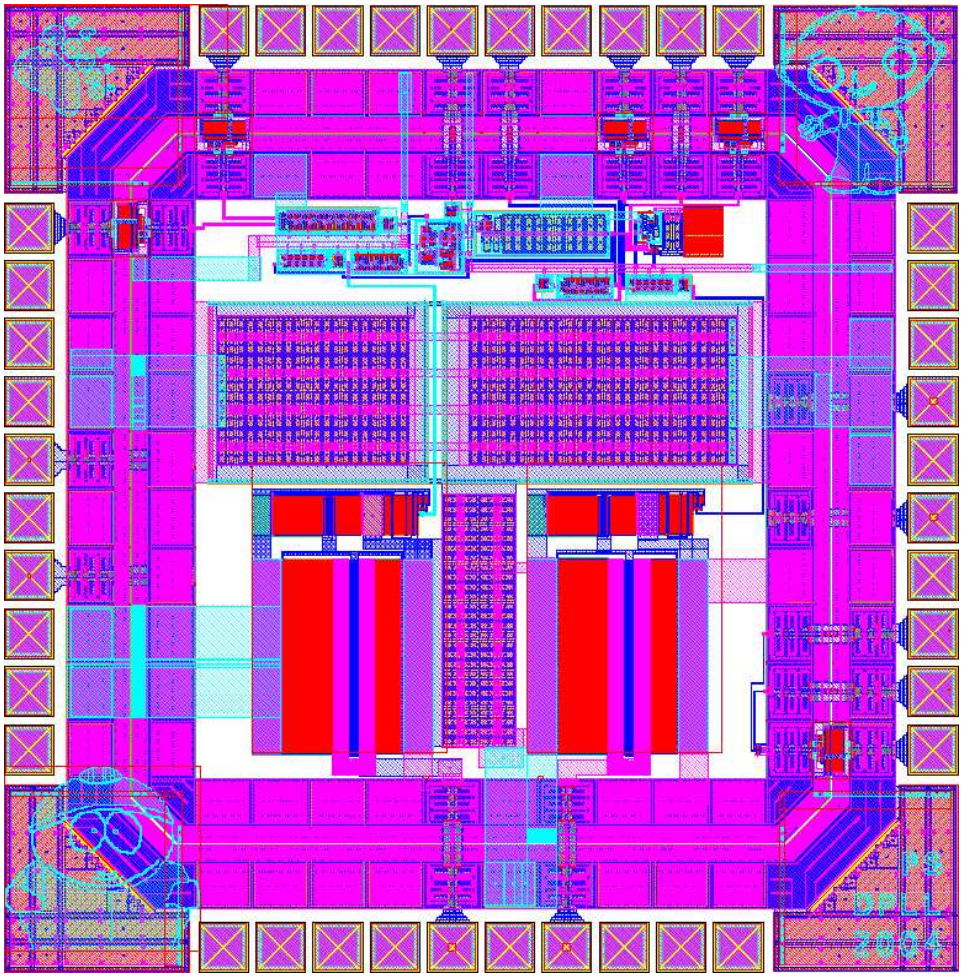

Figure B.17: Complete Chip

Appendix C

Pinout Diagram

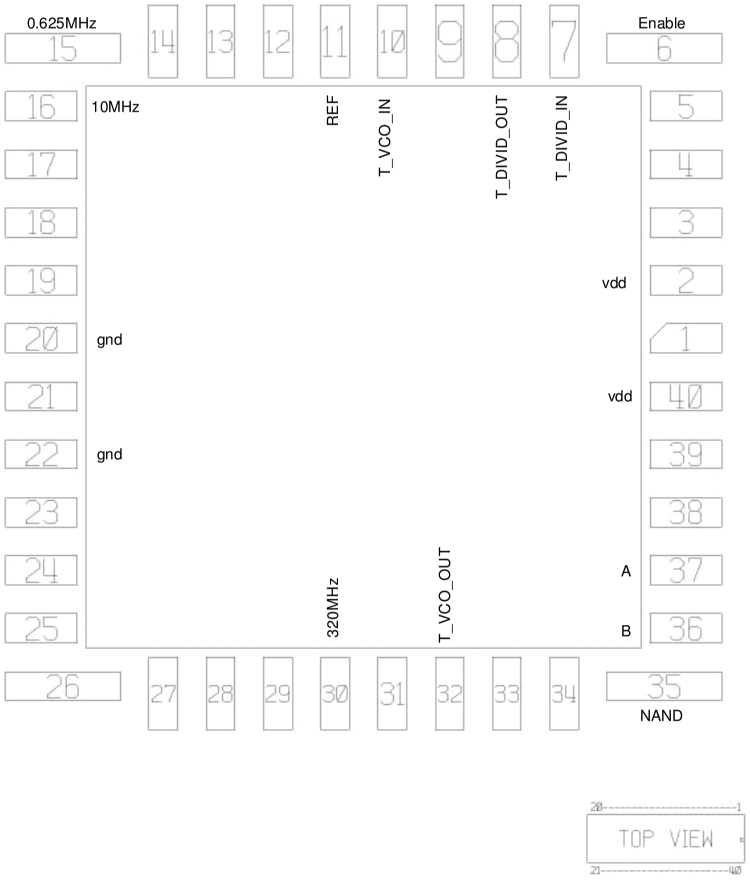

Figure C.1: Pin Out

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