5MHz PIPELINE ANALOG TO DIGITAL CONVERTER VLSI CIRCUIT DESIGN

ELECTRICAL AND COMPUTER ENGINEERING
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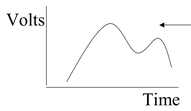
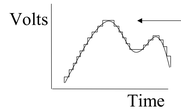
INTRODUCTION: The Very Large Scale Integrated circuit (VLSI) design process has four phases: 1) Circuit Design and Simulation, 2) Physical Layout and Simulation, 3) Fabrication, 4) Test and Characterization. This pipeline Analog to Digital Converter (ADC) is unique in that the intermediate digital data is routed off chip for research considerations. The basic concepts of analog to digital conversion is:



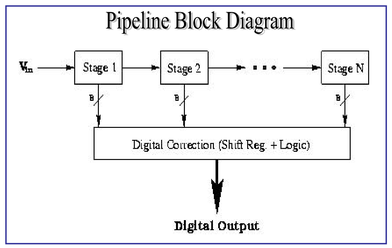
Analog Signals are continuous in time. The voltage level can represent physical quantities such as temperature, pressure, sound etc.



Digital signals represent analog signals in discrete steps. An analog to digital converter samples the continuous signal and outputs a digital number, read by a computer, equal to the sampled voltage level. The smallest step size is the resolution of the ADC.

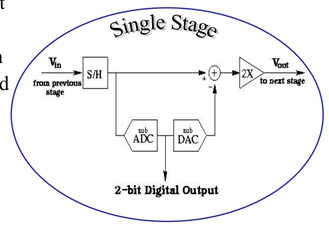
Design Concept

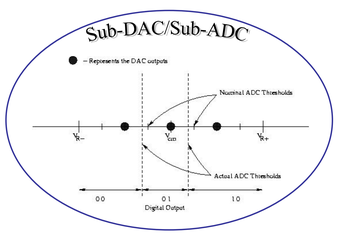
The pipeline ADC architecture consists of N, high speed, low resolution cascaded stages. The digital output of each stage is stored in a shift register. Correction logic circuitry provides 10 bit resolution off chip. The advantages of breaking down the conversion into many stages are:



- High conversion rate
(The data is valid at each clock cycle).
- Chip size is reduced
(The sample rate is not governed by number of stages, minimal stages can be used).
- Increased resolution
(Additional stages can be added to increase the final output resolution).

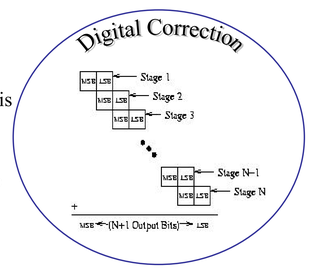
This design utilizes 9 stages with 2 bit outputs fed to the shift register. The sub-DAC converts stage outputs to an analog signal. This signal is subtracted from the original sample creating the residue. The residue x 2 is passed to the next stage. This maintains low stage resolution. Non-overlapping clocks control alternate stages. The system models parallel processing.





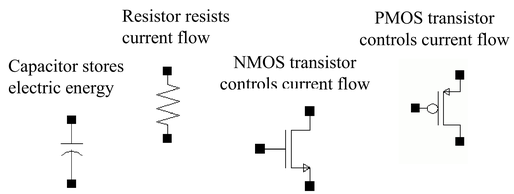
Each stage compares inputs to constant thresholds, in the sub-ADC. The sub-DAC converts the 00, 01 or 10 sub-ADC output to the indicated analog thresholds.

The 18 raw output stage bits, stored in the shift register, are corrected to 10 bits by the correction logic. In this design the intermediate outputs, MSB and LSB, of the first 4 stages, are routed off chip to aid in pipeline error compensation research.

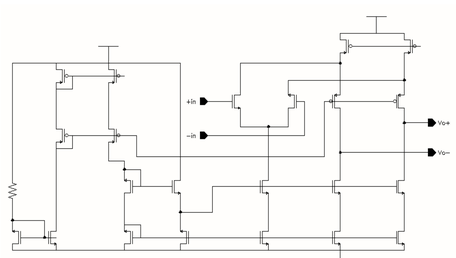


Circuit Design and Simulation

Basic Circuit Components and Schematic Symbols

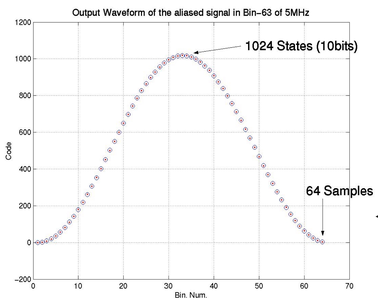


Circuit components are used as building blocks to design complicated circuits that perform a desired function.



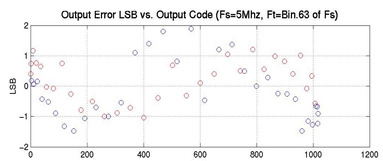
Small portion of the pipeline stage schematic.

Design Simulation Results.

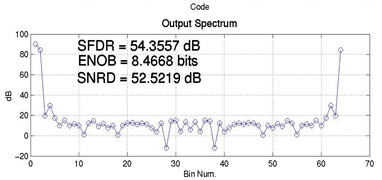


Comparison of an input sinusoid '**o**' to the converted output '**.**'

The error plot indicates the error between the simulated and ideal converted signal.

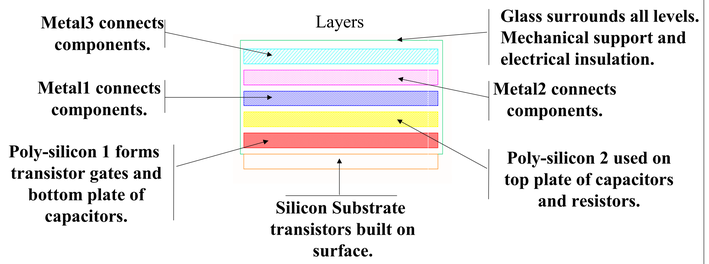


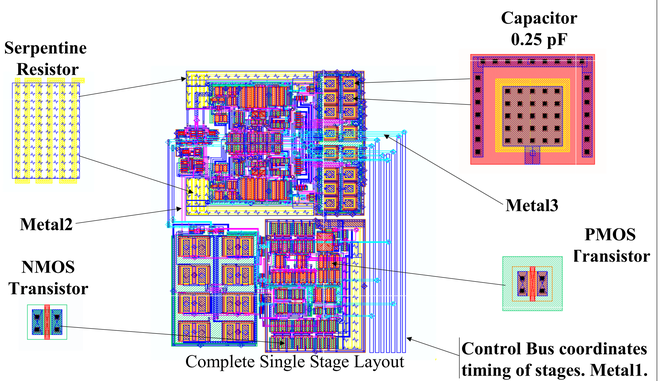
The power spectrum yields:
SFDR - Spurious Free Dynamic Range
ENOB - Effective Number of Bits
SNRD - Signal to Noise Ratio with Distortion



Physical Layout and Simulation

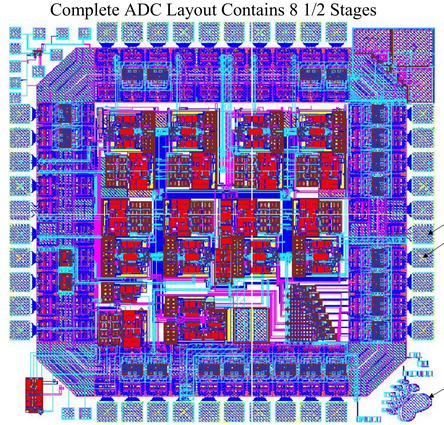
Physical design is the art of creating and placing geometric shapes needed to produce photo-lithographic masks. These masks are used in chip fabrication. The circuits are built on a silicon substrate in layers. The colors allow designers to visually separate layers when viewed from the top.





Complete Single Stage Layout

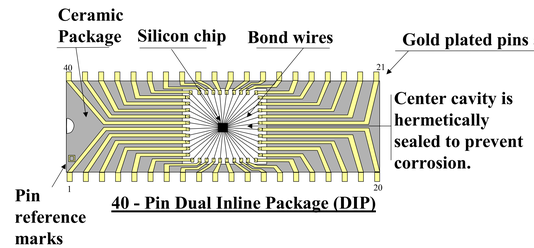
Complete ADC Layout Contains 8 1/2 Stages



Dimensions	30	305	2073	2854
1.5x1.5mm	Resistors	Capacitors	PMOS	NMOS

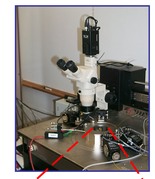
Fabrication

This chip is fabricated by AMI using the C5N process. The smallest line or trace possible in this process is .5 microns. These devices are processed in clean rooms that are 100,000 times cleaner than a typical office space. There are over 300 steps in the fabrication process and a wafer is 8 weeks in process.



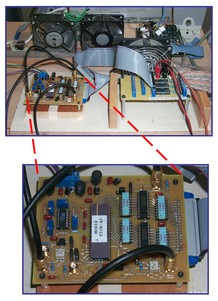
ACTUAL CHIP

Test and Characterization



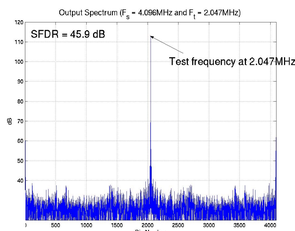
The manufactured chip is probed using a Cascade Microtech probe station. On chip test pads can be probed using this equipment.

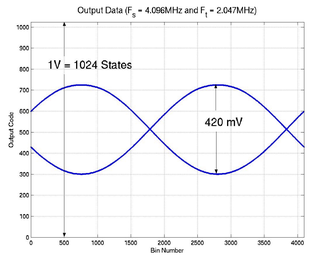
A 2-layer printed circuit test board was designed to test the ADC.



Characterization Results.

Preliminary results show that the ADC is able to provide valid 10-bit data. A 15% reduction in performance from design simulation is observed.





This chip is still in active characterization . . .

www.eece.maine.edu/vlsi/pipeline

. . . for more information.