Appendix B - Physical Design (Color)

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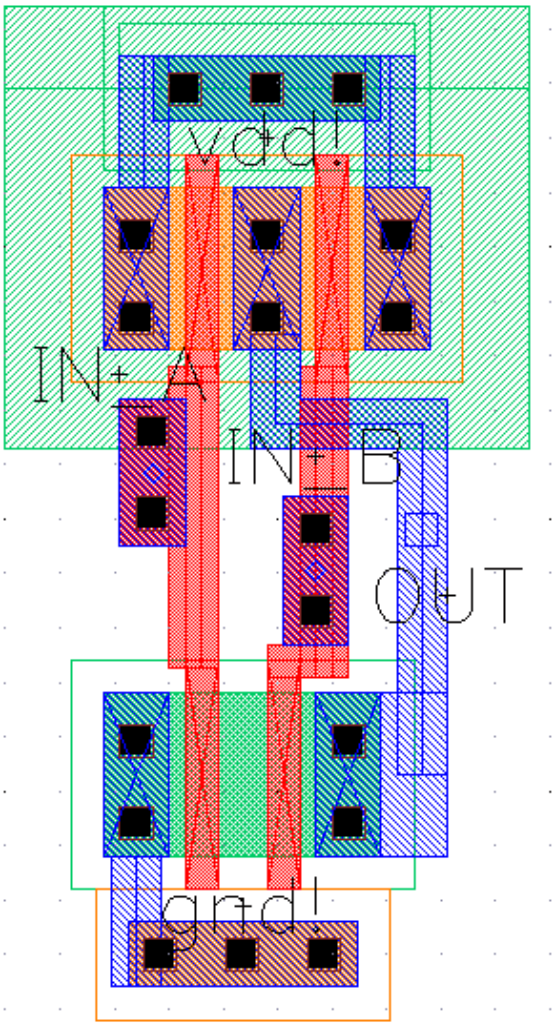

Figure 1: 2 Input NAND Gate.

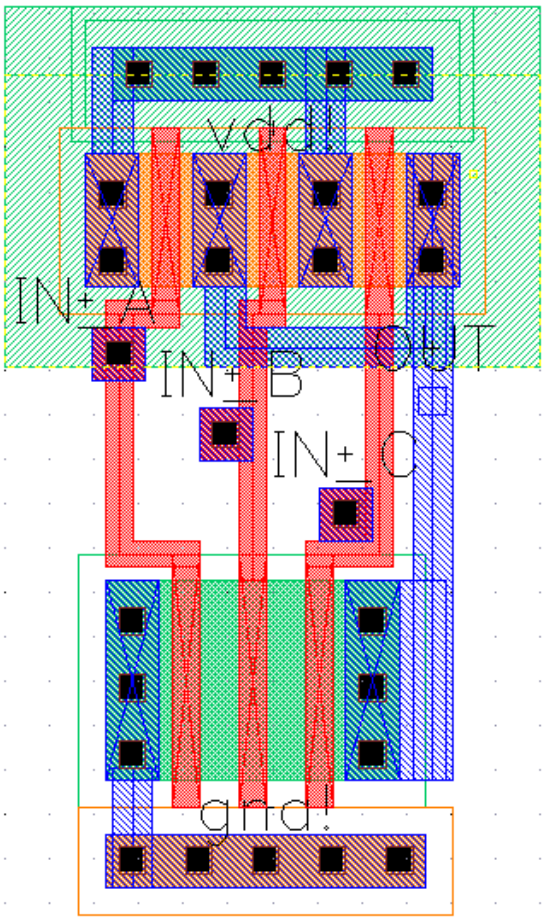

Figure 2: 3 Input NAND Gate.

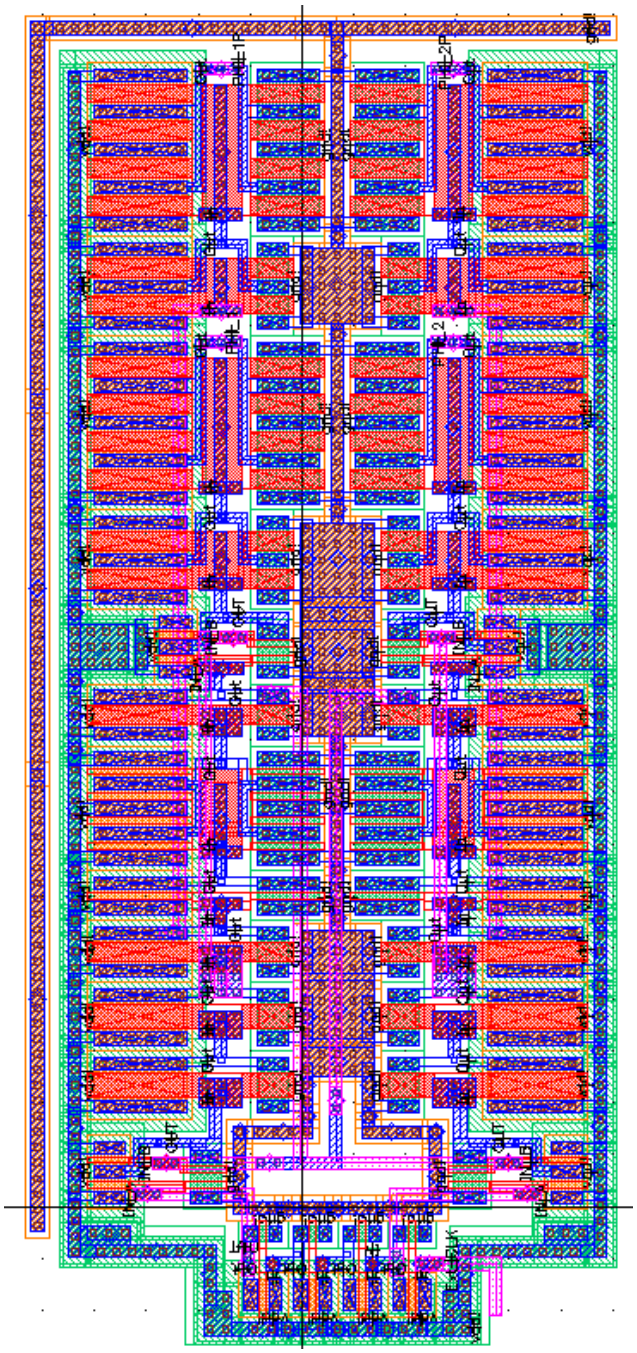

Figure 3: 2 Phase Non-Overlapping Clock.

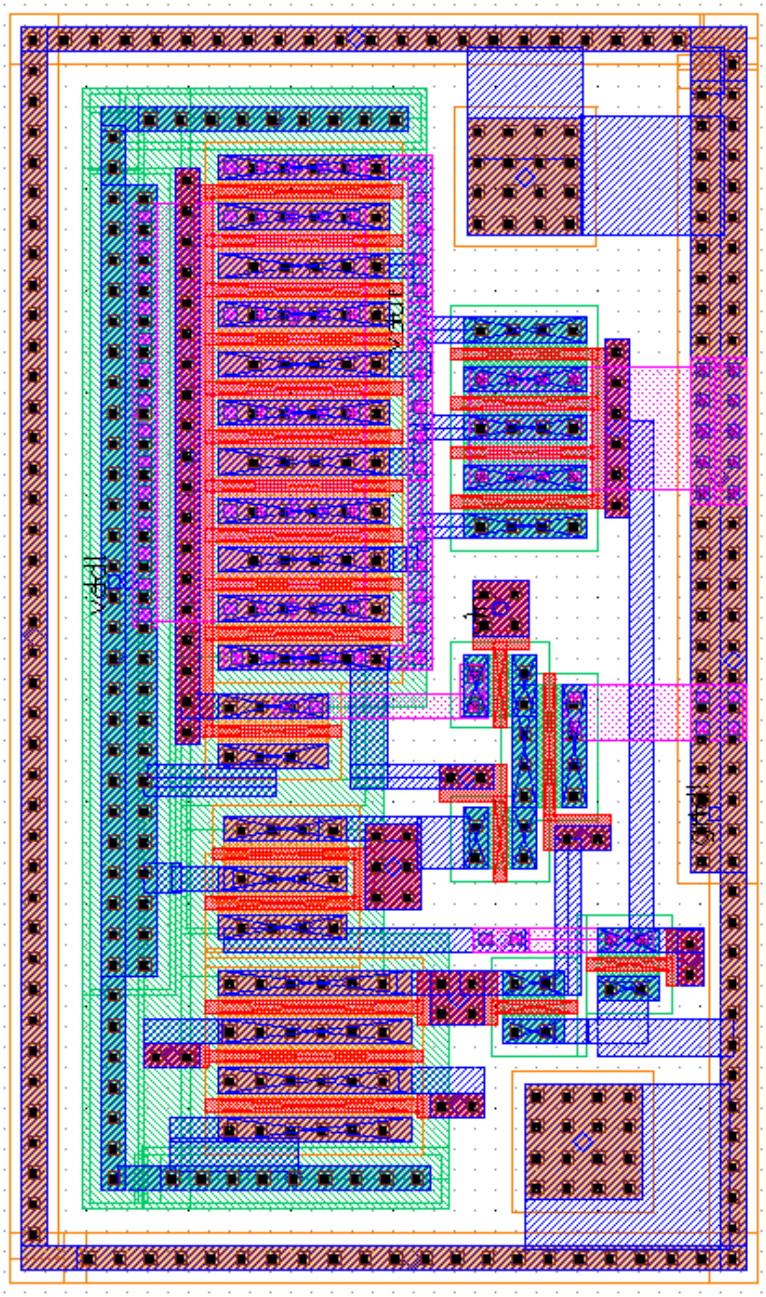

Figure 4: Analog Buffer.

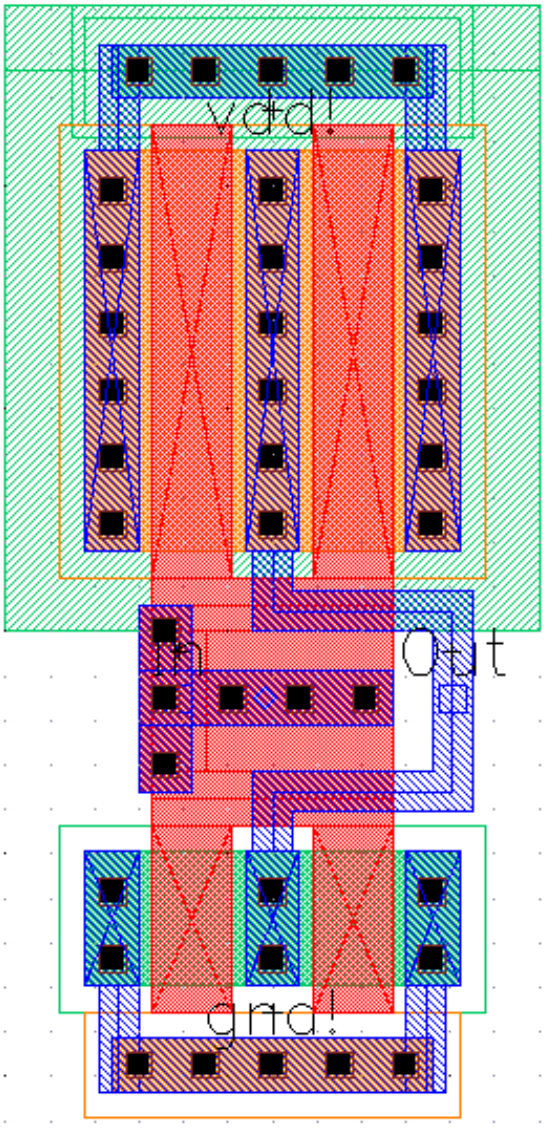

Figure 5: Buffer BUFF_1.

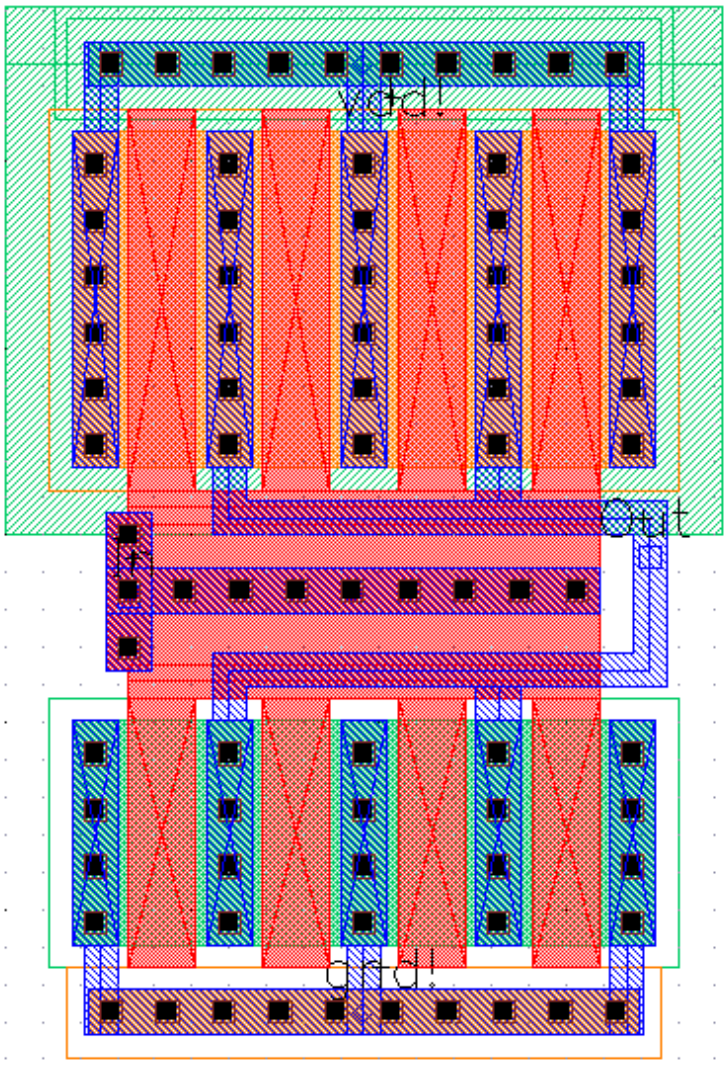

Figure 6: Buffer BUFF_2.

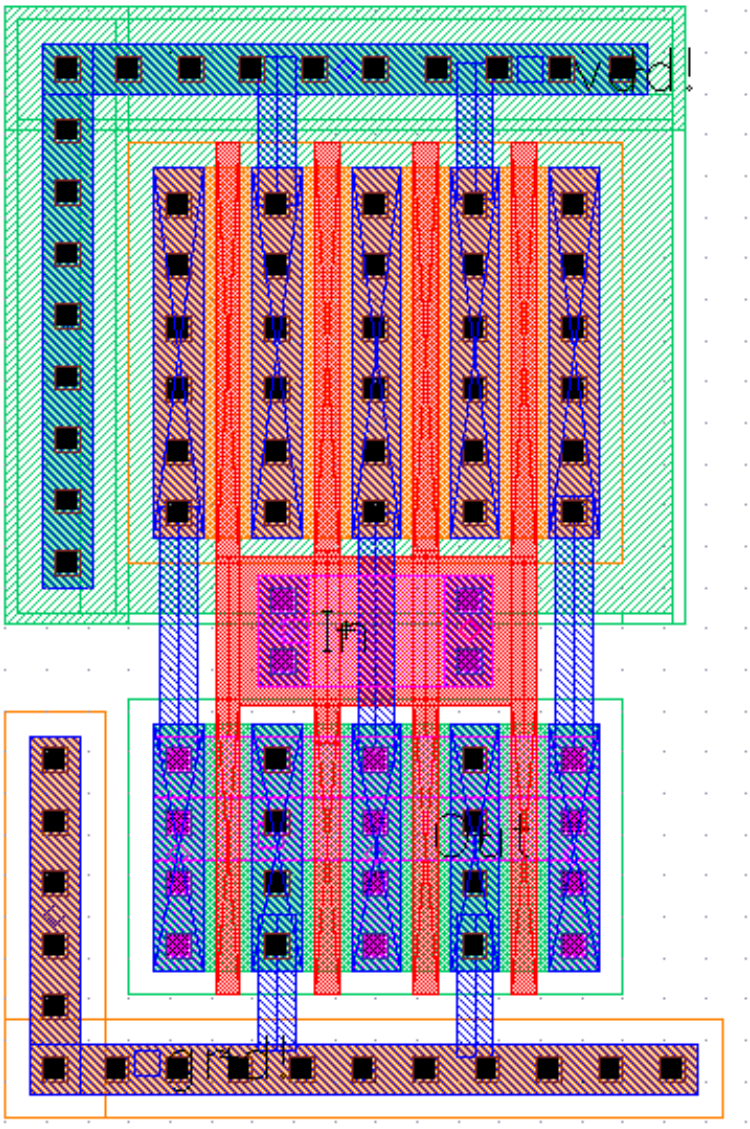

Figure 7: Buffer BUFF_3.

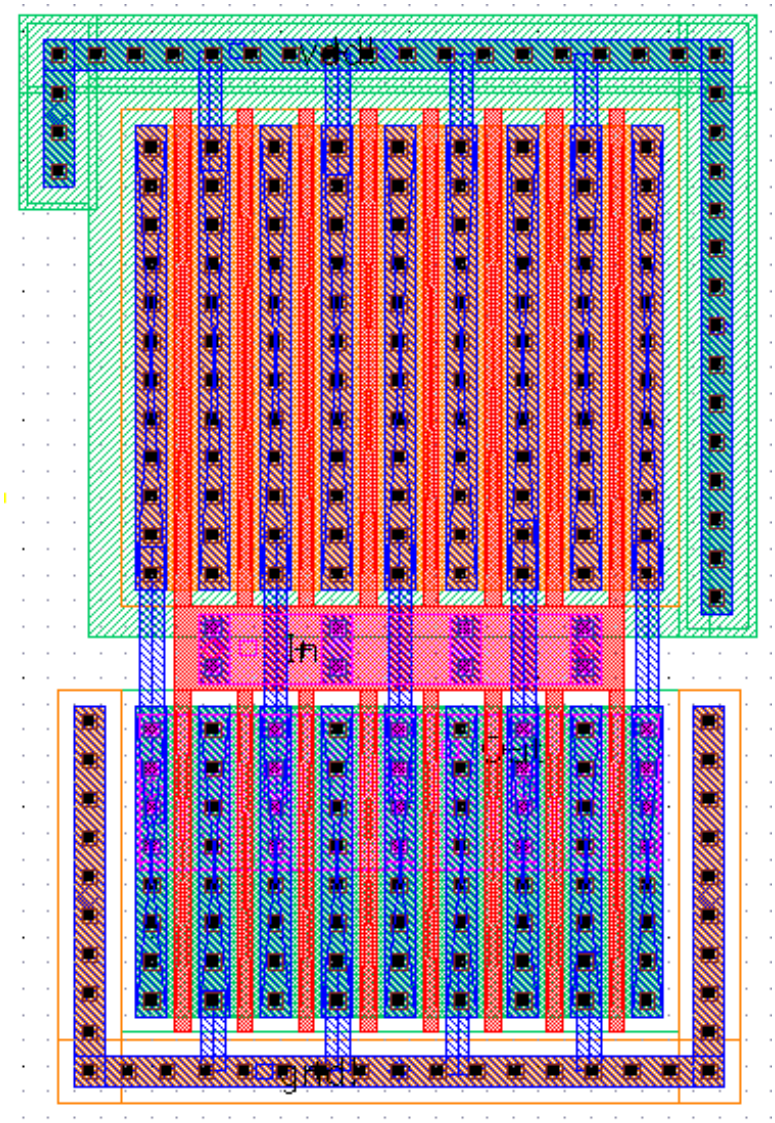

Figure 8: Buffer BUFF_4.

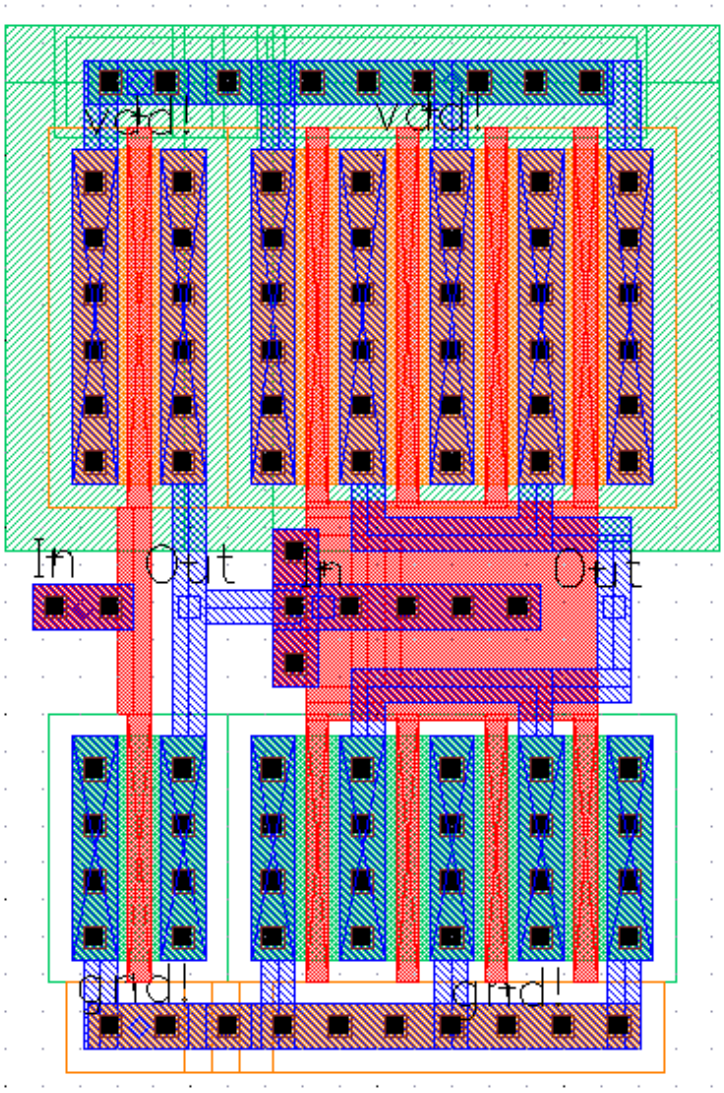

Figure 9: Buffer BUFF.

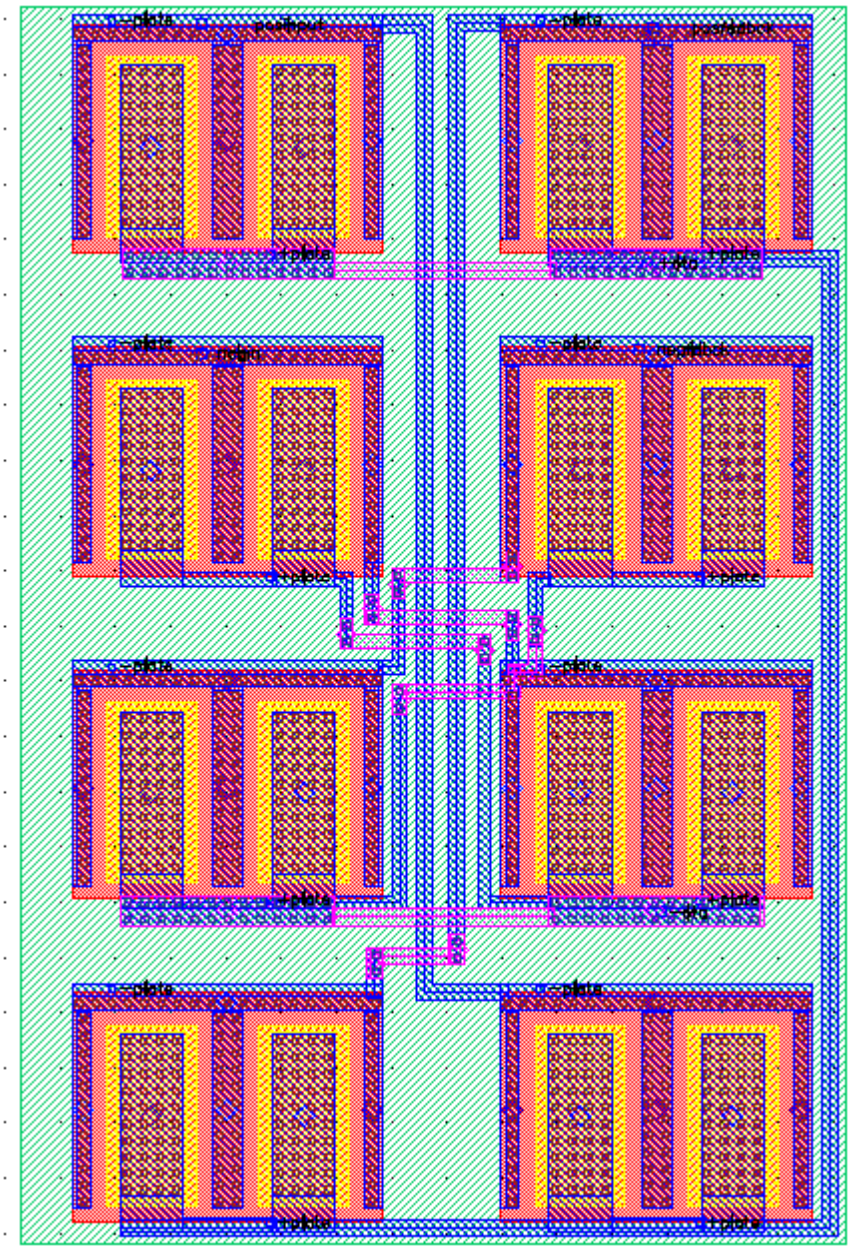

Figure 10: Common-centroid Capacitor Array.

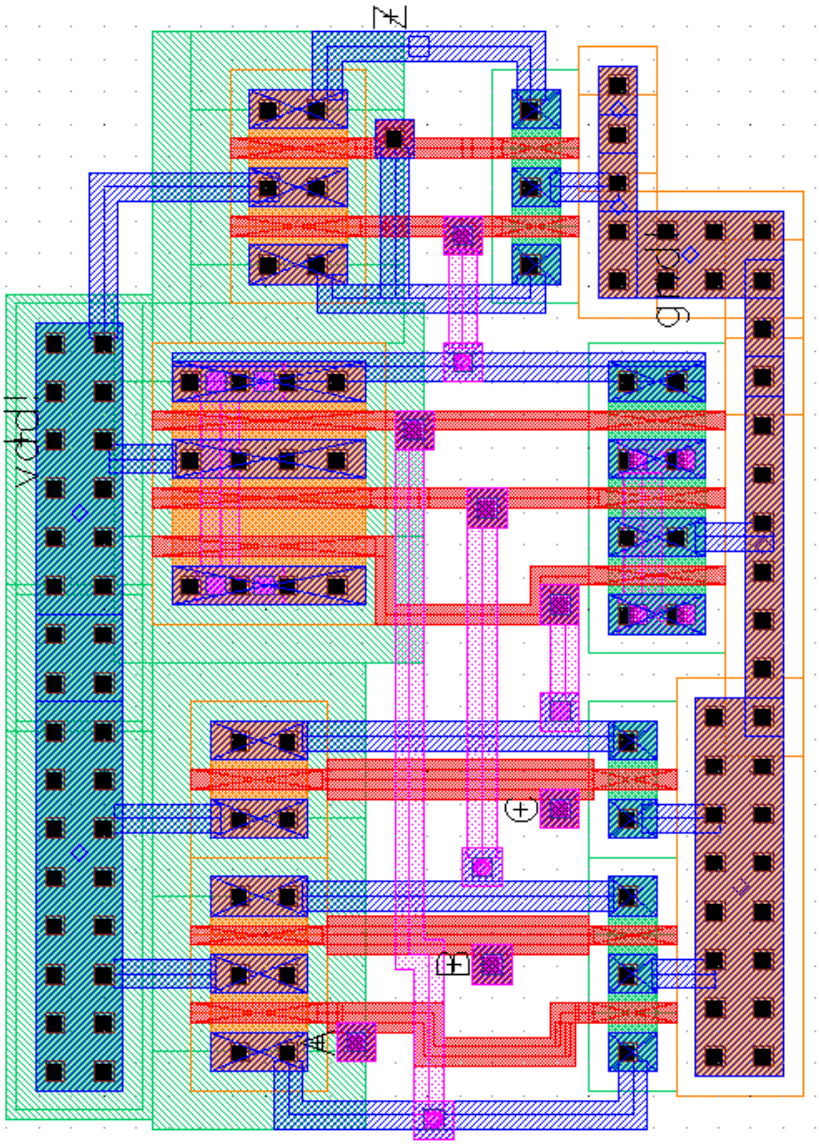

Figure 11: Carry Bit.

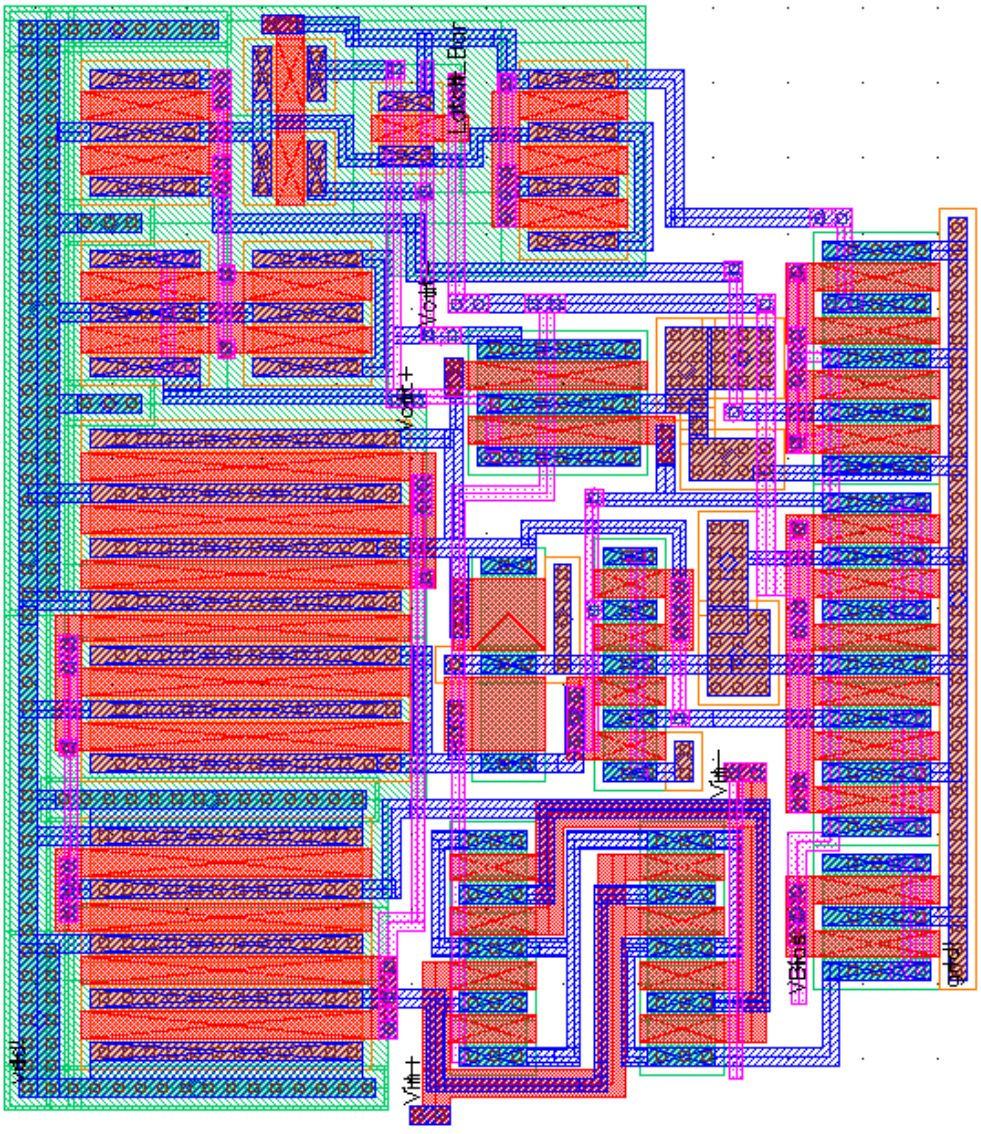

Figure 12: Clocked Comparator.

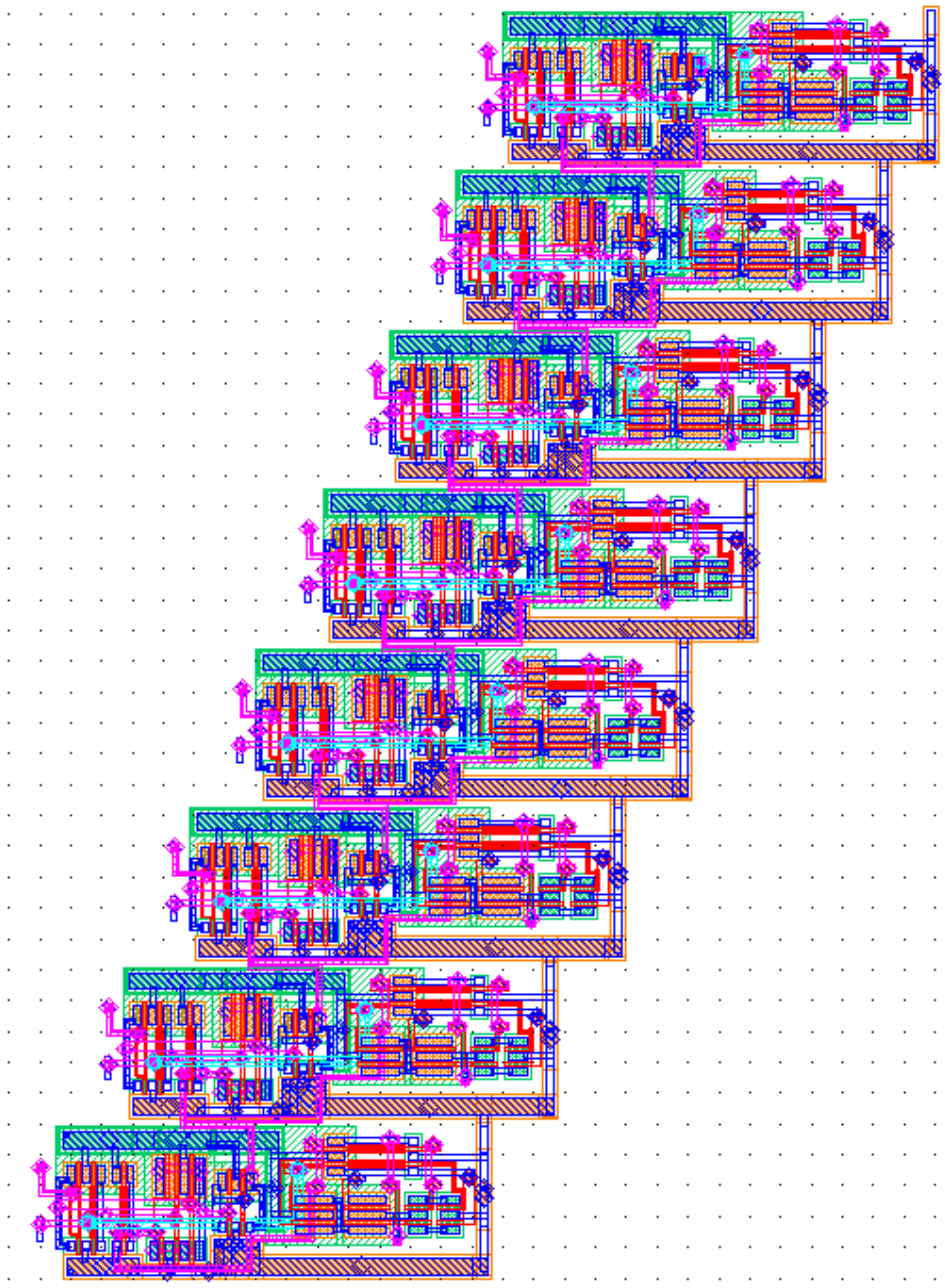

Figure 13: Correction Logic.

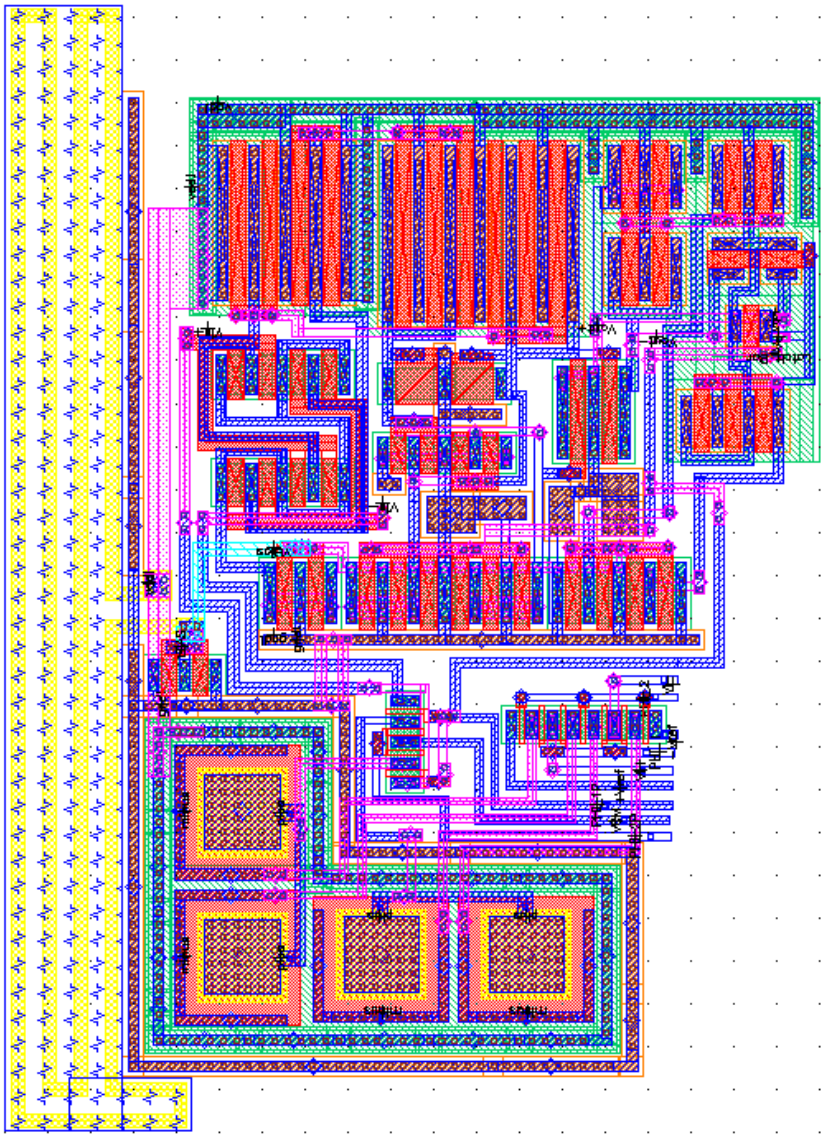

Figure 14: Last Stage Differential Comparator.

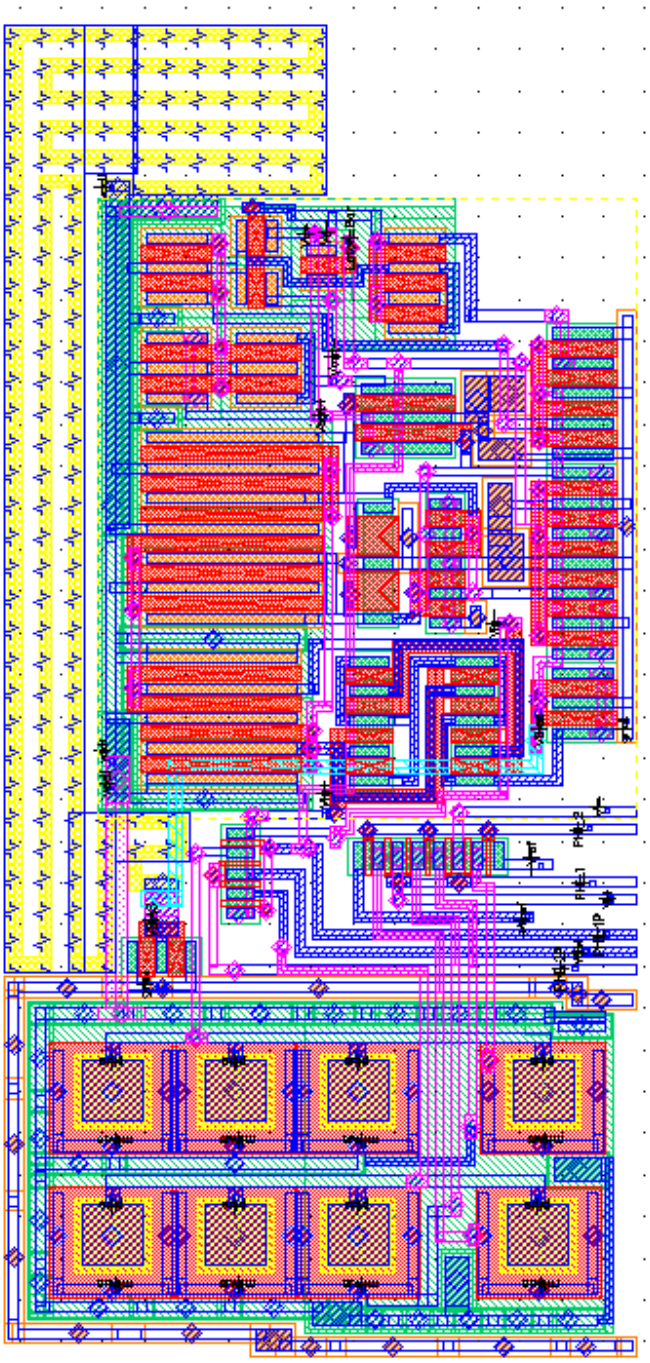

Figure 15: Differential Comparator.

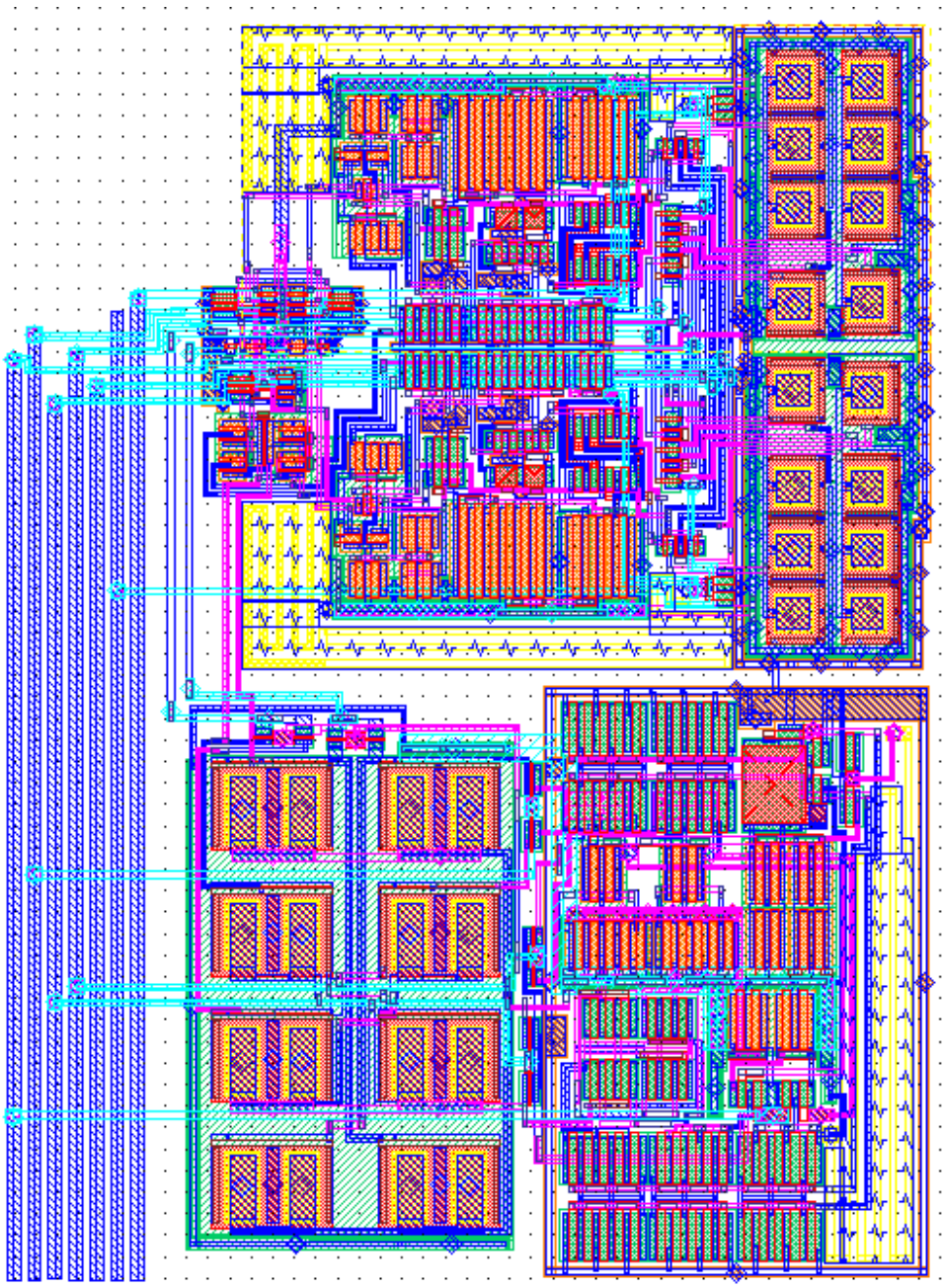

Figure 16: Even Stage.

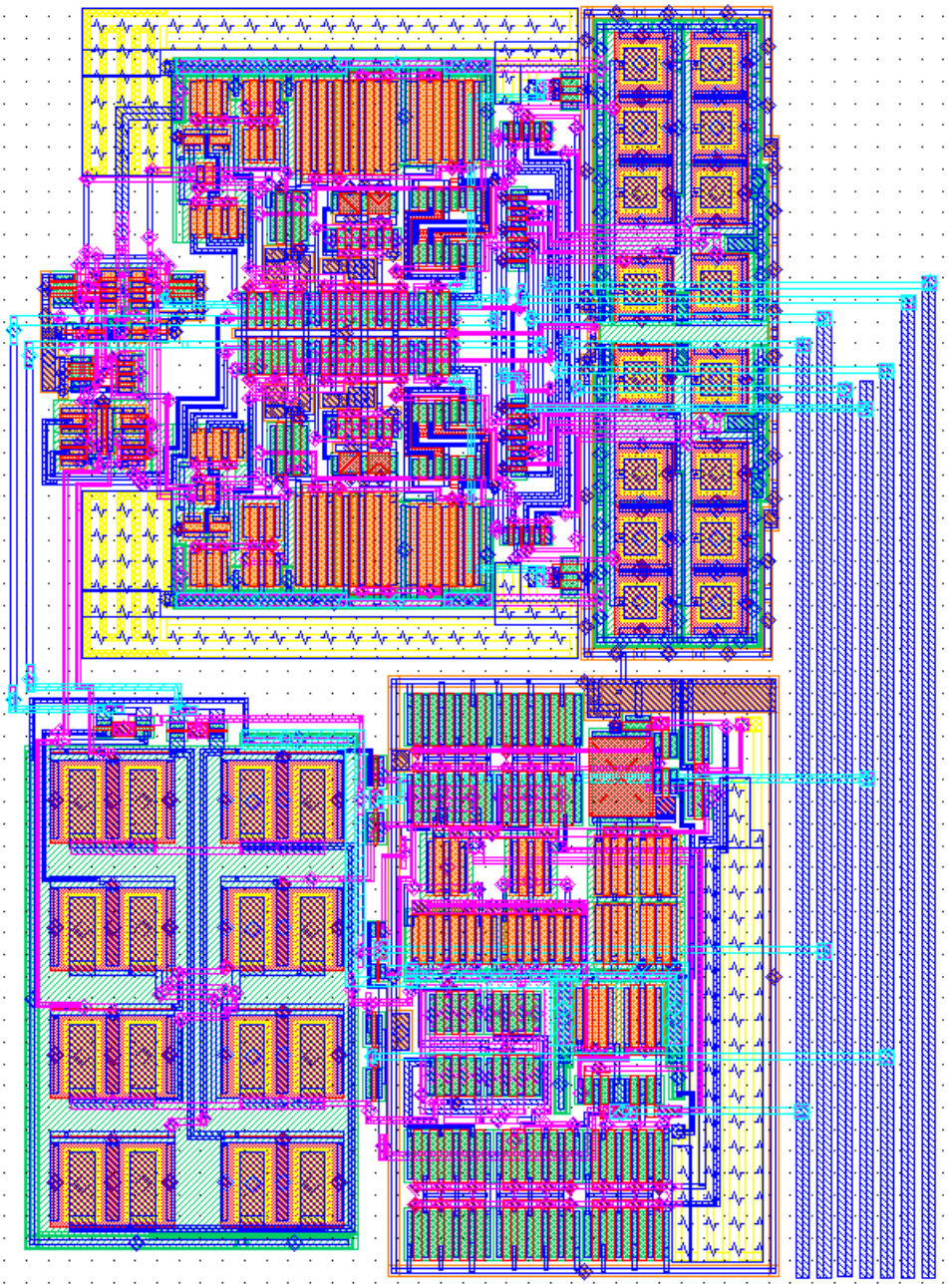

Figure 17: Odd Stage.

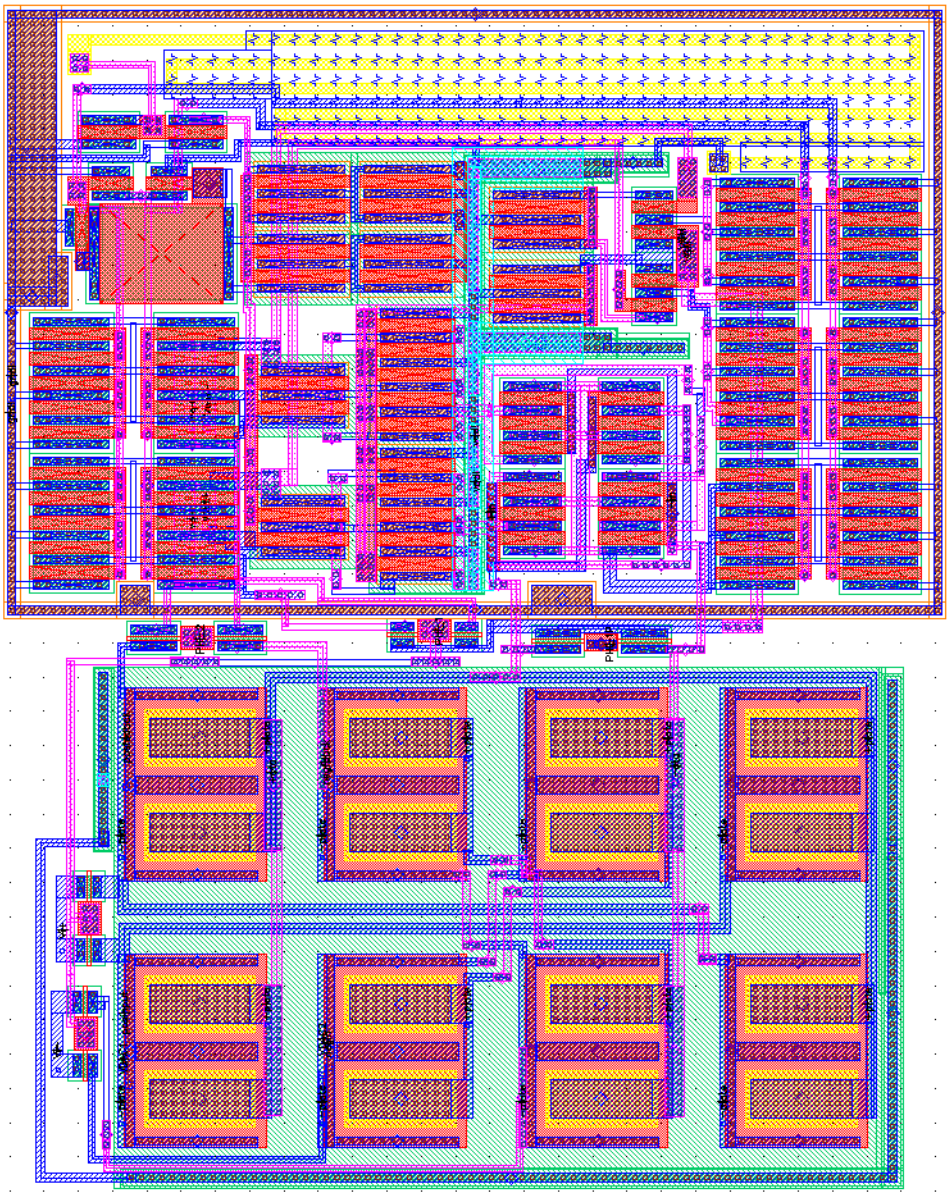

Figure 18: Gainstage.

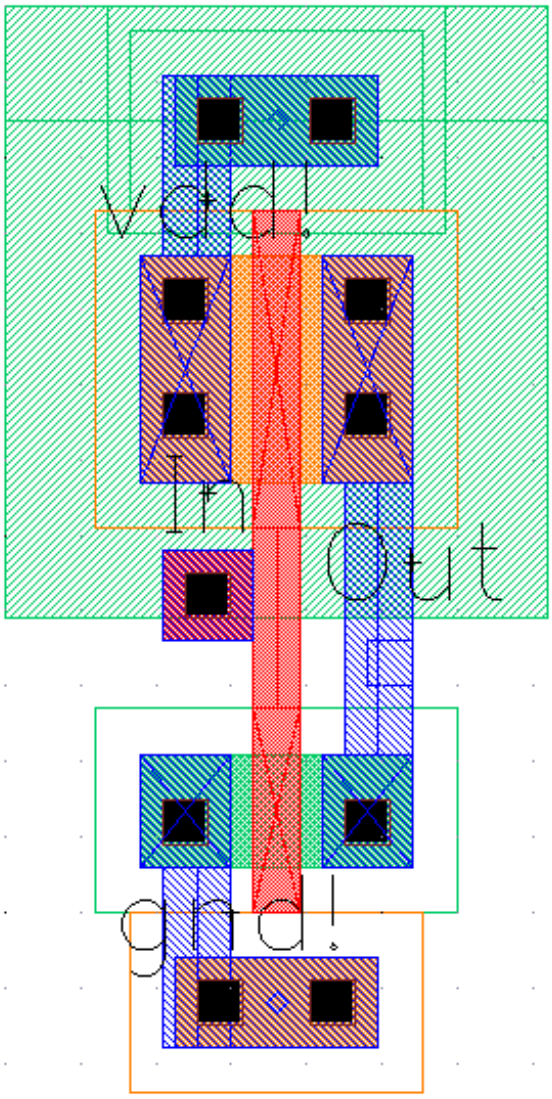

Figure 19: Basic Inverter.

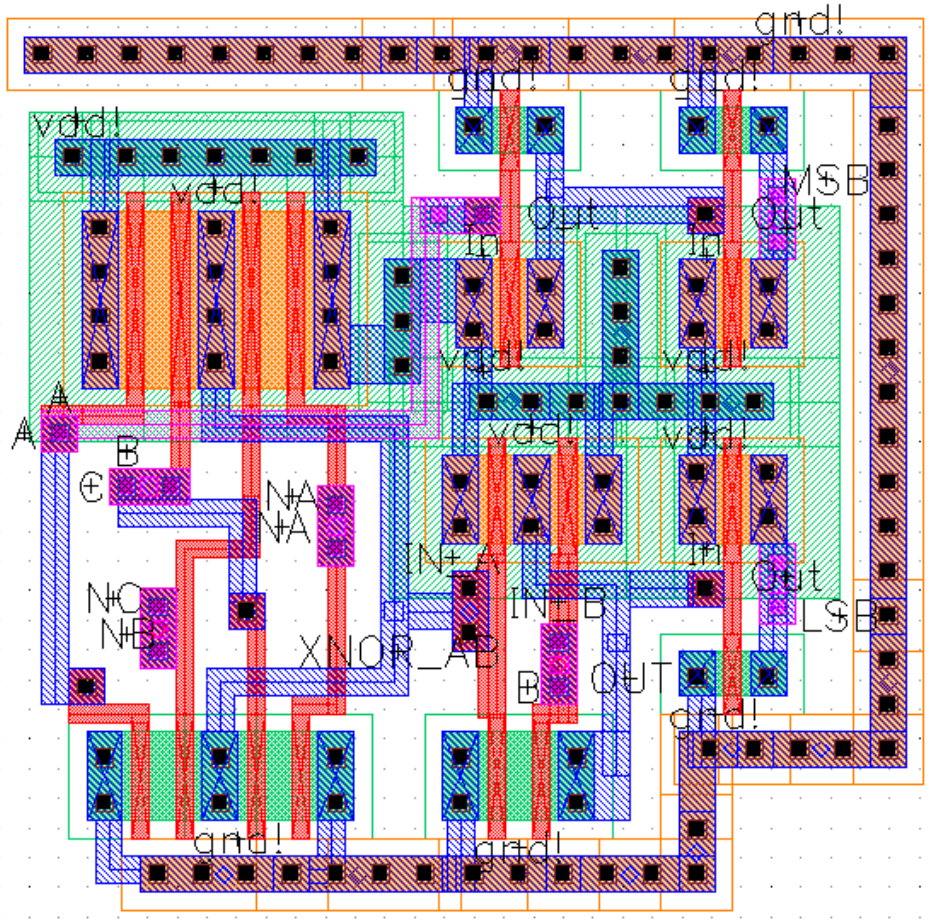

Figure 20: Last Stage ADC.

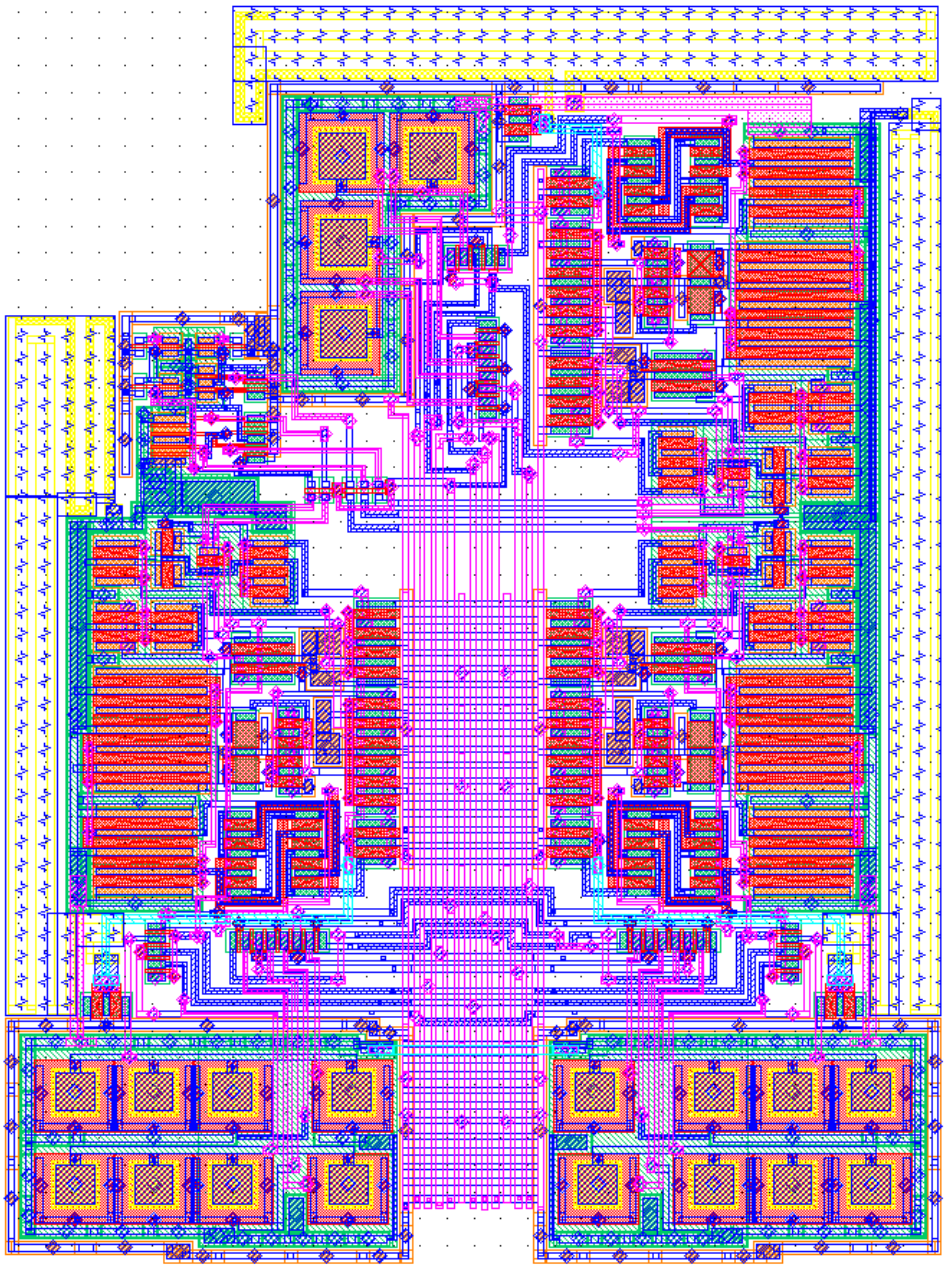

Figure 21: Last Stage.

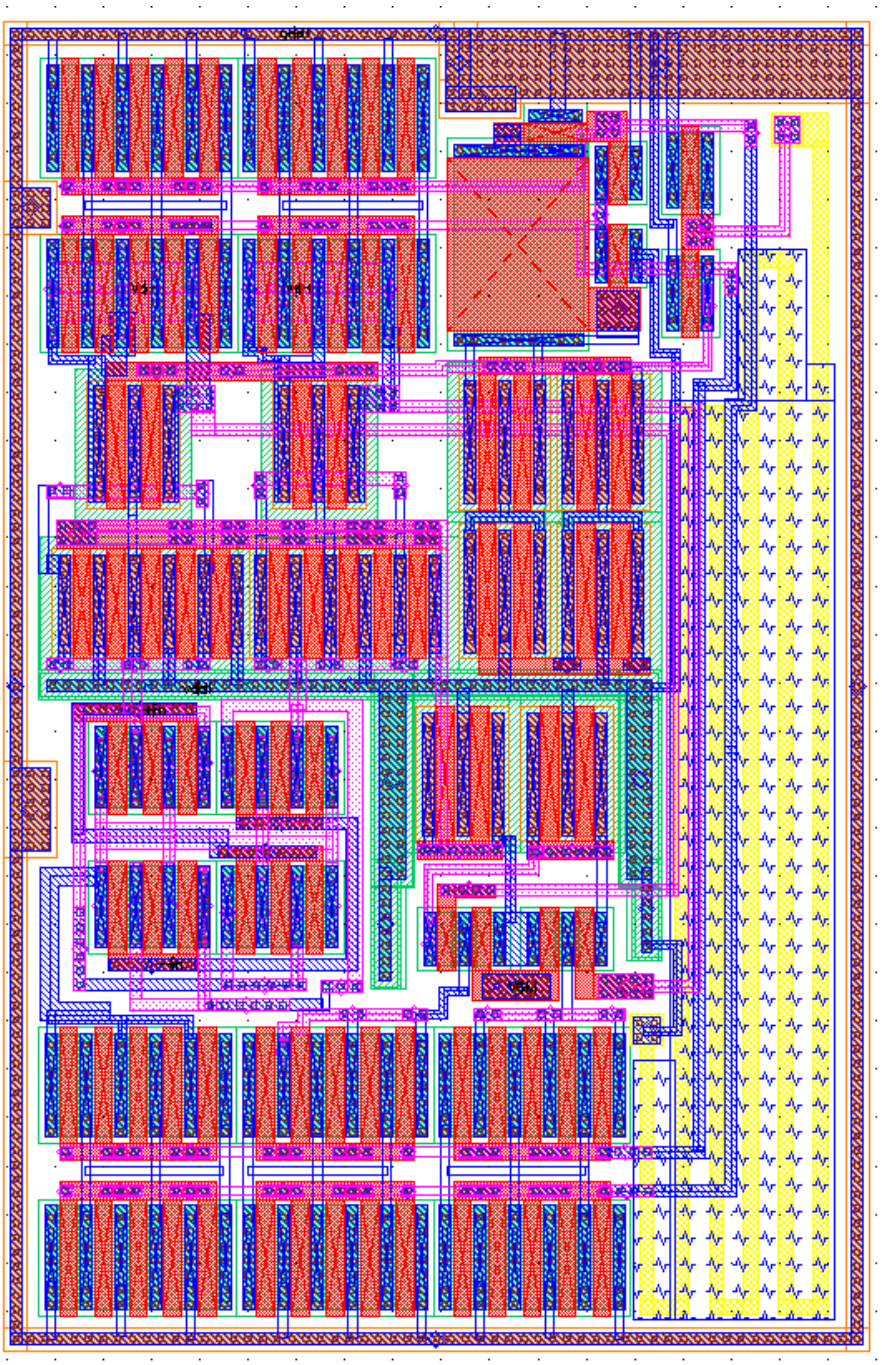

Figure 22: Operational Transconductance Amplifier.

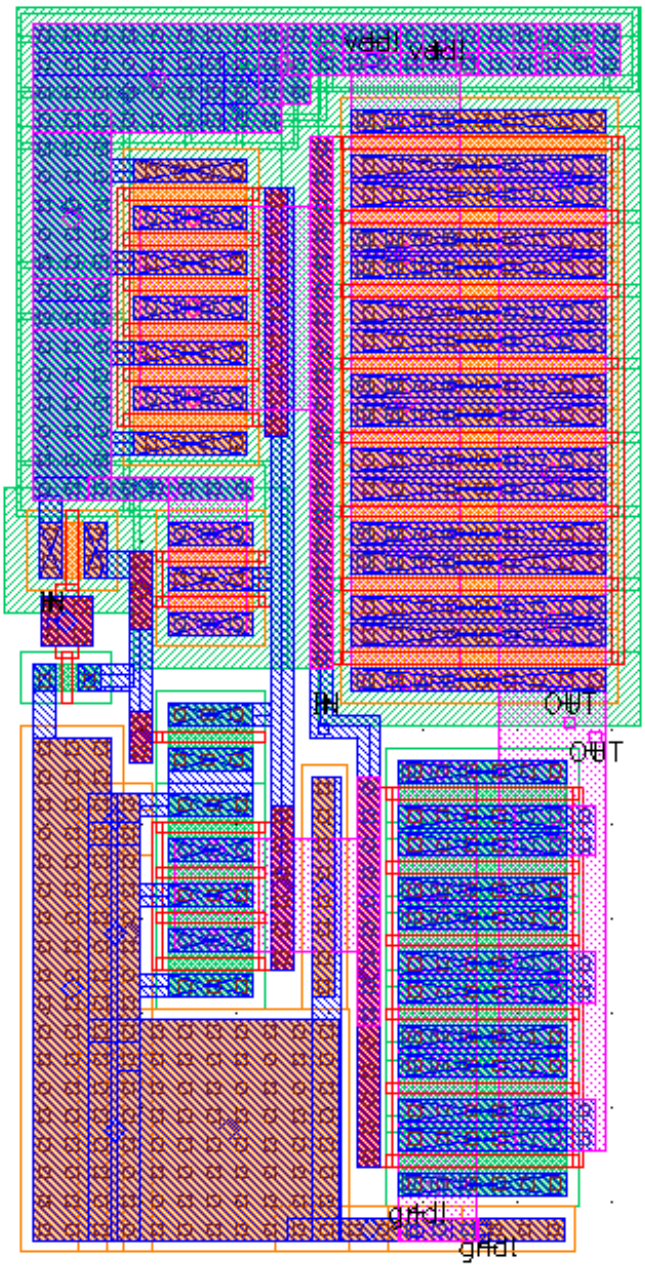

Figure 23: Output Driver.

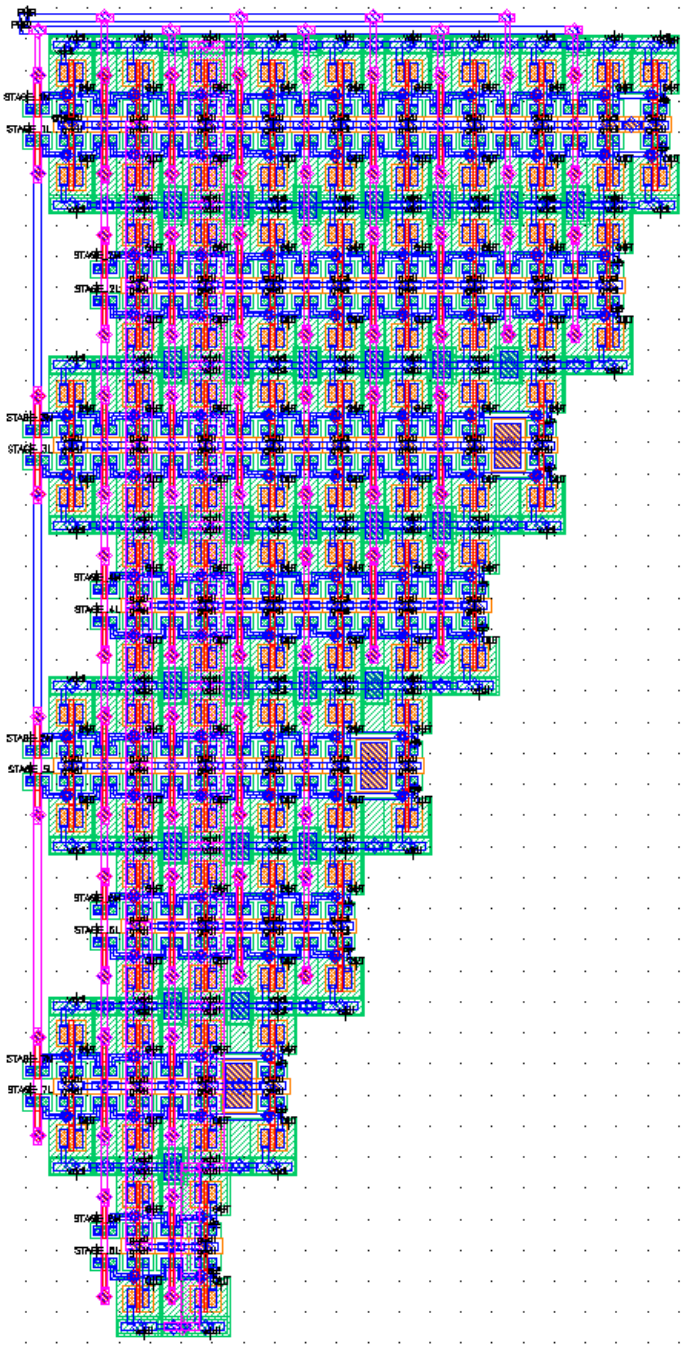

Figure 24: Shift Register.

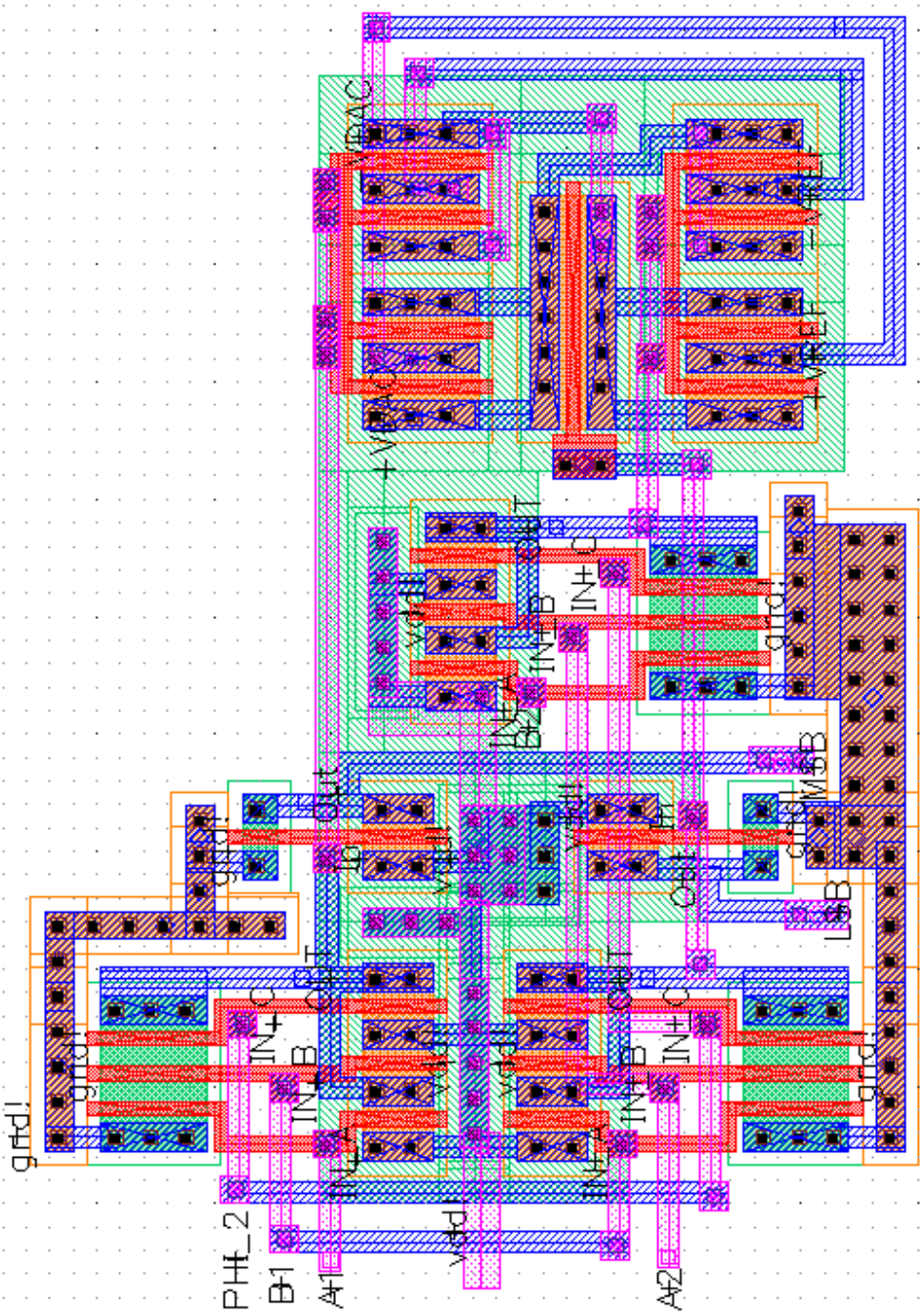

Figure 25: Sub-DAC.

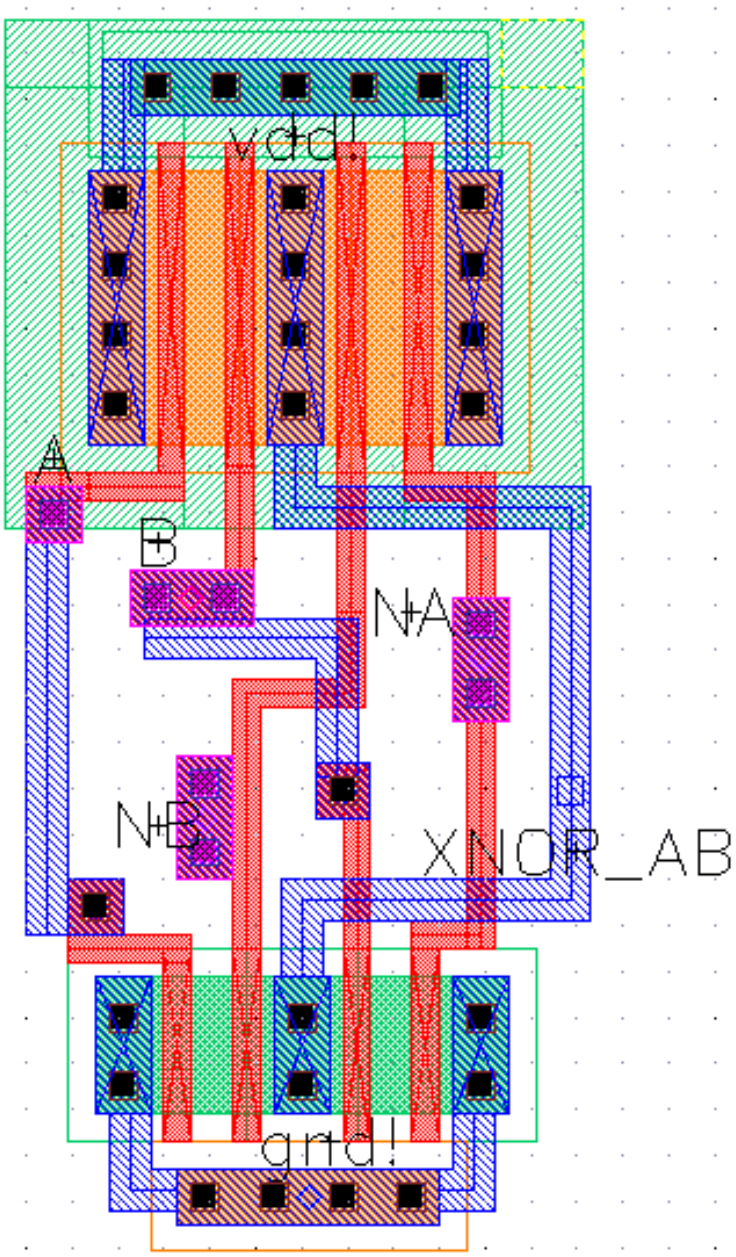

Figure 26: XNOR.

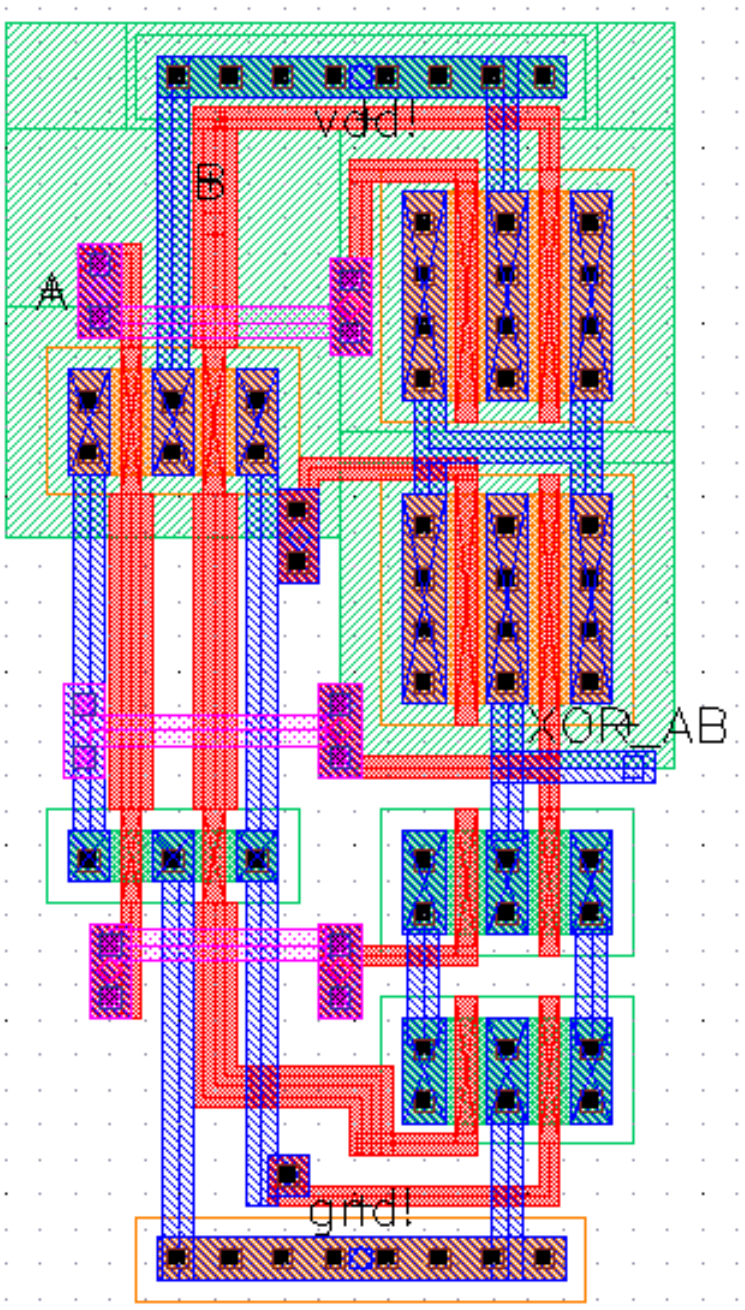

Figure 27: XOR.

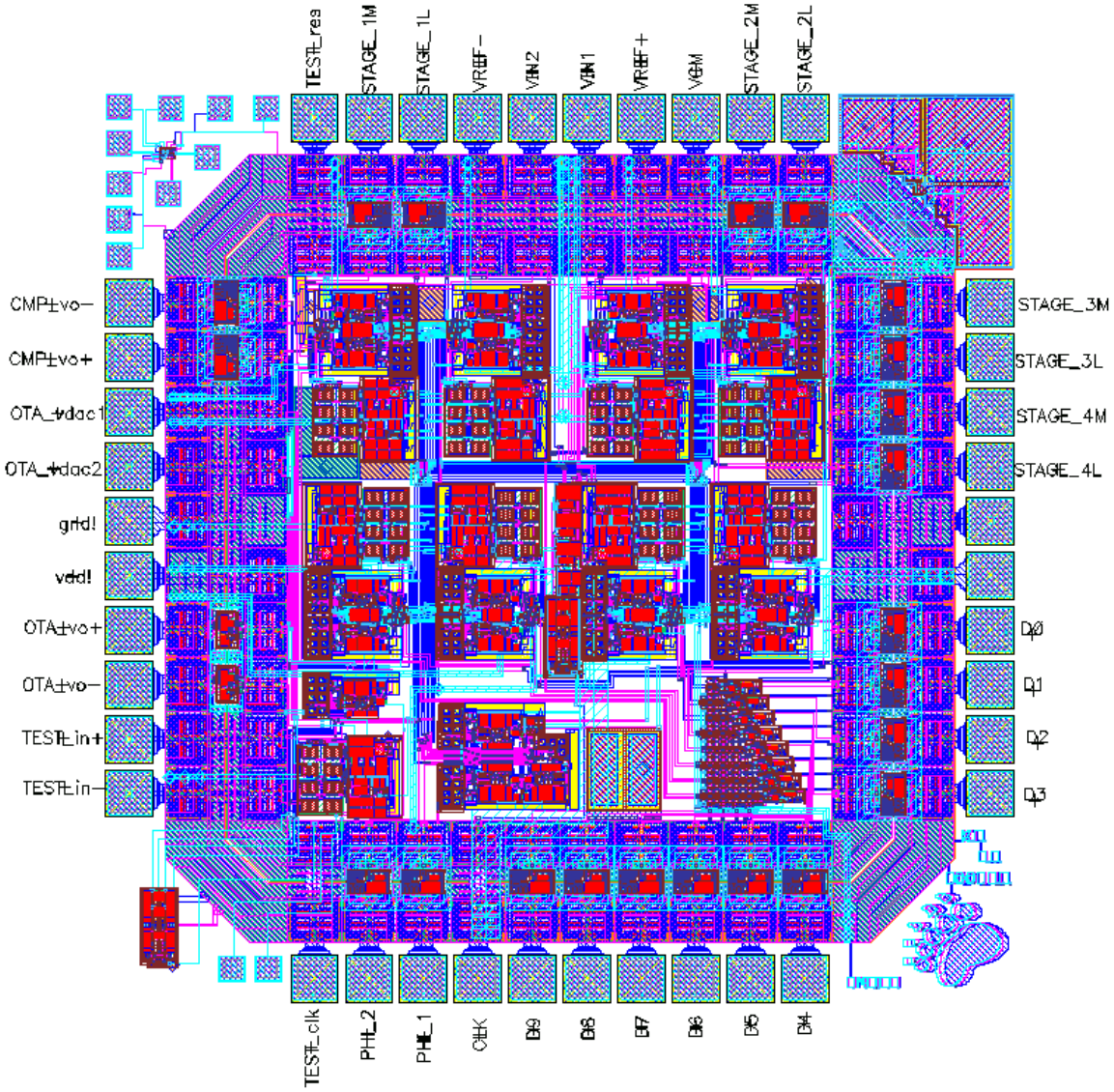

Figure 28: Final Chip Layout.