‘UMAINE ECE’ Morse Code ROM and Transmitter at ISM Band Frequency

Jamie E. Reinhold

December 15, 2011

Abstract

The design, simulation and layout of a ‘UMAINE ECE’ Morse code Read Only Memory and transmitter are described. The chip uses a band-gap reference circuit to convert a voltage stored onto a capacitor, to a DC power supply that is insensitive to temperature. The band-gap reference powers a variety of clocks used in the timing for 32x4-bit ROM and 32-bit multiplexer; all based from a voltage-controlled oscillator. The output of the ROM and multiplexer is the Morse code representation of UMAINE ECE, which is transmitted by a 433MHz sinusoidal oscillator and off-chip antennae. Logic 1 is represented by oscillation and logic 0 is no oscillation. Simulations show less than $\pm$10mV variation around 1.185V in the band-gap reference output from -50°C to 125°C with a charge on the capacitor ranging from 1.7V to 2.6V. The output of the overall circuit is a 325mV peak-to-peak sinusoid that oscillates at 433MHz (ISM-band frequency), where each character in the Morse code has a 50ms pulse width. Test and verification procedures are outlined and described.

Contents

1 Introduction

This report describes the design, test, and analysis of a 'UMAINE ECE' Morse code Read Only Memory (ROM) and transmitter. The circuit consists of five major stages. The first stage is a band-gap reference that is powered from a charged capacitor. It is used as the temperature insensitive power supply for the rest of the circuitry. The second stage is the clocks used for the timing of accessing the Read Only Memory and the clocks for the select lines of the 32-bit multiplexer, which are the third and forth stages respectively. The output of the ROM is used as the control bit for a 433MHz oscillator, which will oscillate with every Logic 1. An off-chip antenna is used to transmit the signal to a base station. The 433MHz oscillation frequency was selected so that the transmission will be in the ISM-band of the frequency spectrum.

Section 2 describes the design of the circuitry including schematics, Section 3 illustrates the layout of the circuitry and discusses layout rules, Section 4 discusses the circuit simulations, and Section 5 describes how the chip will be tested. Section 6 includes suggestions for future work and a biography of the author. Designs, layouts, and simulations are all done using Cadence software version 1.9.

2 Circuit Design and Analysis

The overall circuit is represented as a block diagram in Figure 1 below. The band-gap reference will draw power from an off-chip capacitor. The design and analysis of a band-gap reference, clocks, read only memory, multiplexer, and 433MHz oscillator are discussed in sections 2.1, 2.2, 2.3, 2.4, and 2.5 respectively.

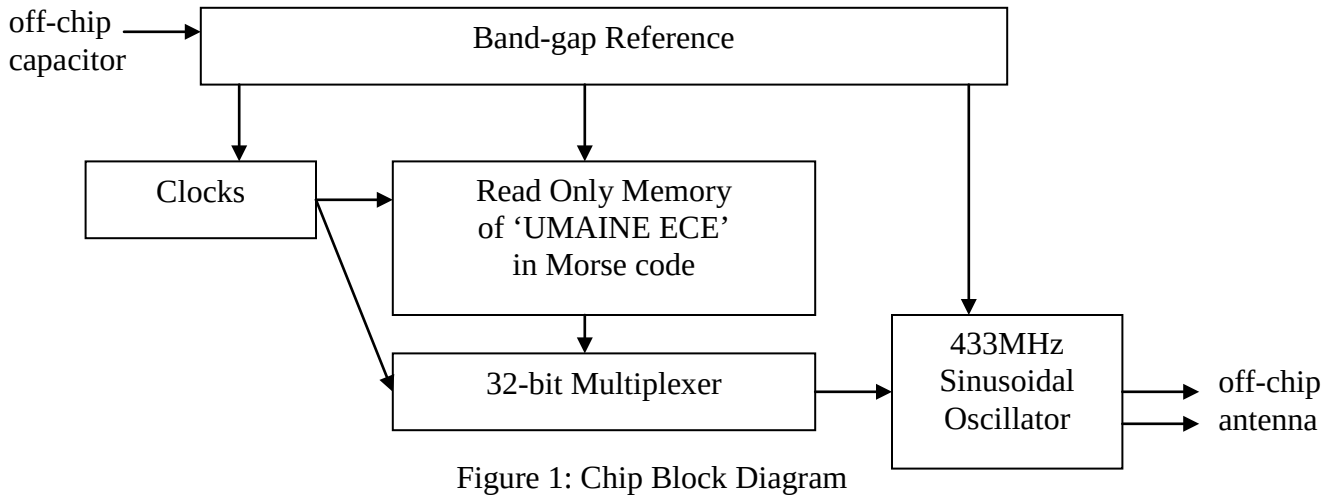

Figure 1: Chip Block Diagram

The output of the 32-bit Multiplexer will be a control sequence for the 433MHz oscillator, where the oscillator will turn on for every Logic 1 that is passed. An example of the output of the MUX is shown in Figure 2, where each pulse will last 50ms, and correspond to the shortest beep in a Morse code sequence. The Morse code that is transmitted through an off-chip antenna will spell 'UMAINE ECE'. The antenna was previously designed and has an impedance of 74Ω.

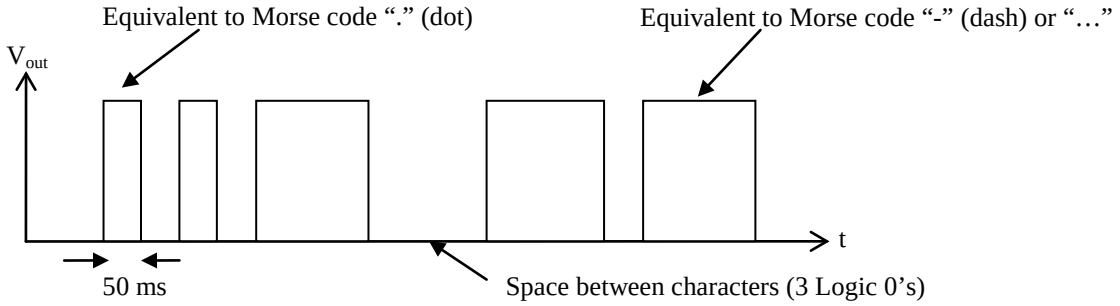

Figure 2: Example output of the multiplexer, a digital representation of a Morse code sequence

2.1 Design of Band-Gap Reference

In order to generate a DC power supply that is independent of temperature and also independent of supply voltage over a certain range, a band gap reference circuit was used, shown in Figure 3 below. This circuit does not use the band gap to create a voltage reference, but the output voltage is very close to the band gap of Silicon (≈1.24V) [1].

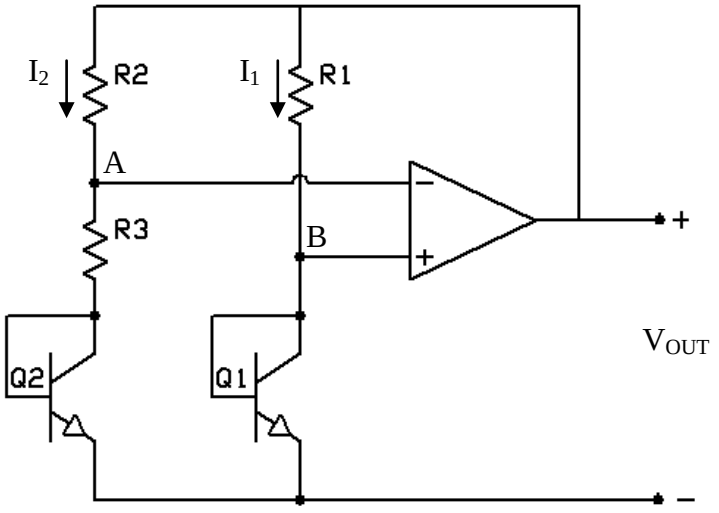

Figure 3: Schematic of a band-gap reference circuit

An operational amplifier is used to drive the feedback network, which must be able to source a specific amount of current. It can be seen that the voltage at node A and node B will be approximately equal, and the current into the op-amp will be close to zero. By sizing the transistors and resistors appropriately, the output voltage can be determined by the following equation.

$$V_{OUT} = V_{BE2} + \left[1 + \frac{R_2}{R_3}\right] V_T \ln\left[\frac{R_2}{R_1}\frac{I_{S2}}{I_{S1}}\right] \quad (1)$$

V_{BE2} is the base to emitter voltage of Q_2, and I_{S1} and I_{S2} are the reverse saturation currents of Q_1 and Q_2 respectively.

By changing the sizes and values of the components, the output voltage can be selected to vary at a constant slope with temperature, or stay relatively the same with change in temperature. The output voltage was selected to be 1.2V and stay constant for temperatures ranging from -50°C to 125°C. A schematic of the band gap reference circuit is shown in Figure 4, with the calculated resistor values and diode sizes. Due to process constraints, calculated resistance values were modified to fit the specifications. Havar diodes are used instead of diode-connected bipolar junction transistors.

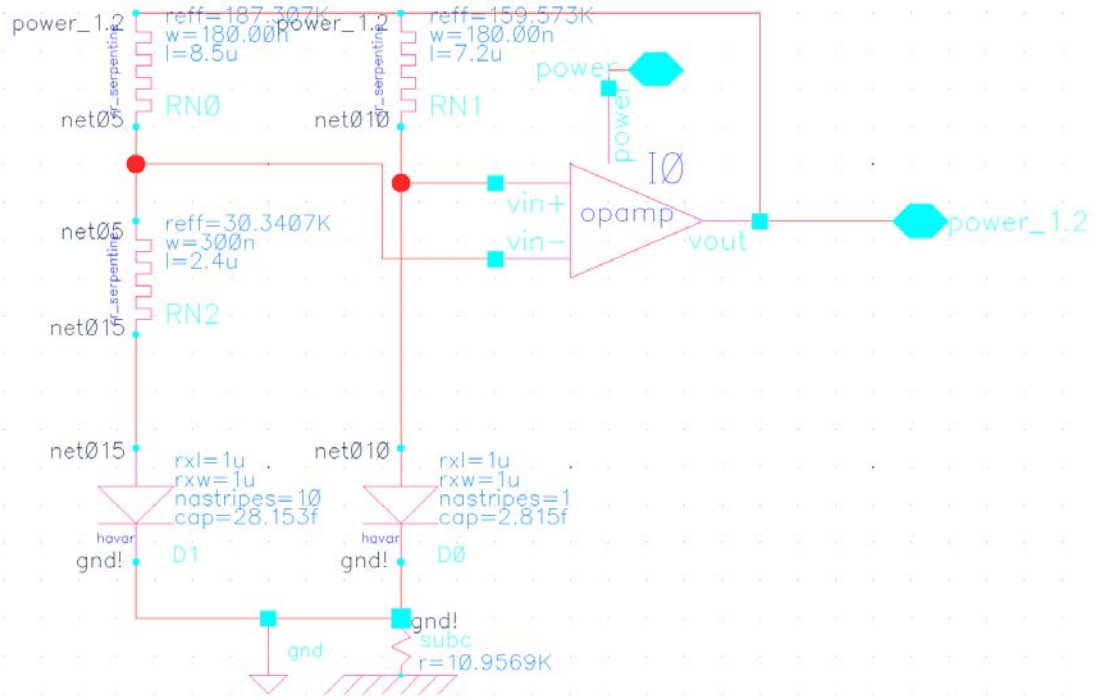

Figure 4: Schematic of band-gap reference circuit

The operational amplifier used in the band gap reference was designed to have a high open-loop gain, and high current drive capability. The differential inputs were selected to be PMOS devices so that the power supply rejection ratio of the positive rail will be approximately zero. A Miller capacitor was added between the differential pair and output stage of the op-amp so that the op-amp will remain stable for desired frequencies. An output stage was used to increase the current drive capability, since the 433 MHz oscillator will need a few milliamps to run. The output stage can source up to around 3 mA. Transistors sizes are shown on the schematic of the op-amp in Figure 5. In all following schematics, v_{dd} refers to the DC voltage supplied by the band-gap reference.

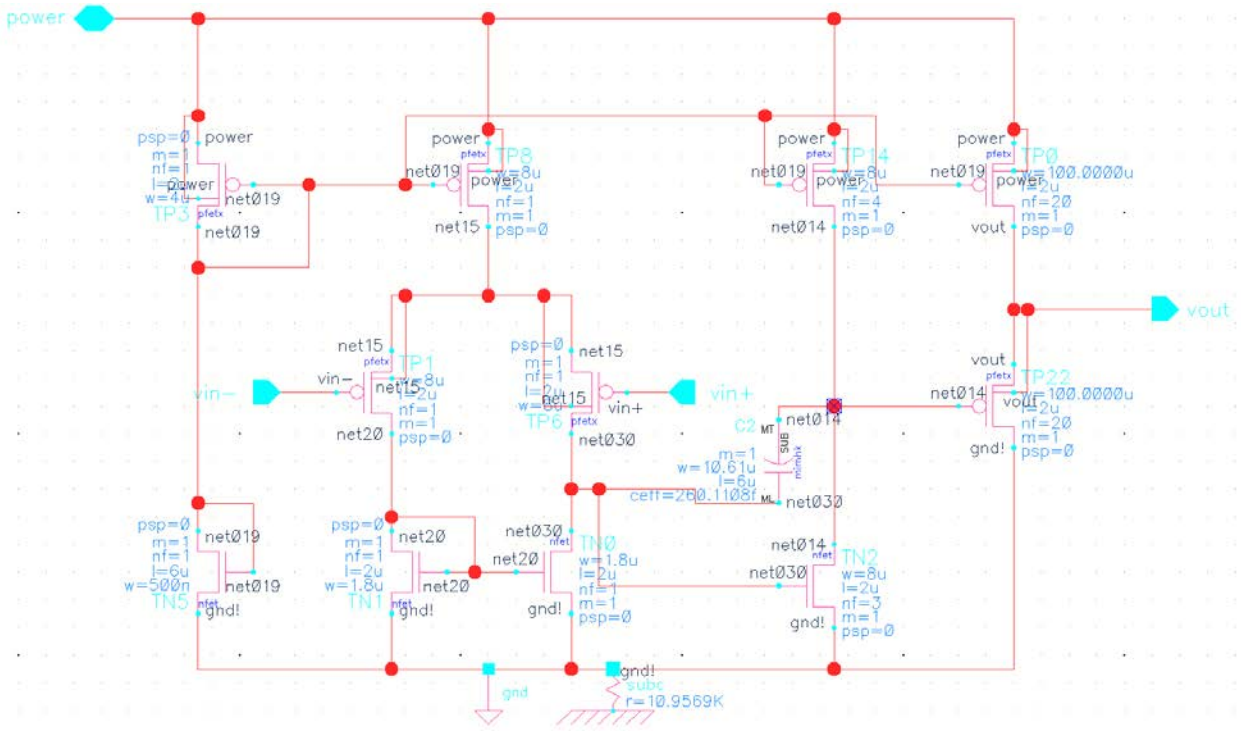

Figure 5: Schematic of operational amplifier, where l = transistor length and w = transistor width

2.2 Design of Clocks

To control the digital circuitry needed to produce a Morse code sequence, a variety of clocks were used. A voltage-controlled oscillator was designed as the main clock of the circuit, and all other clocks are based off of it. If there are any variations in the oscillation frequency of the VCO due to changes in temperature or process variations, the circuit will still run as designed. Design of the VCO is discussed in Section 2.2.1, the design of a 5-bit clock for the multiplexer select lines is discussed in Section 2.2.2, and the design of a non-overlapping clock to access the ROM is discussed in Section 2.2.3.

2.2.1 Design of Voltage-Controlled Oscillator

The fastest clock in the circuit has a period of 50ms. In order to generate this square wave, a number of options were looked at. Due to the low frequency of the clock, it was determined that a voltage-controlled oscillator would be the best option. If a ring oscillator was used, it would need a very large amount of stages and would take up a large amount of chip space. The VCO was constructed using a string of delay stages. One of the delay stages is shown in Figure 6, where P and N are tied to the gates of PMOS and NMOS transistors in a current source, respectively.

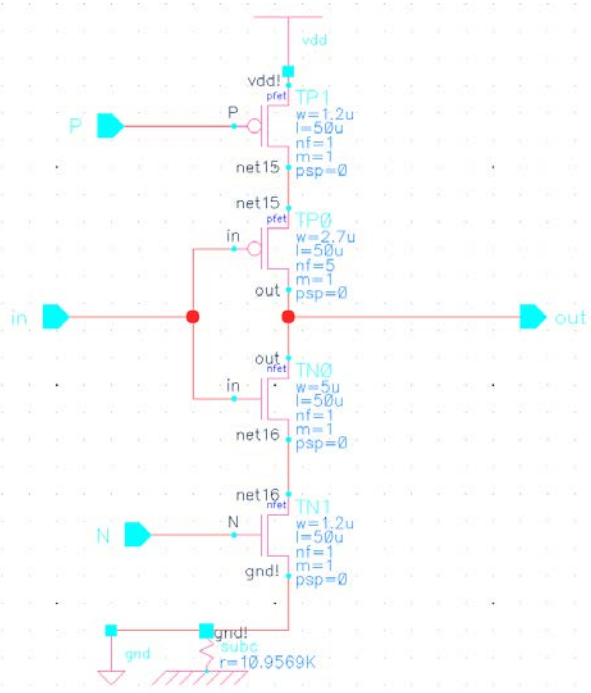

Figure 6: Schematic of one stage in a voltage-controlled oscillator

The delay time of each stage is determined from the R-C time constant. To increase the capacitance of each stage, transistors with a large length were selected. The number of stages needed, N, was determined by measuring the delay of one stage, $\tau_{single\ stage}$, where the total delay is found by

$$\tau_{total} = N * \tau_{single\ stage} \quad (2)$$

Since the size of the transistors needed for each stage were so large, it was decided that T flip-flops, or "toggle" flip-flops (discussed in Section 2.2.2) will be used to divide the frequency of the oscillator by 2^N where N is the number of T flip-flops in the chain. T flip-flops take up less space in the layout than additional stages of the VCO. Four flip flops will be attached to the output of the VCO and are used to reduce the frequency of the VCO to $1/16^{th}$ of its initial output (Figure 7).

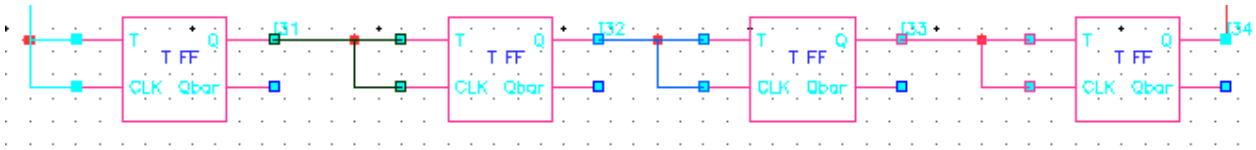

Figure 7: Schematic of T flip-flop chain used to decrease the VCO frequency

A current source is used to drive the VCO (shown in Figure 8). The output of the VCO is tied back to the input of the first stage, so that the VCO will continually oscillate and produce a square wave with a period of 3.125ms.

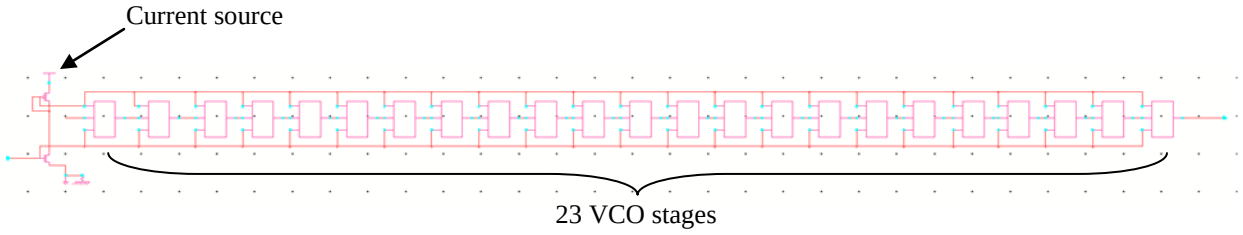

Figure 8: Schematic of the voltage controlled oscillator

Since the desired oscillation frequency will always be the same, a resistor ladder tied to v_{dd} is used to set a specific control voltage. The resistors are dependent on temperature but since both have the same temperature coefficient, the supplied control voltage will not vary with temperature.

A series of pulses was noticed on the rising edge of the VCO output (shown in Simulations Section 4.2). A digital buffer was designed to lower the rise and fall time of the square wave and to make sure the output is from rail to rail (0V to 1.2V). The digital buffer is simply a string of inverters, each sized 3 times larger than the previous. This will better shape the clock signal. A schematic of the buffer is shown in Figure 9.

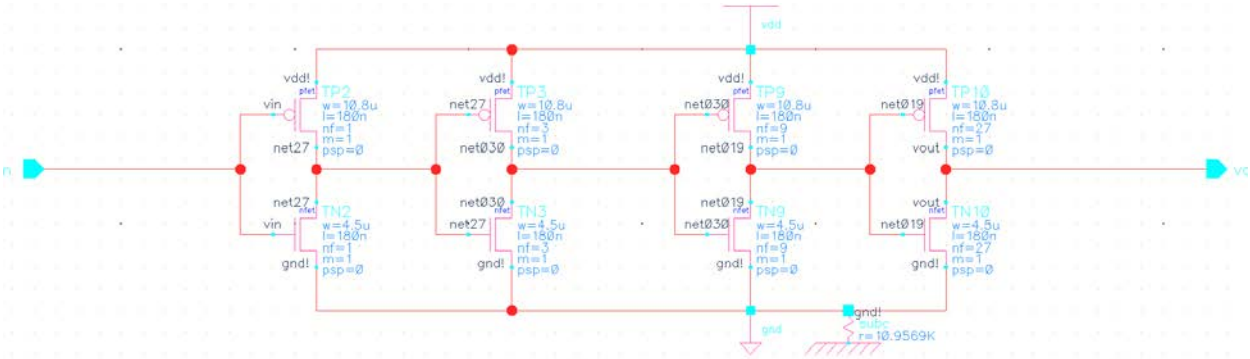

Figure 9: Schematic of a digital buffer

The VCO and buffer will drive 4 T flip-flops, producing a square wave output signal that ranges from 0V to 1.2V and has a period of 50ms. The initial timing schematic is shown in Figure 10.

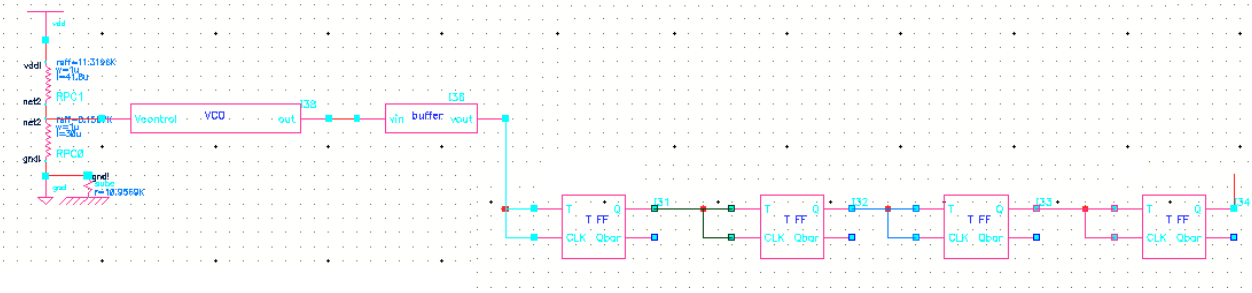

Figure 10: Initial timing schematic consisting of VCO, digital buffer, and series of T flip-flops

2.2.2 Design of 5-bit Clock

In order to drive the select lines of the 32-bit MUX, a 5-bit clock is needed. The clock is implemented by using a series of T flip-flops, or toggle flip flops. The schematic of a T flip-flop is shown in Figure 11. When the input and clock line are tied together, the output will be a square wave at ½ the frequency of the input. In this fashion, a series of 5 T flip-flops will produce 5 outputs, each at half of the frequency of the previous (Figure 12). By inverting each output, a binary 5-bit clock starting at 00001 is generated [2]. (See Section 4.2 for simulation results.)

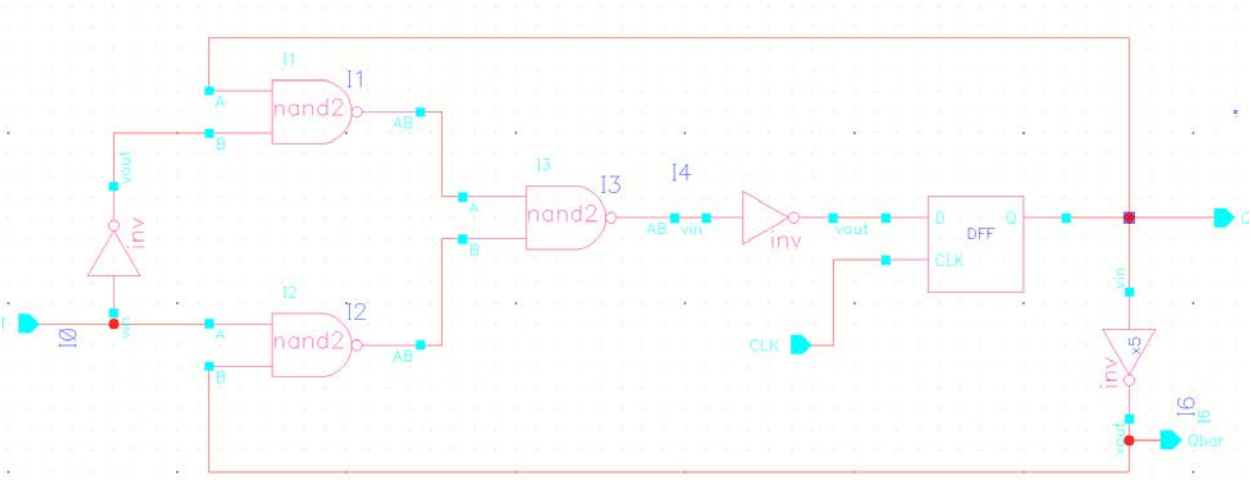

Figure 11: Schematic of T flip-flop

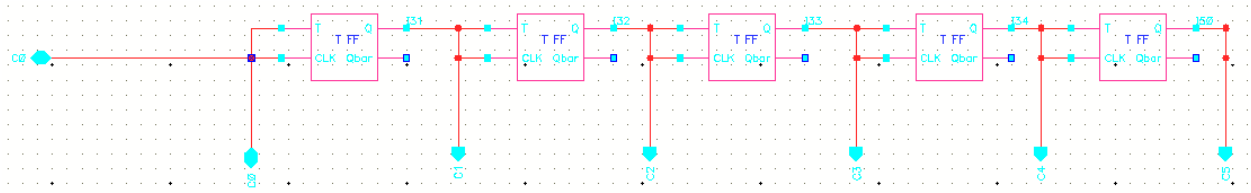

Figure 12: Schematic of T flip-flop chain used to generate 5-bit clock

The logic gates used to create the T flip-flop were designed using transistor sizes based off of a minimum sized inverter. Schematics of the inverter and 2-input NAND gates are shown in Figure 13. A D flip-flop was designed using transmission gates since these will draw less power than other logic gates. Schematics of the D flip-flop and transmission gates are shown in Figure 14. Inverters labeled “x5” are five times bigger than the minimum sized inverters shown in Figure 13. These were used to increase the drive capability of the flip-flop.

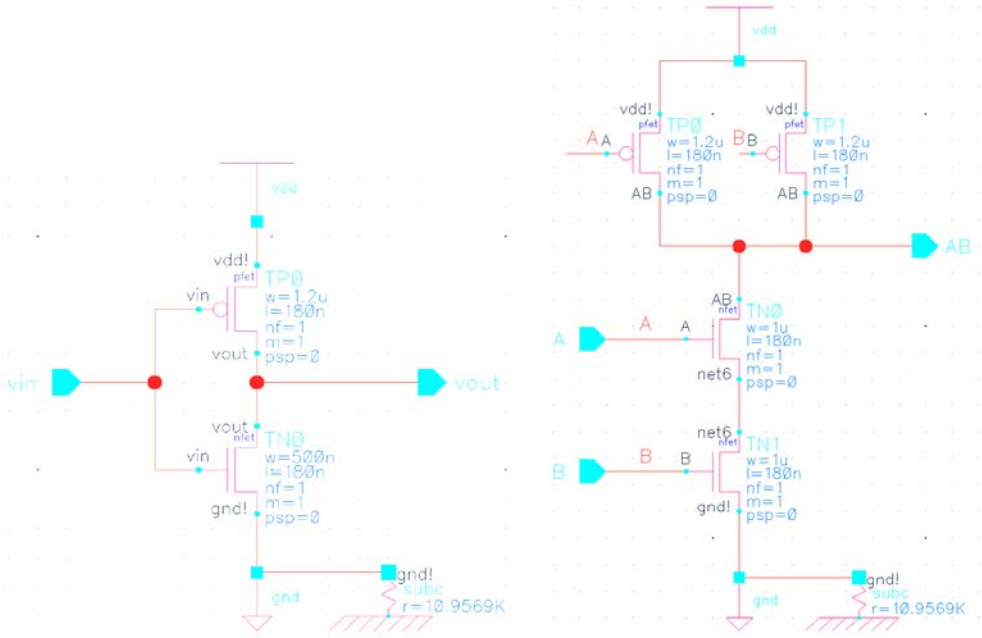

Figure 13: Schematic of minimum sized inverter (left) and 2-input NAND gate (right)

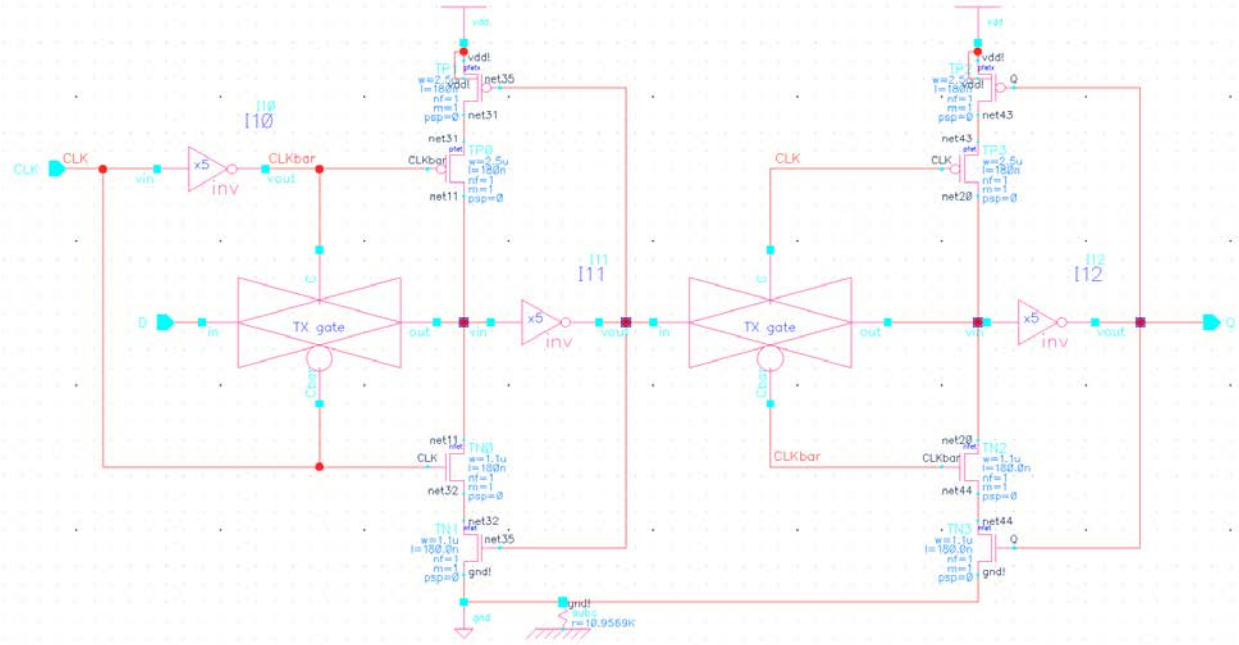

Figure 14a: Schematic of D flip-flop

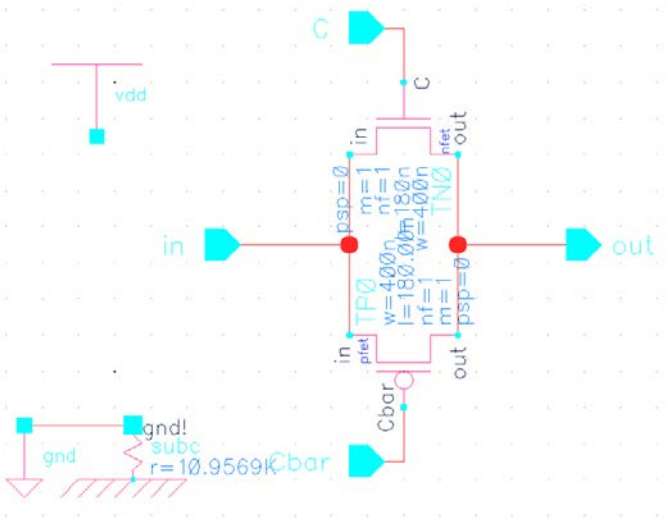

Figure 14b: Schematic of transmission gate, where v_{dd} and ground are shown for body contacts

2.2.3 Design of Non-overlapping Clock

To access the ROM array, a non-overlapping clock was needed. This will be used to drive each word line of the ROM separately. The non-overlapping clock was implemented using T flip-flops and a decoder made of 2-input NAND gates. A schematic and example output is shown in Figure 15 and Figure 16, respectively.

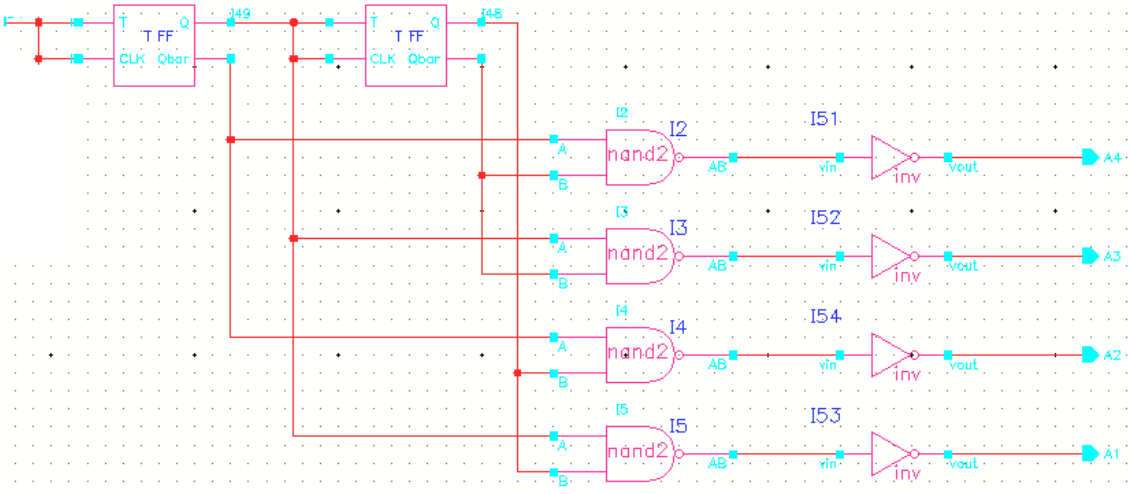

Figure 15: Schematic of non-overlapping clock including decoder

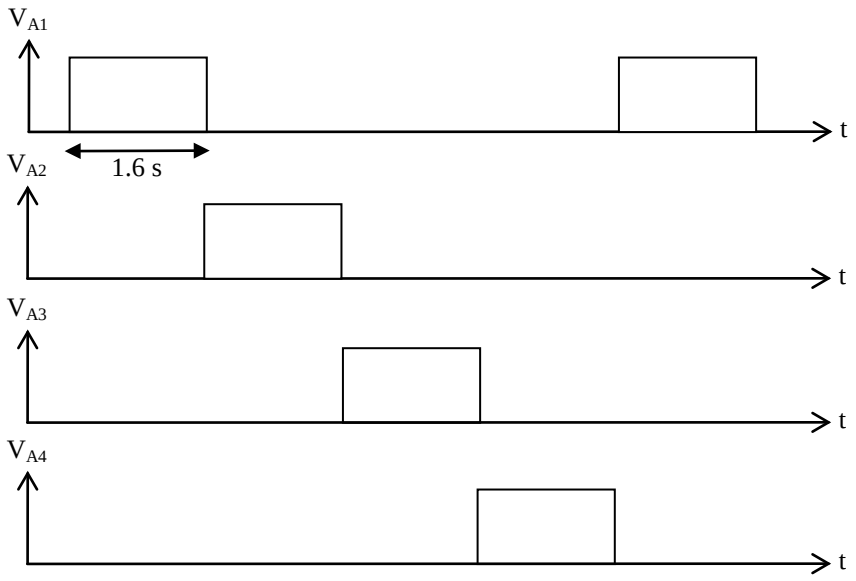

Figure 16: Example output of the non-overlapping clock

A full schematic of the clocks needed to operate the circuit is shown in Figure 17.

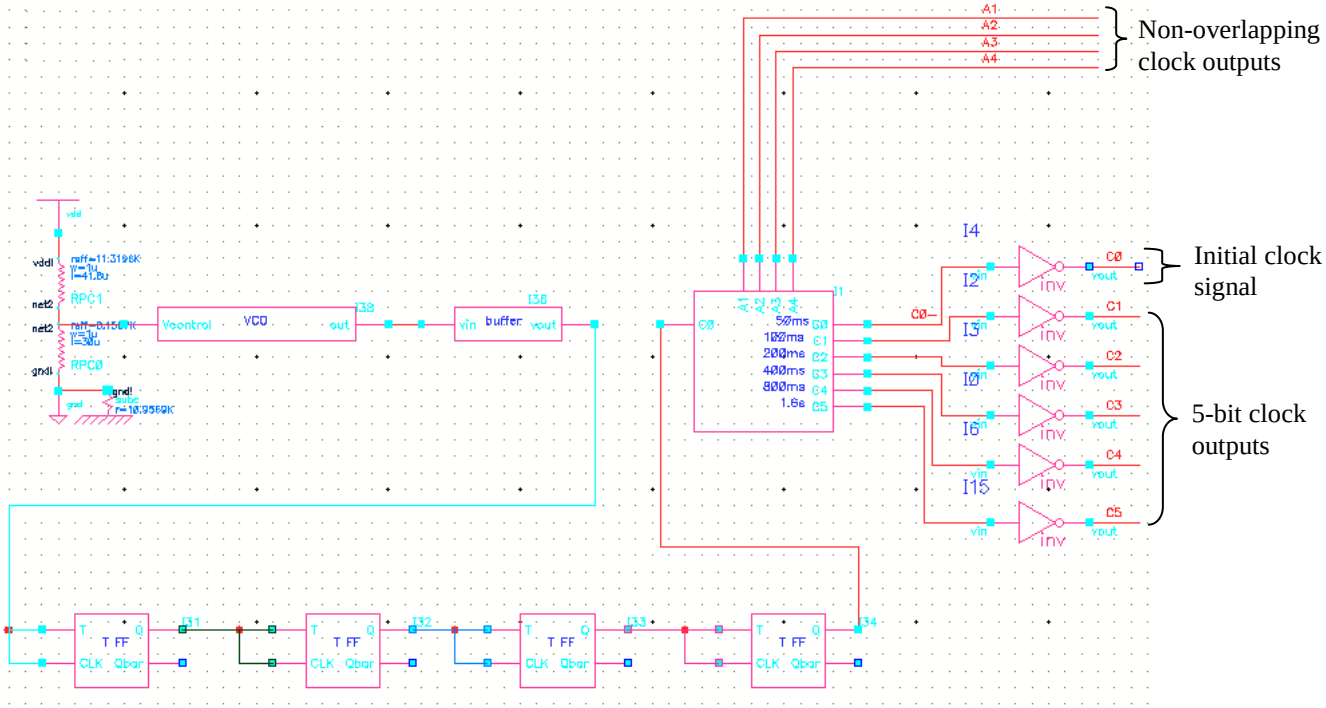

Figure 17: Clock schematic

2.3 Design of Read Only Memory

A total of 69 bits are needed to generate a Morse code signal reading ‘UMAINE ECE’. A table of the Morse code and digital representation for each letter is shown in Table 1.

Table 1: Morse code and digital representation of ‘UMAINE ECE’

Letter	Morse Code Representation	Digital Representation
U	••-	1010111
M	--	1110111
A	•-	10111
I	••	101
N	-•	11101
E	•	1
(space between words)		0000000
E	•	1
C	-•-•	11101011101
E	•	1

Note: Each letter is separated by 000

Since multiplexers are simplest to design with inputs based on powers of 2, the Read Only Memory (ROM) array was selected to be 4 word lines by 32 bit lines. This will make up a 128-bit ROM array. A schematic of the ROM array is shown in Figure 18 and operates as follows. When a word line is driven high by the non-overlapping clock, a Logic 1 or 0 on each bit line will be produced. A pull-up resistor (PMOS transistor) is used at the top of each bit line to hold the line high. If an NMOS transistor is present at the intersection of the word line and bit line, it will pull the line low, generating a Logic 0 on the line. A small capacitor was added to each bit line so ensure that the Logic 0 will be close to 0V. An example of a Logic 1 and Logic 0, and pull-up resistor are shown in Figure 19.

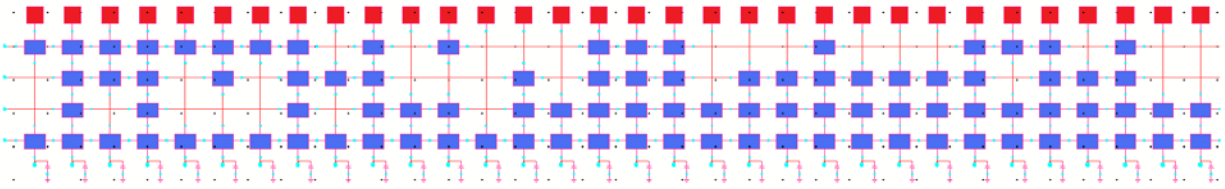

Figure 18: Schematic of ROM array where red boxes denote pull-up resistors and blue boxes denote a minimum sized NMOS transistor

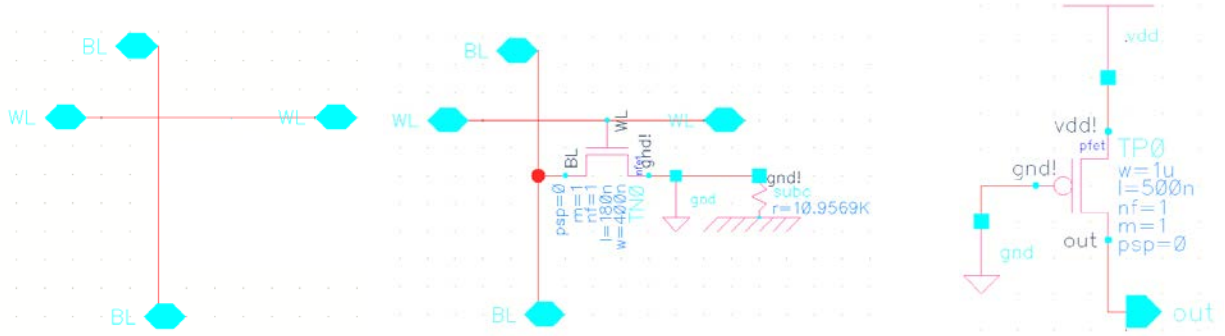

Figure 19: Schematics of Logic 1 (left), Logic 0 (center) and pull-up resistor (right)

The outputs from each bit line are fed into the inputs of a 32-bit multiplexer, discussed in the following section.

2.4 Design of 32-bit Multiplexer

A multiplexer (or 'MUX') is used to select one ROM bit line at a time, in sequential order, to produce an output that will spell 'UMAINE ECE' in Morse code. To create a 32-bit MUX, two 16-bit multiplexers and a transmission gate are used. Each 16-bit MUX is created using five 4-bit multiplexers, which are created using transmission gates. Transmission gates are used to reduce power consumption of the device. A schematic of each stage is shown in Figure 20. The select lines of the 32-bit multiplexer will be controlled by the 5-bit clock.

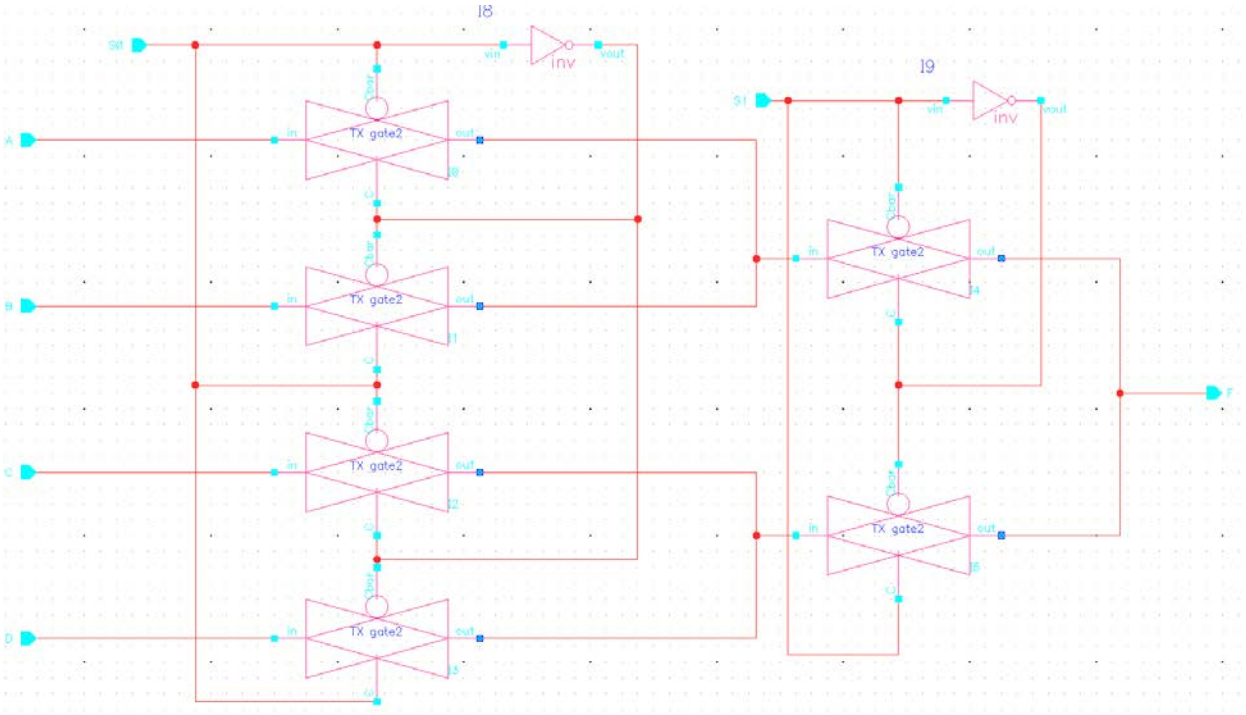

Figure 20a: Schematic of a 4-bit multiplexer

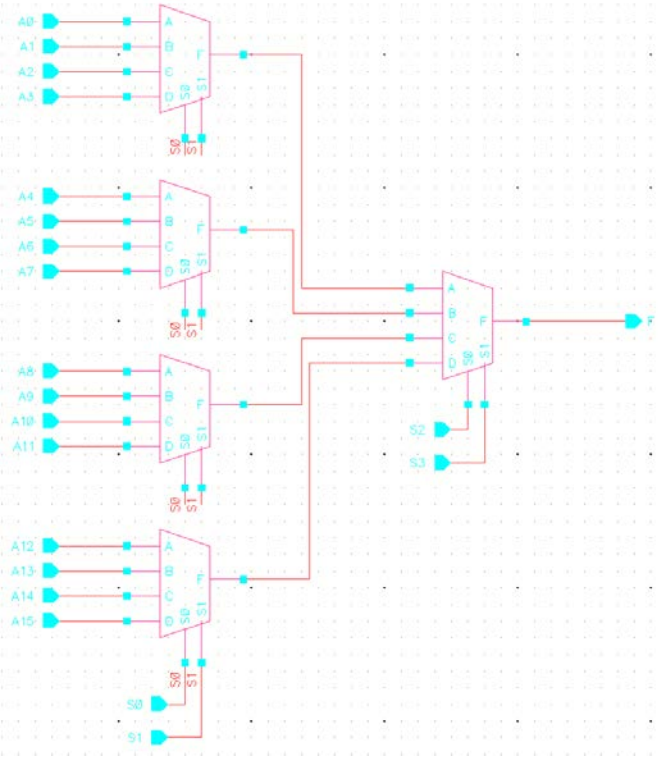

Figure 20b: Schematic of a 16-bit multiplexer

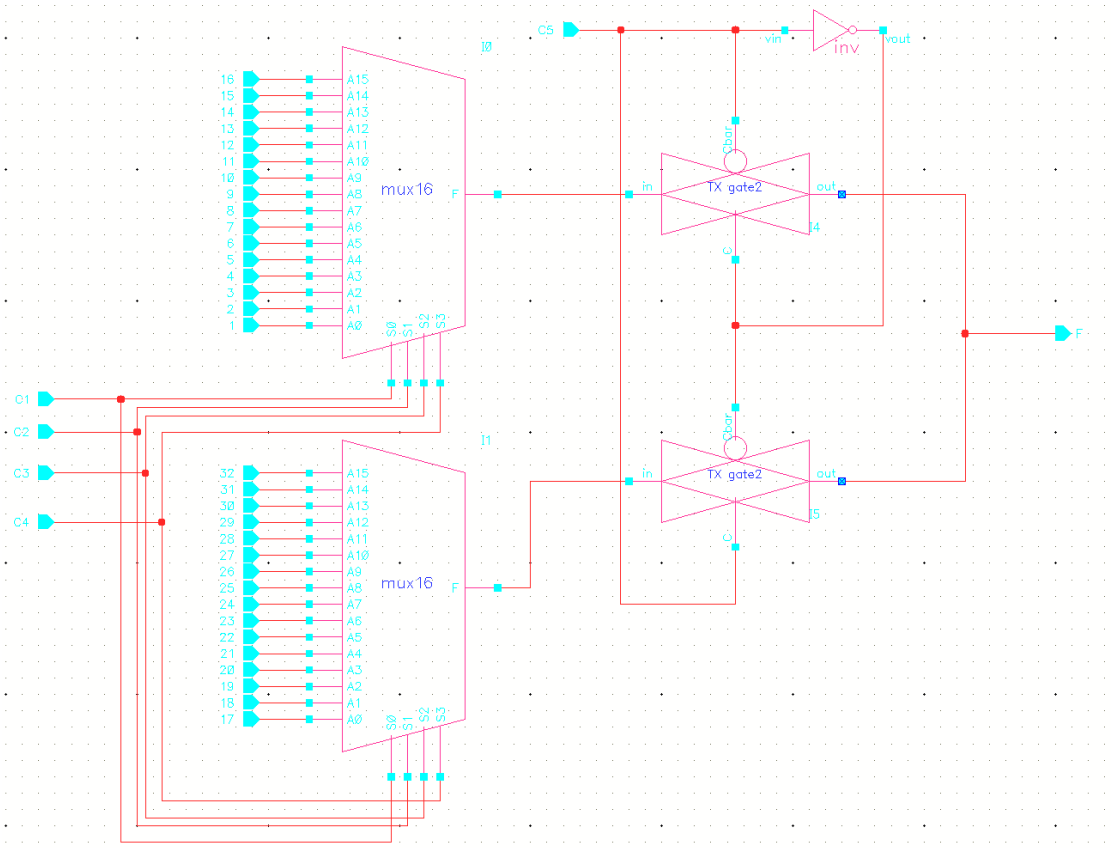

Figure 20c: Schematic of a 32-bit multiplexer

The output of the multiplexer was not a clean signal as expected (see Section 4.3 for simulations and Section 3.2 for layout). Inverters were used to ensure that the Logic 1 and Logic 0 outputs were at corresponding voltage levels. A D flip-flop was used to latch the signal at constant outputs to reduce noise on the signal. A delay element was needed for the clock input of the flip-flop. A schematic of the delay element is shown in Figure 21. It is made up of a series of inverters and capacitors, which give it a total delay of 5ms. Each capacitor is 80 pF, and inverter RO is an inverter with minimum transistor width and length of 170µm. The highest frequency clock signal from the MUX clock is used as an input. This ensures that the D flip-flop will latch the value of the signal when it has reached a Logic 1 or Logic 0, past any rise or fall time.

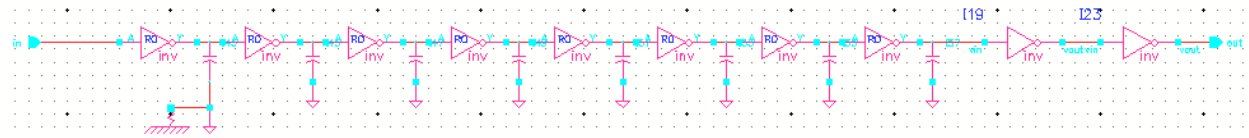

Figure 21: Schematic of 5ms delay element

2.5 Design of 433 MHz Sinusoidal Oscillator

An oscillation frequency of 433MHz was selected so that the output signal of the chip will be a Morse code signal in the ISM-band frequency range. The 433 MHz sinusoidal oscillator was designed using a standard LC circuit (Figure 22). The inductor, L, and capacitor, C, will share charge back and forth. The output of each side of the first stage will be a rail-to-rail sinusoidal signal at resonant frequency,

$$f_R = \frac{1}{2\pi(LC)^{1/2}} \quad (3)$$

Due to the parasitic capacitance inherent with each transistor in the circuit, the value of the discrete capacitor was lowered in order for the oscillation frequency to be closer to 433 MHz. The inductor and capacitor were selected to be 60nH and 800fF respectively.

A second stage (voltage buffer) is added to each output so that the oscillator will be able to drive an off-chip antenna that has an equivalent impedance of 74 Ω. The peak-to-peak voltage of the differential output will be reduced due to the impedance of the antenna. The transistors of the output stage are sized so that their current, I_{DS}, is a few milliamps, using the standard MOSFET equation,

$$I_{DS} = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2 \quad (4)$$

The output voltage across the antenna will be a sinusoidal signal with frequency 433 MHz, centered about 0V DC. Simulations are shown in Section 4.4.

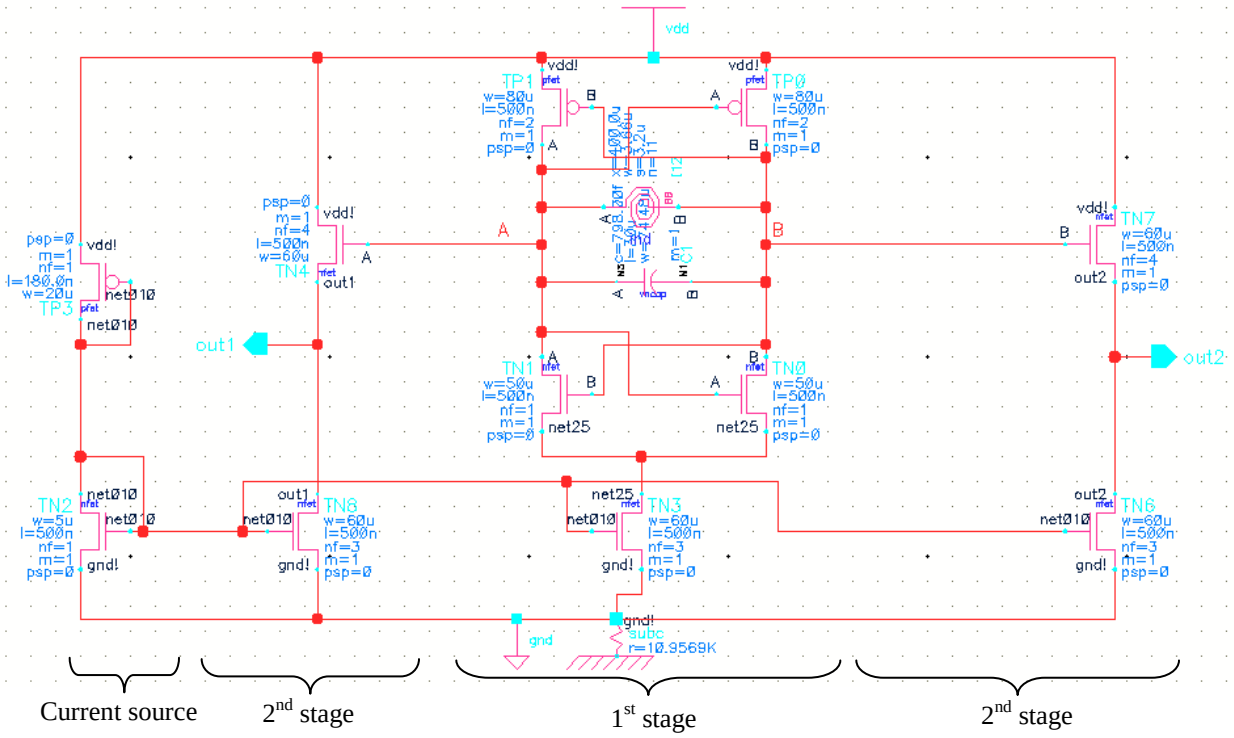

Figure 22: Schematic of 433 MHz oscillator

In order to control the output of the oscillator, a transmission gate and start up circuit were added to the design (shown in Figure 23). When the control bit is a Logic 0, the PMOS transistor will generate a '1' on one side of the oscillator, and the transmission gate will pull the gate of the current source transistors to ground. In this state, the oscillator will be off since no current will be drawn. When the control bit is a Logic 1, the PMOS transistor is turned off and the current source is turned on, which allows the circuit to oscillate. The oscillator will be controlled by the output of the 32-bit MUX, which is a logic representation of 'UMAINE ECE' in Morse code.

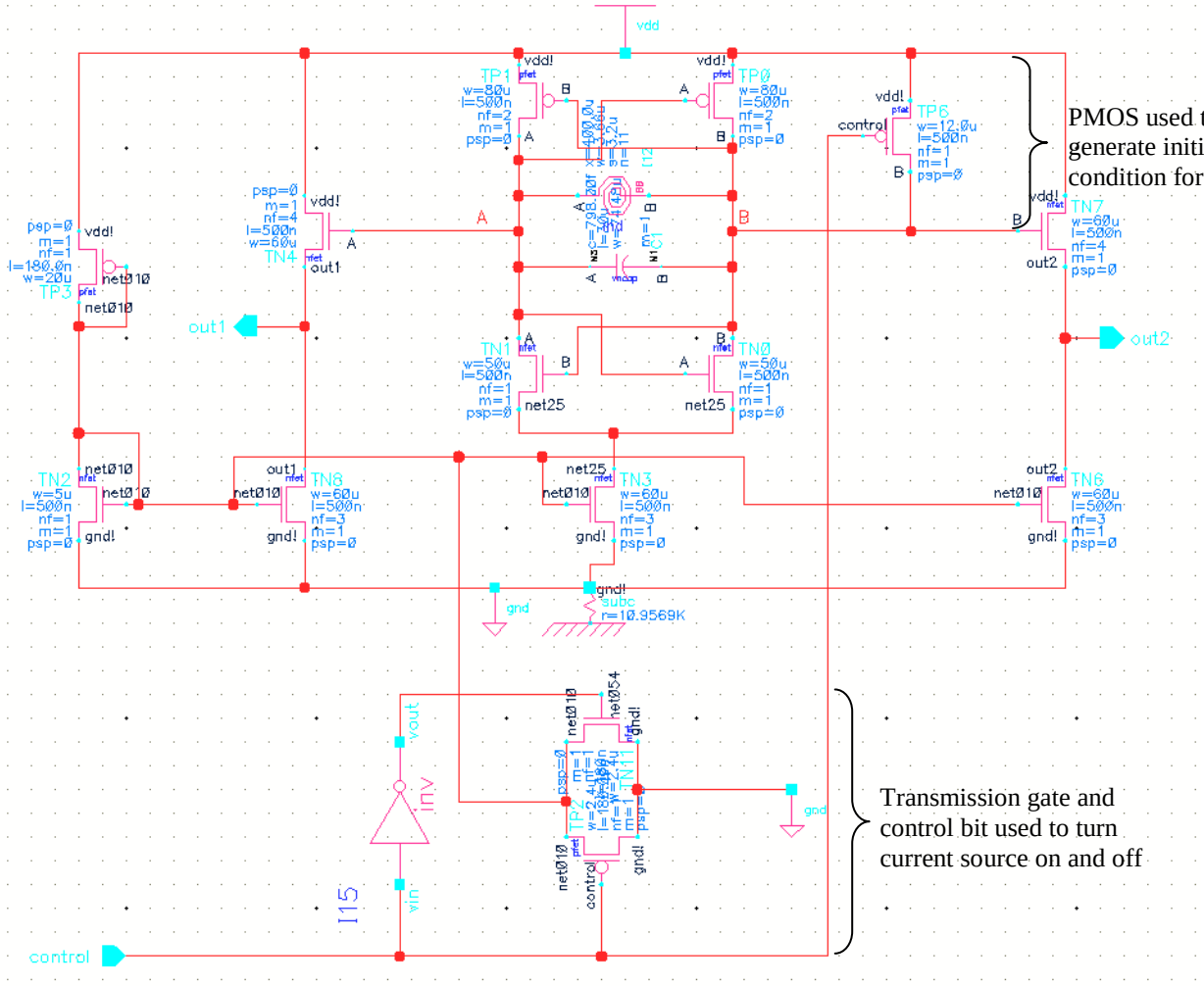

Figure 23: Schematic of 433 MHz oscillator with control bit and start-up circuit

A complete schematic is attached in Appendix A. The layouts of each part of the circuit will be discussed in the following section, Section 3.

3 Design Layout

All circuit layouts were designed using the Virtuoso layout editor in Cadence. Each piece of the circuit was laid out in such a way as to minimize device area. Careful consideration was used when sizes traces and placing vias, since the maximum current rating for each metal layer is ≈500 μA/μm, and for each via is ≈100 μA/μm. The layouts of the band-gap reference, clocks, ROM, multiplexer, oscillator, and the whole chip layout are shown in Sections 3.1, 3.2, 3.3, 3.4, 3.5 and 3.6 respectively.

3.1 Layout of Band-gap Reference

The band-gap reference circuit was laid out to minimize area on the chip, and is shown in Figure 24. Serpentine resistors were selected since they have the lowest temperature coefficient. They will vary the least over temperature out of all given resistors for this process. Due to the large amount of current that the band-gap reference will supply (≈3 mA), the majority of space used in the layout is taken up by the transistors used in the output stage of the op-amp.

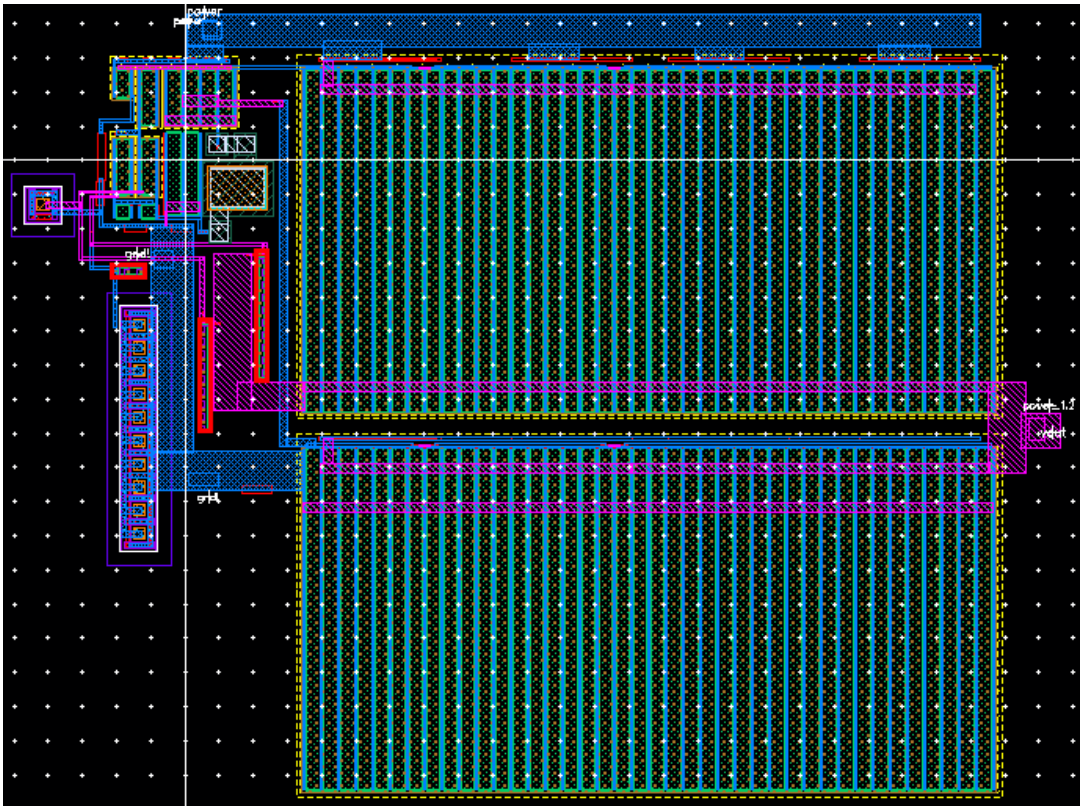

Figure 24: Layout of Band-gap reference

3.2 Layout Clocks and Delay Element

The delay element used to latch the multiplexer output will take up the largest layout area due to the capacitors in the circuit, so was designed first. MIMHK capacitors were selected since they take up the smallest area. The layout of the delay element is shown in Figure 25.

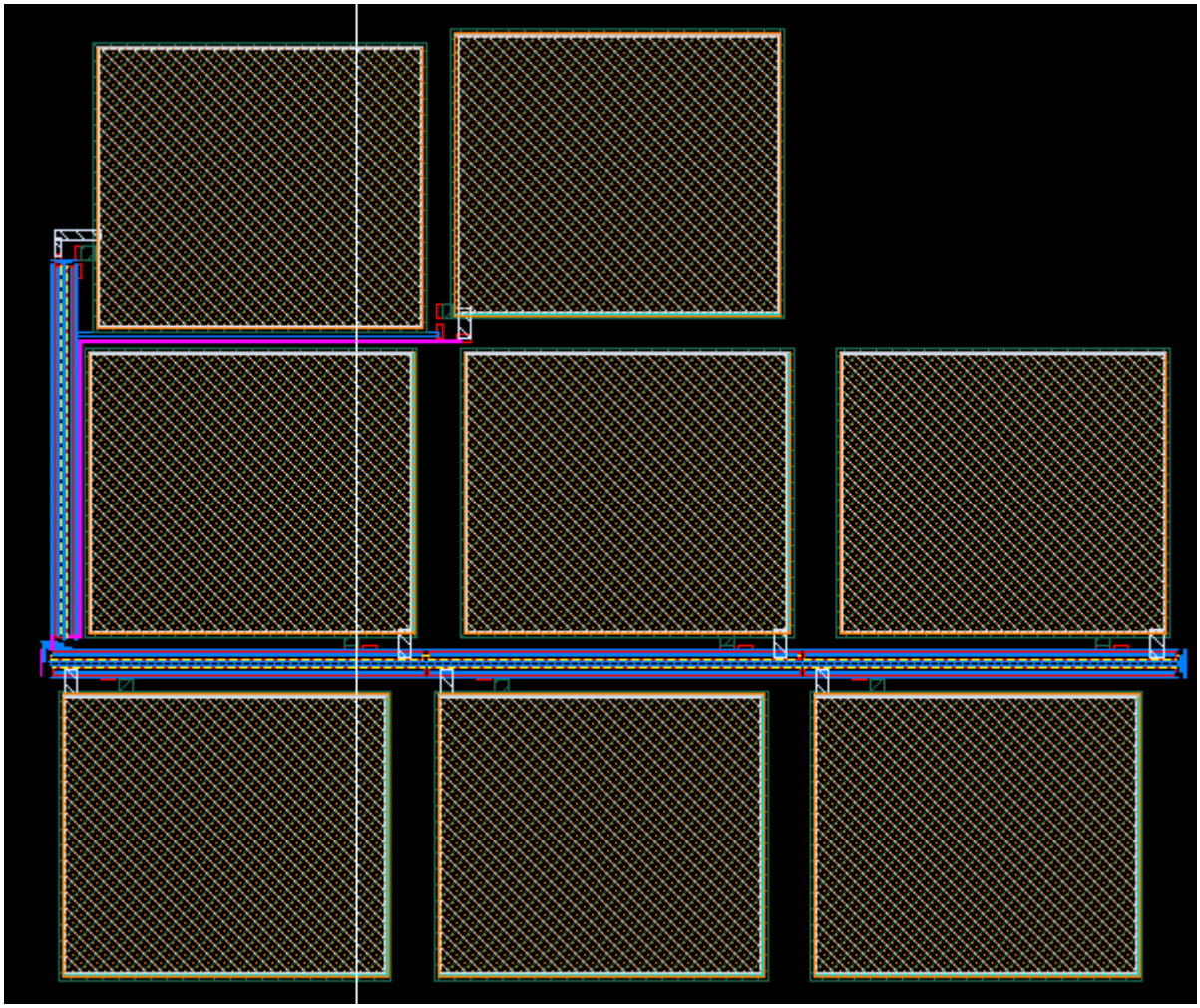

Figure 25: Layout of 5ms delay element

The Voltage-controlled oscillator was designed so that the layout will fit underneath capacitors in the layout of the delay element, which will reduce space needed on the chip. The VCO layout is shown in Figure 26, and the digital buffer used to sharpen the output of the VCO is shown in Figure 27.

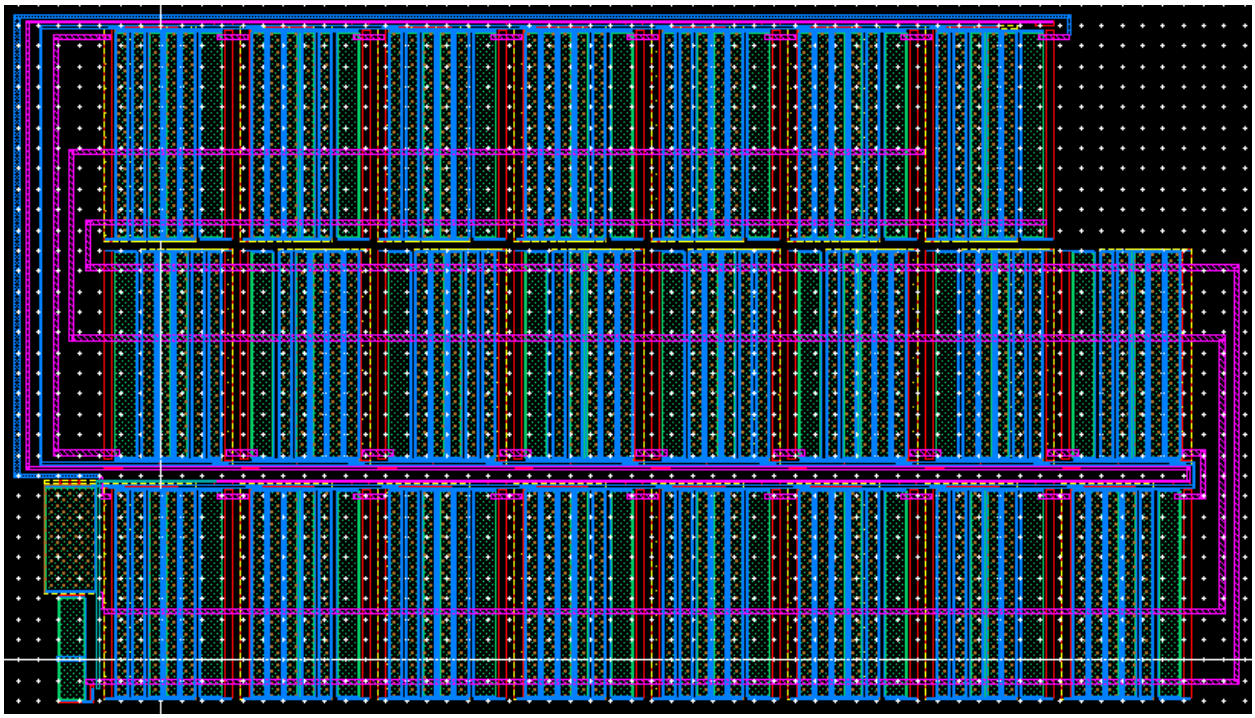

Figure 26: Layout of voltage-controlled oscillator

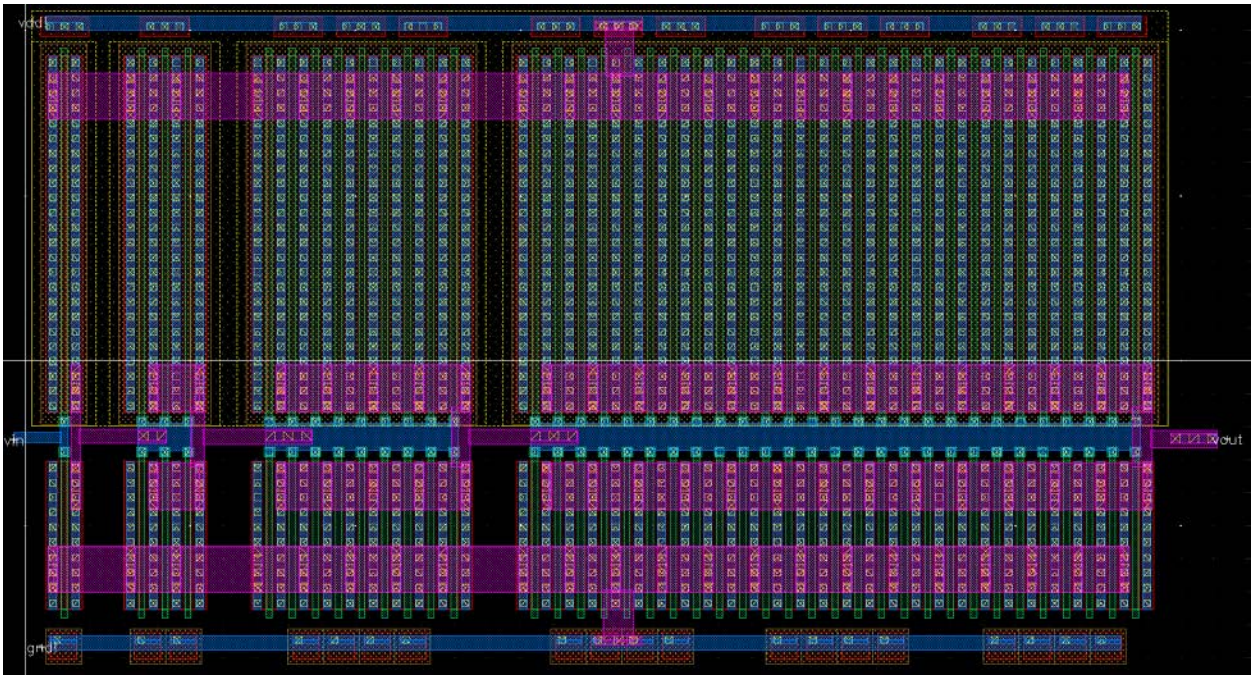

Figure 27: Layout of digital buffer

The layout of a T flip-flop used to reduce the frequency of the VCO is shown in Figure 28 below.

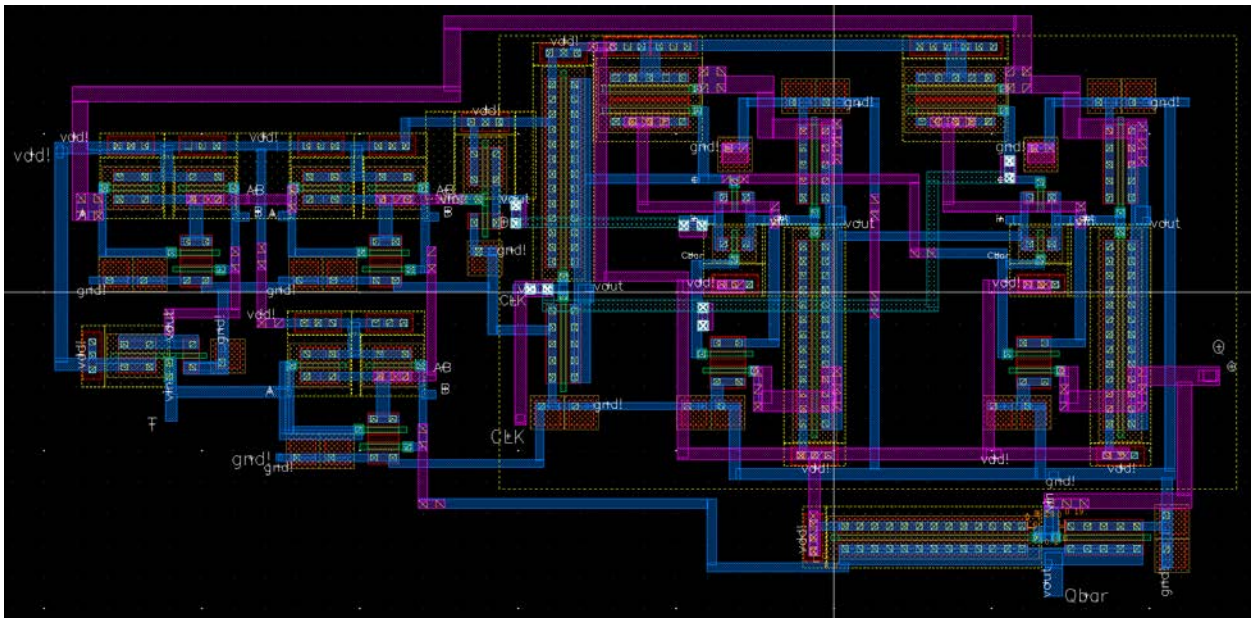

Figure 28: Layout of T flip-flop

The layout of the ROM access and multiplexer clocks is shown in Figure 29, which includes both the non-overlapping clock and 5-bit clock.

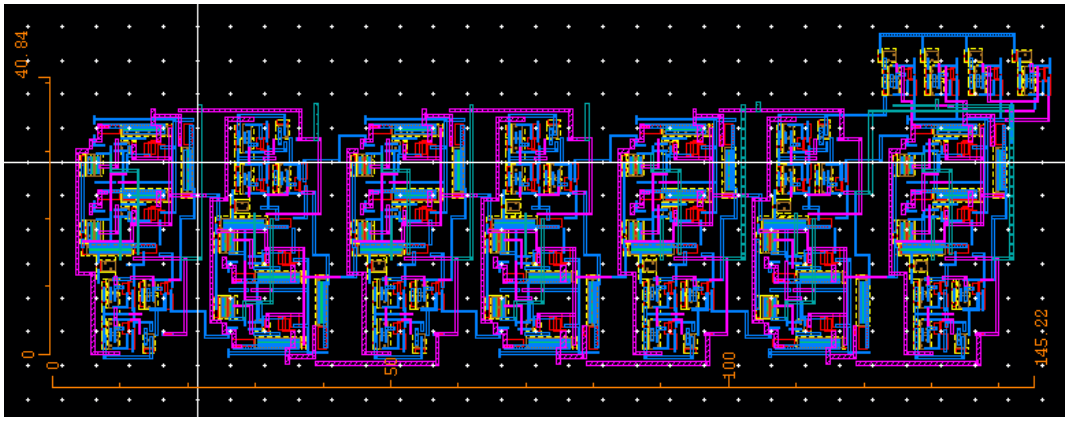

Figure 29: Layout of clock generation circuit consisting of the 5-bit and non-overlapping clocks

3.3 Layout of Read Only Memory

The size of the Read Only Memory is dependent on the layout of the NMOS structure that will be used to generate Logic 0's, since it will appear between word lines and bit lines, and the size of the pull-up resistors on each bit line. The layout of the NMOS and PMOS resistor are shown in Figure 30, with corresponding word lines and bit lines attached.

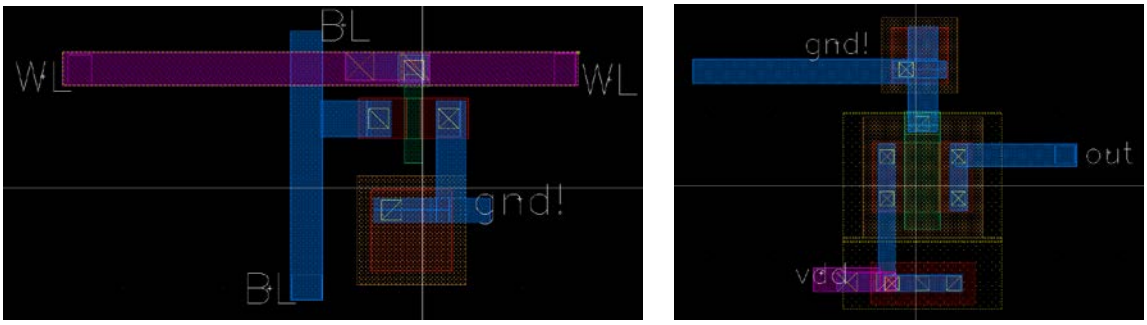

Figure 30: Layout of NMOS used to generate a Logic 0 (left) and PMOS pull-up resistor (right)

The 32-bit x 4-bit ROM layout is shown in Figure 31. The layout of the ROM was minimized on the spacing of the capacitors required by the process. MIMHK capacitors were selected since they take up the smallest amount of space. Although other devices can be placed beneath MIMHK capacitors, capacitors must be a certain distance apart. This limited how close bit lines could be to each other. The full layout of the ROM was measured to be 230 μm x 25 μm.

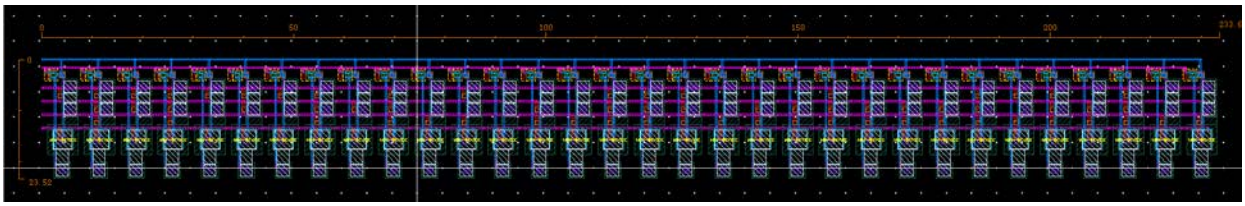

Figure 31: Layout of Read Only Memory Array

3.4 Layout of 32-bit Multiplexer

The layout of the 32-bit Multiplexer is shown in Figure 32. The layout was measured to be 200 μm x 50 μm.

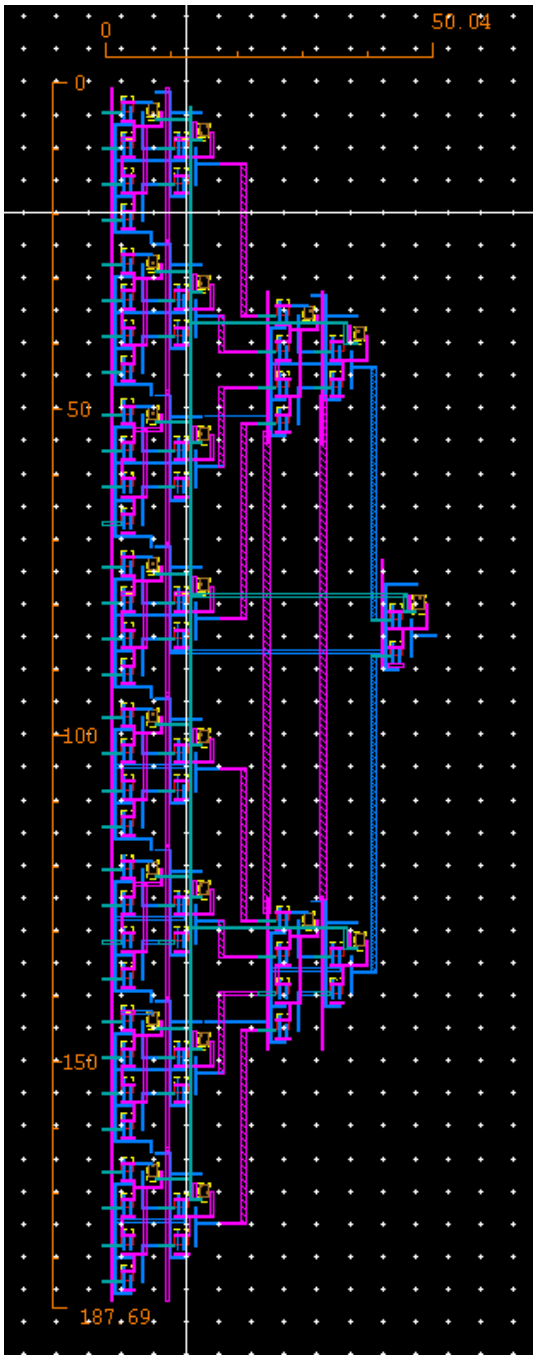

Figure 32: Layout of 32-bit multiplexer

3.5 Layout of 433 MHz Sinusoidal Oscillator

The majority of the space used for the layout of the oscillator was taken up by the inductor. The inductor size was selected to be 400 μm x 400 μm so as to have a high quality factor at the desired resonant frequency of 433 MHz. The layout of the oscillator is shown in Figure 33.

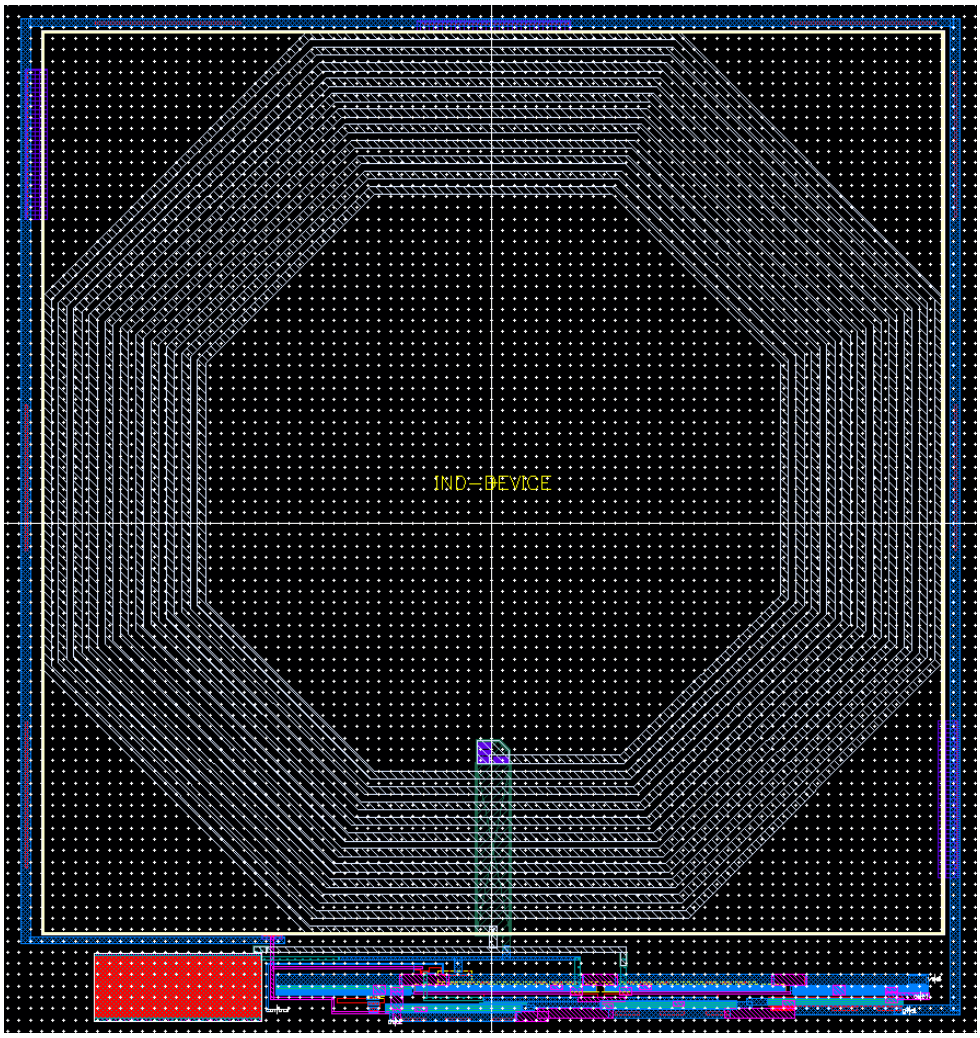

Figure 33: Layout of 433 MHz oscillator

The final circuit was laid out in such a way as to minimize area. The final chip layout can be seen in Appendix A. It is shown that there was room for two copies of the final circuit on each chip.

4 Circuit Simulation

Each piece of the circuit was simulated separately and confirmed to be working before being combined for more complex simulations. Simulations of the band-gap reference, clocks, ROM and multiplexer, and oscillator are shown and discussed in Sections 4.1, 4.2, 4.3, and 4.4 respectively.

4.1 Simulation of Band-gap Reference

The first piece of the circuit to be simulated is the operational amplifier used in the band-gap reference. The op-amp must have a high open-loop gain at low frequencies, preferably above 60 dB, and an appropriate gain margin to remain stable. The simulation of the op-amp is shown in Figure 34, where the low frequency gain is measured at 70.03 dB and the phase margin is 55.4 degrees, which meets requirements.

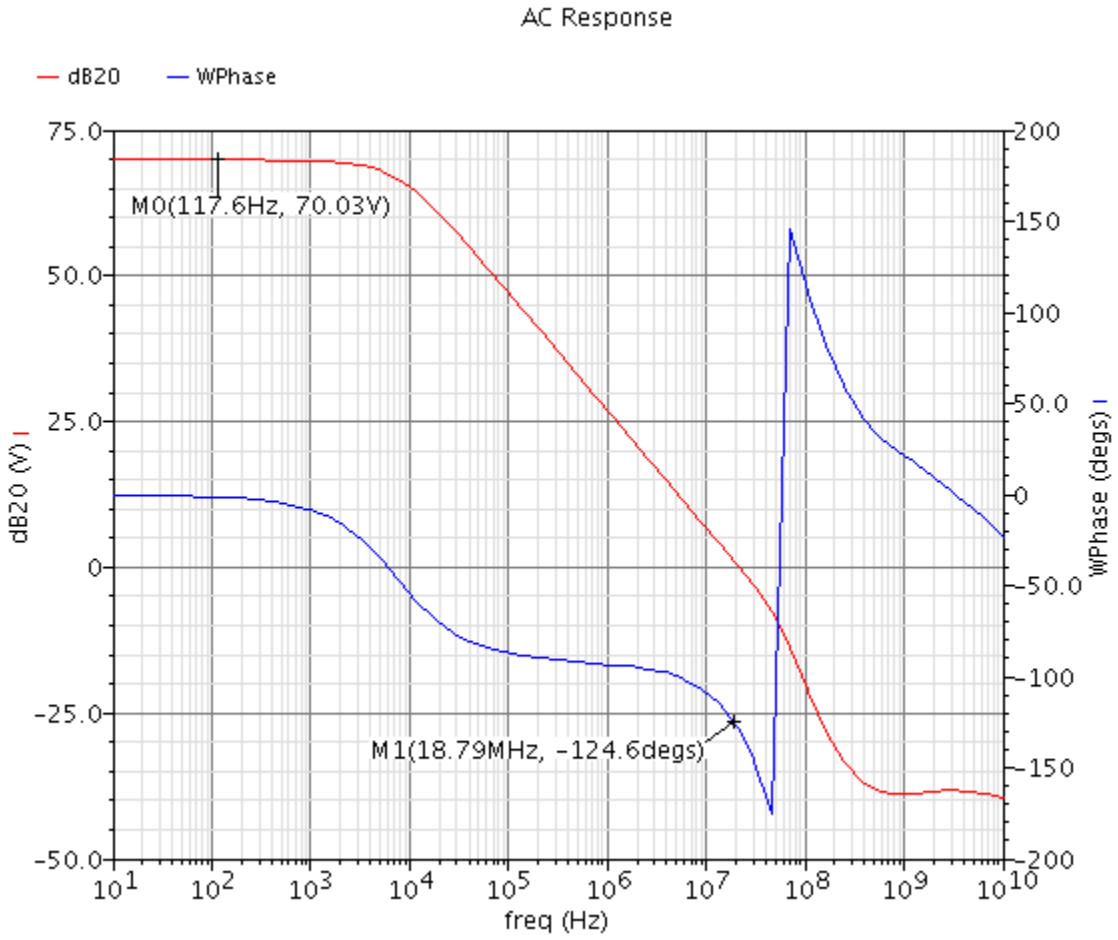

Figure 34: AC Simulation of open-loop gain and phase of the op-amp

The output voltage of the band-gap reference, including parastics in the layout design, was simulated over a temperature range of -50°C to 125°C and with varying input voltage levels from 1.7V to 3.2V. It can be seen from Figure 35 that the output voltage of the band-gap reference is relatively independent of voltage and changes in input voltage. For input voltages between 1.7V and 3.0V, the output voltage is 1.18V $\pm$ 0.01V. However, since the process specifies a breakdown voltage of around 2.6V, in reality the band-gap reference can operate on an input voltage from 1.7V to 2.6V.

A 100 mF capacitor was hooked up to the input of the band-gap reference with an initial condition of 2.6V. Driving all of the circuitry, the voltage drop across the capacitor was measured to be roughly 700mV for 4 seconds, the time needed to transmit the Morse code representation of 'UMAINE ECE'. This will drop the band-gap reference input voltage to a level of 1.9V. Since the 433 MHz oscillator requires the most power and is only running for half the time, it is safe to assume that the voltage drop on the capacitor will be closer to 350 mV over 4 seconds of transmission. Therefore, as long as the initial voltage level of the capacitor is above 2V, the circuit will be able to complete the transmission.

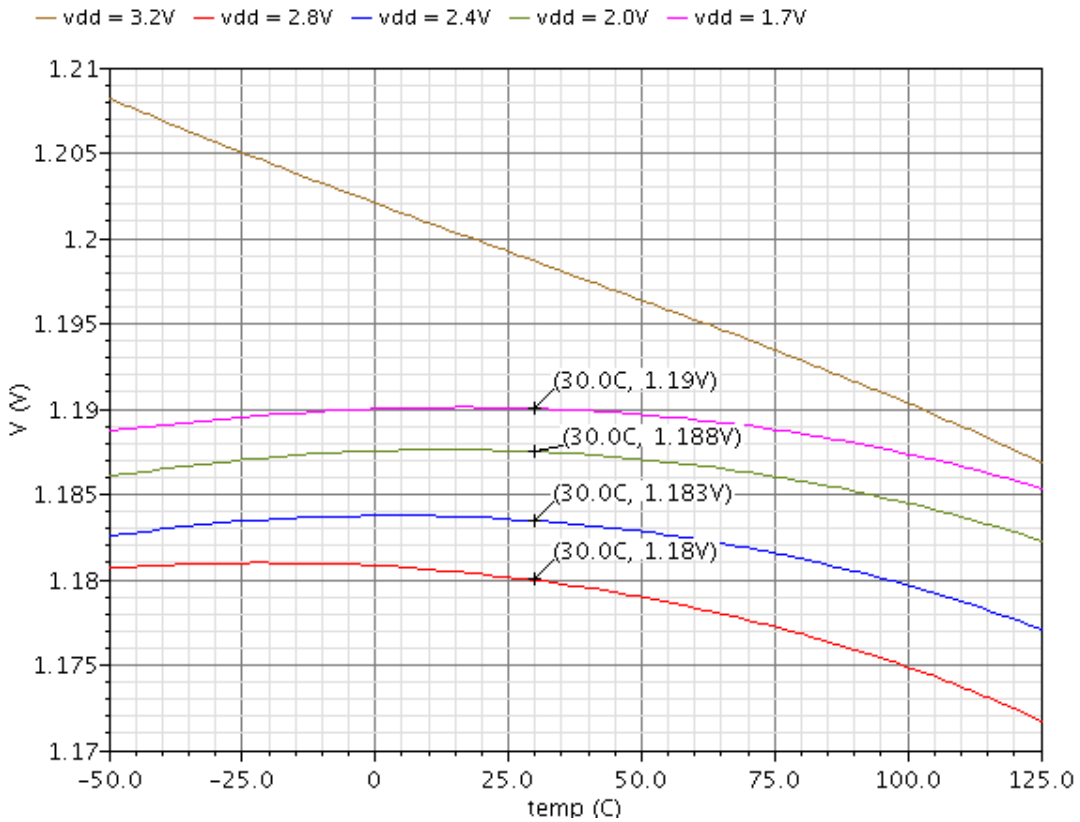

Figure 35: Simulation of band-gap reference with varying input voltage and temperature

4.2 Simulation of Clocks

The clocks are a very important part of the circuit. If one clock in the circuit fails, the output of the overall design will not be correct. Extensive simulations were done on each type of clock and are presented in this section. Simulation of the voltage-controlled oscillator is discussed in Section 4.2.1, the design of a 5-bit clock for the multiplexer select lines is discussed in Section 4.2.2, and the design of a non-overlapping clock to access the ROM is discussed in Section 4.2.3.

4.2.1 Simulation of Voltage-Controlled Oscillator

The transient response of the voltage-controlled oscillated was simulated and is shown in Figure 36. The period of the VCO is 3.128 ms which is very close to the designed period of 3.125 ms.

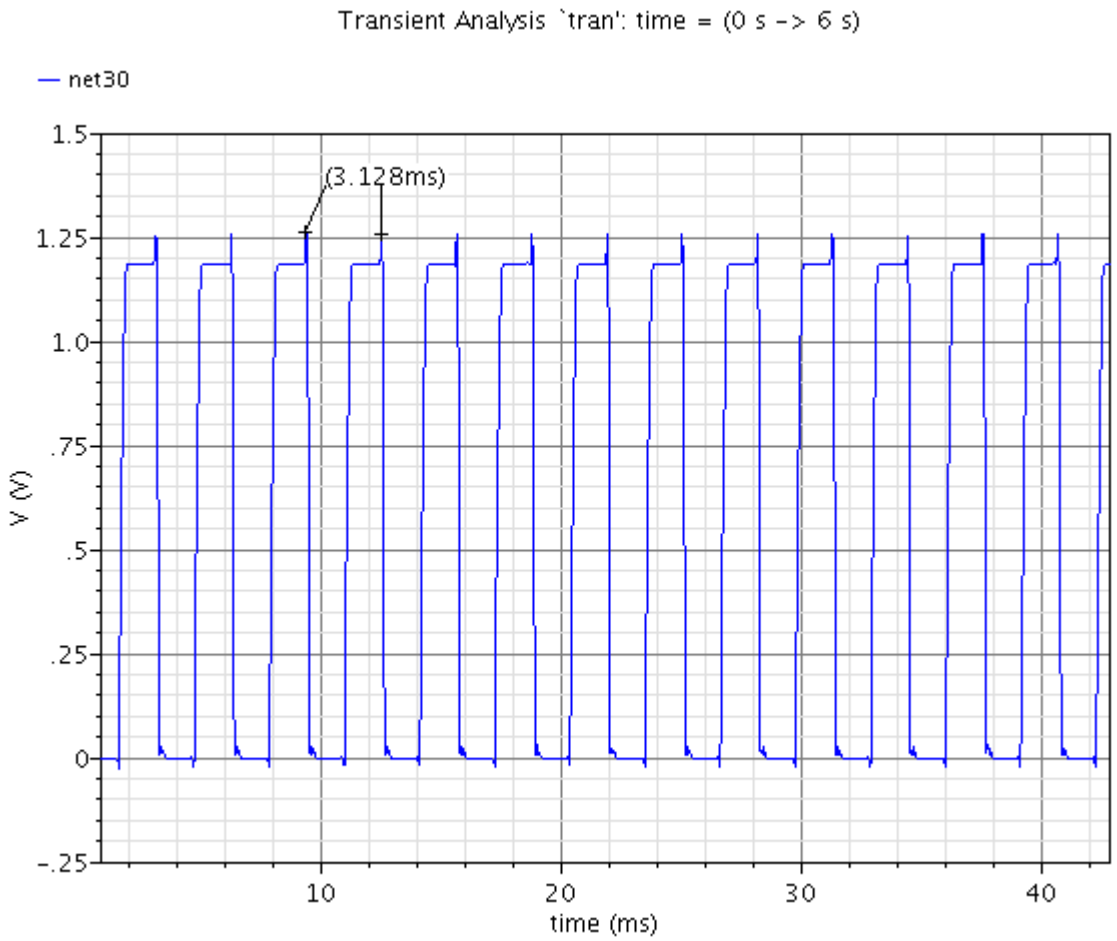

Figure 36: Transient response of the voltage-controlled oscillator

It can be seen from Figure 36 that the output of the VCO is not a very clean signal, but contains sharp spikes at the rise and fall times of each pulse. A digital buffer was used to eliminate and sharp peaks and to also increase the rise and fall time of the signal. The transient response of the VCO after the digital buffer was added is shown in Figure 37.

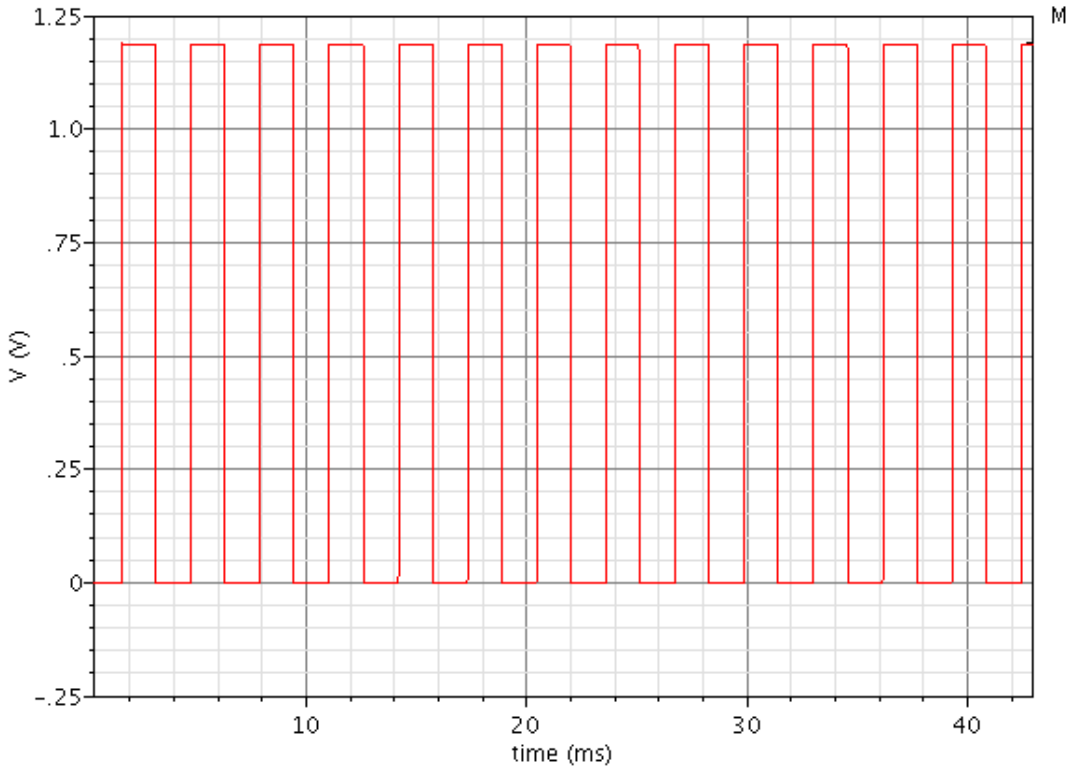

Figure 37: Transient response of VCO after digital buffer

The frequency of voltage-controlled oscillators is dependent on temperature; therefore the frequency of the bits on the output of the ROM and MUX is a measure of temperature and can be used as a sensor. The period and frequency of the VCO was measured at various temperatures, shown in Table 2 below. Also included in Table 2 is the corresponding pulse width of a bit on the output of the ROM and MUX. A plot of the data is shown in Figure 38.

Typically, as the temperature gets lower, the frequency of an oscillator will increase according to the temperature dependence of the MOSFETs. However, an opposite response was noticed. This could be due to the very slight temperature dependence of the band-gap reference circuit used as the power supply, which is used to drive the resistor ladder that supplies the VCO with a control voltage. Since a resistor ladder is used, any variations in supply voltage will cause variations in the VCO input, which in turn will change the output frequency of the VCO.

Table 2: Temperature dependence of the VCO and ROM/MUX output

	VCO		ROM/MUX	
Temperature (°C)	**Period (ms)**	**Frequency (Hz)**	**Period (ms)**	**Frequency (Hz)**
-50	4.883	204.8	78.13	12.8
-25	4.010	249.4	64.16	15.6
0	3.502	285.6	56.03	17.8
25	3.191	313.4	51.06	19.6
50	2.989	334.6	47.82	20.9
75	2.857	350.0	45.71	21.9
100	2.773	360.6	44.37	22.5
125	2.718	367.9	43.49	23.0

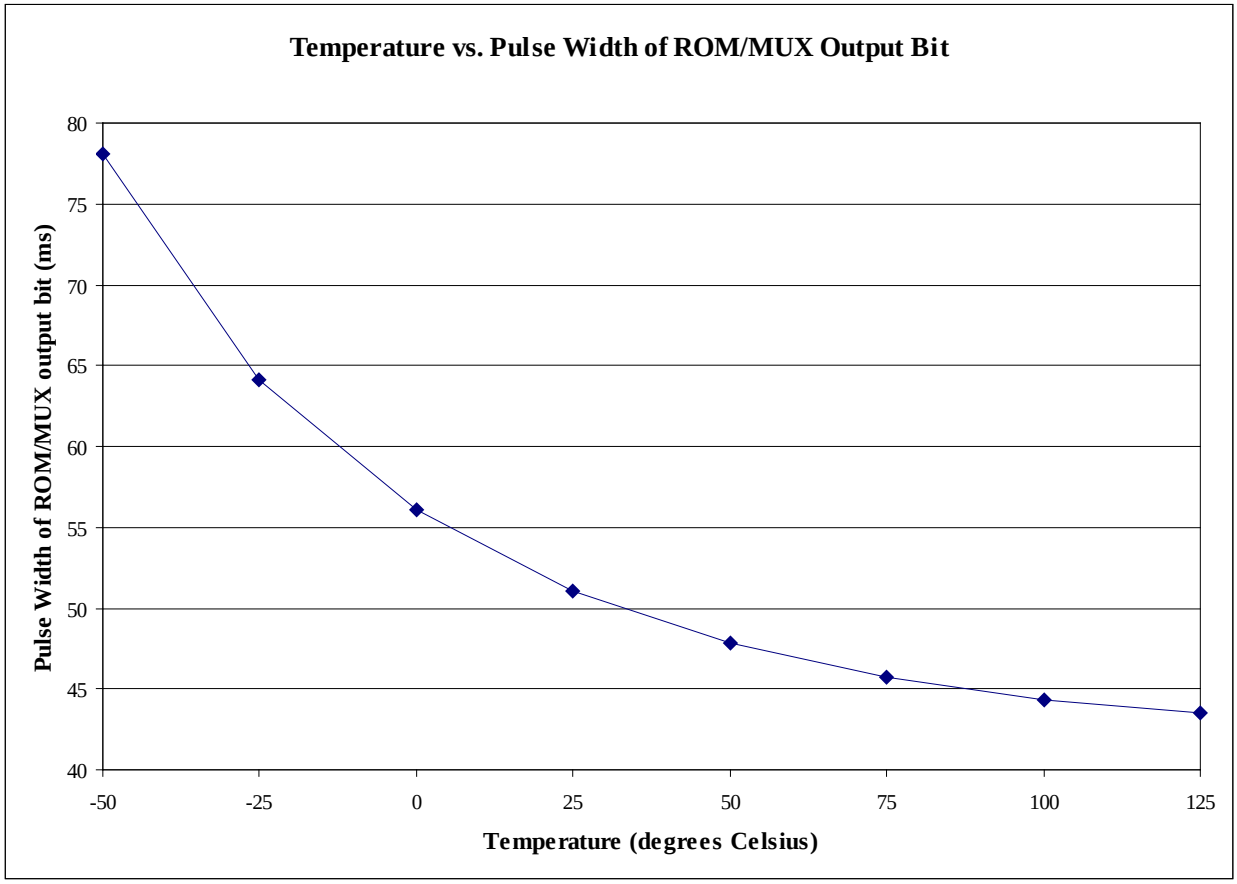

Figure 38: Plot of the temperature dependence of the ROM/MUX output. One bit (pulse width) corresponds to a Logic 1 or "•" in Morse code.

4.2.2 Simulation of 5-bit Clock

The transient response of each output of the 5-bit clock was simulated using Cadence software. The period of each clock line is listed in Table 3, and the transient signal is shown in Figure 39. It can be seen from the figures that the digital representation of the clock will start at 00001, where the least significant bit is clock C1. The 5-bit clock will count upwards in binary since each clock line has twice the period of the previous. This ensures that every bit in the ROM array will be latched by the MUX and in the correct order.

Table 3: Period of 5-bit clock lines

Clock Line	Period
C1	100.3 ms
C2	200.6 ms
C3	401.2 ms
C4	802.5 ms
C5	1.605 s

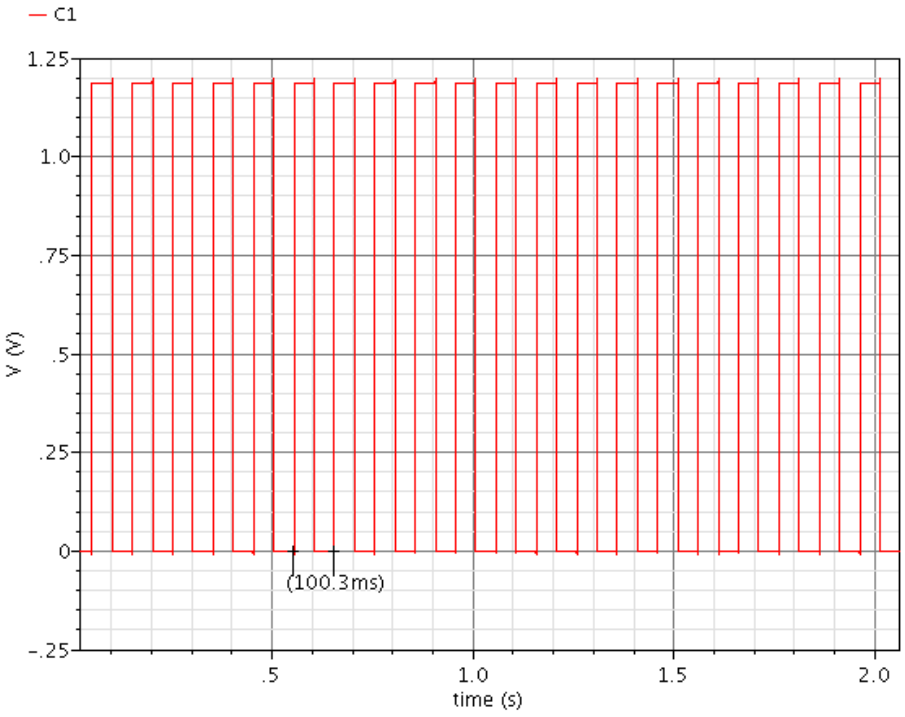

Figure 39a: Transient response of clock line C1

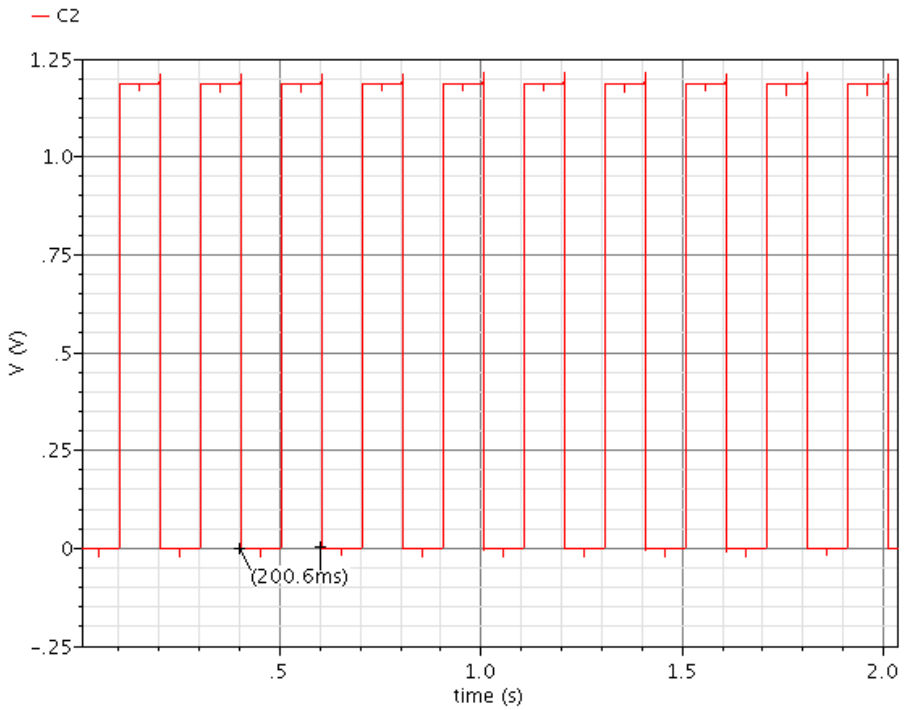

Figure 39b: Transient response of clock line C2

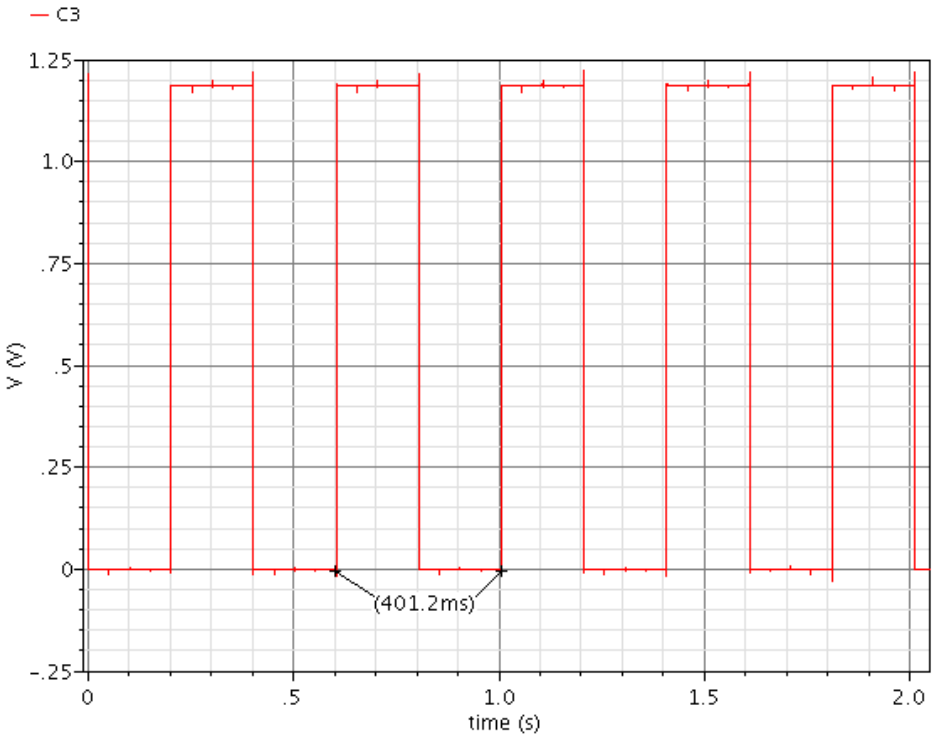

Figure 39c: Transient response of clock line C3

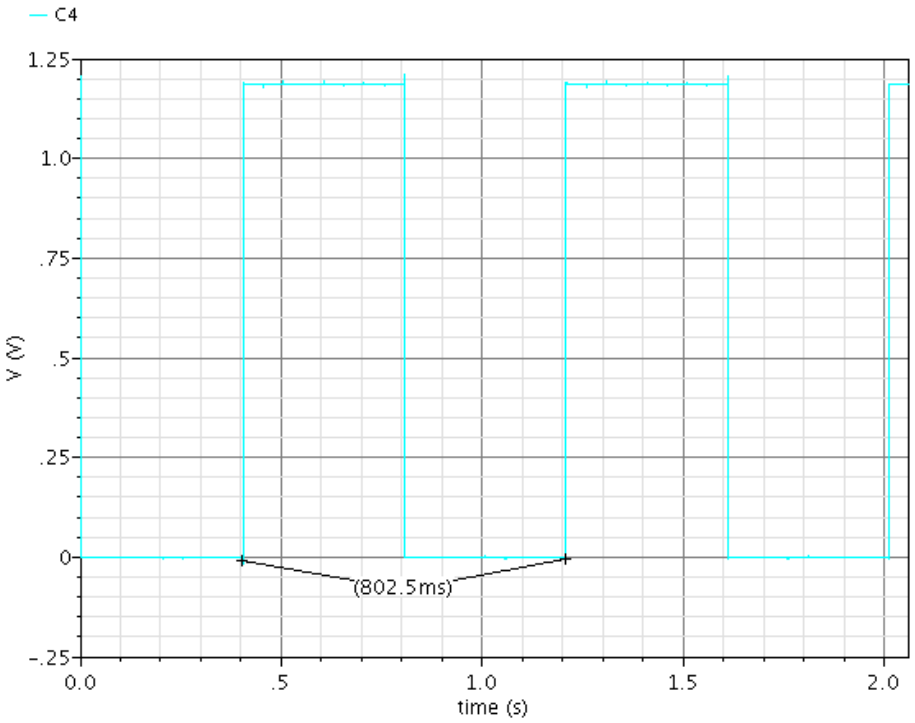

Figure 39d: Transient response of clock line C4

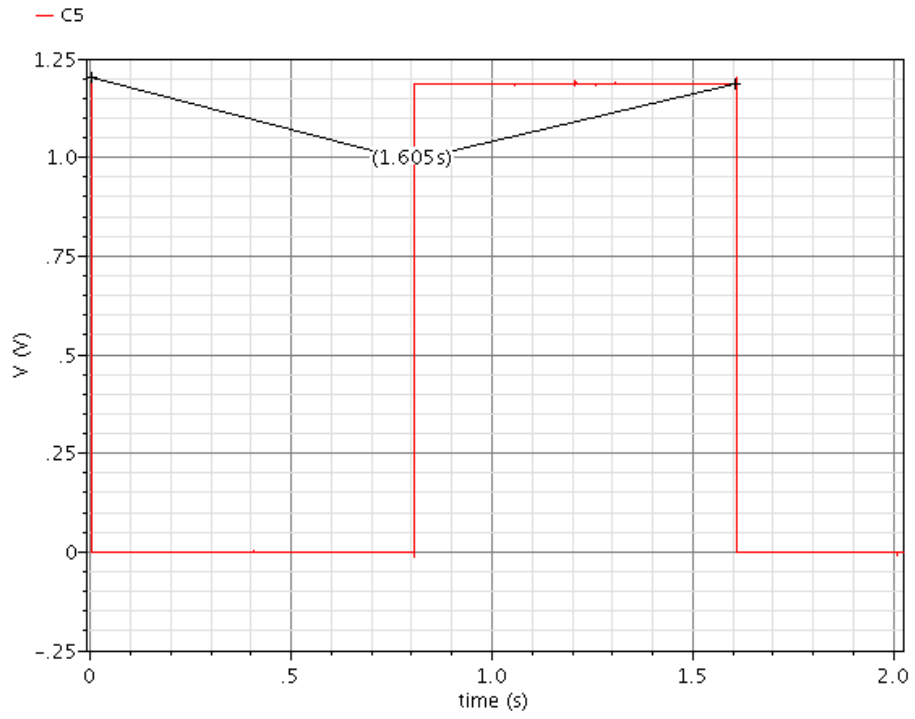

Figure 39e: Transient response of clock line C5

4.2.3 Simulation of Non-overlapping Clock

The transient response of the non-overlapping clock was simulated and is shown in Figure 40. Each of the four clock lines will be high for a time of 1.6 seconds, and no clock line will be high at the same time as any other. This clock is used to access the ROM word lines.

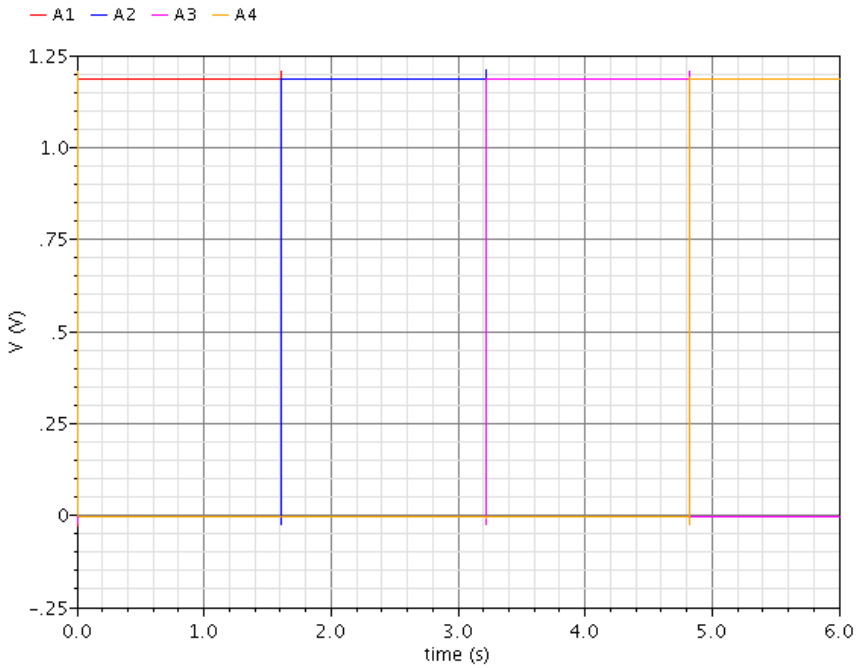

Figure 40: Transient response of the non-overlapping clock

4.3 Simulation of ROM and Multiplexer

The transient response of the read only memory and multiplexer were simulated. The non-overlapping clock was used as inputs to the ROM word lines, and the 5-bit clock was used as inputs to the select bits of the multiplexer. The 32 ROM output bit lines were wired to the 32 inputs of the MUX. The simulated output of the MUX is shown in Figure 41.

The simulation shows that at this point, the signal is not very clean. To fix it, two minimum sized inverters were added to the output of the MUX. The inverters will pull the signal from rail to rail ensuring that the Logic 1's and Logic 0's will be properly recognized. A D flip-flop was also added, as discussed in Section 2.4. The transient response of the 'cleaned' output is shown in Figure 42. Comparing the output to Table 1 in Section 2.3 shows that the output is the digital representation of 'UMAINE ECE' in Morse code.

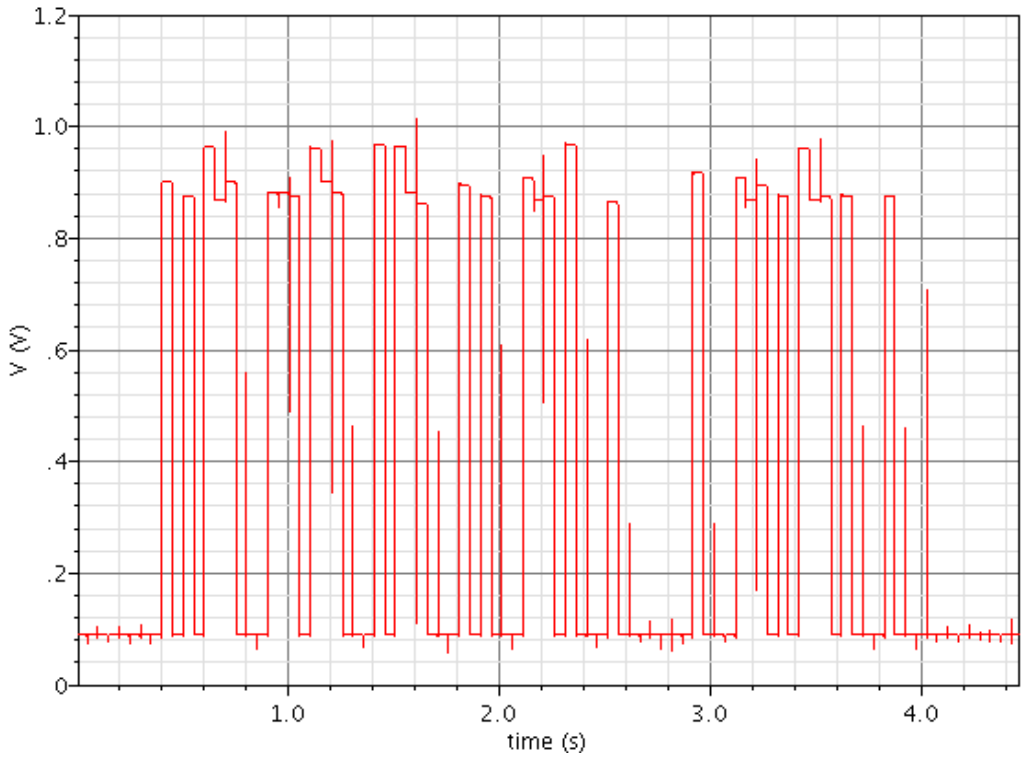

Figure 41: Transient response of the ROM>MUX output

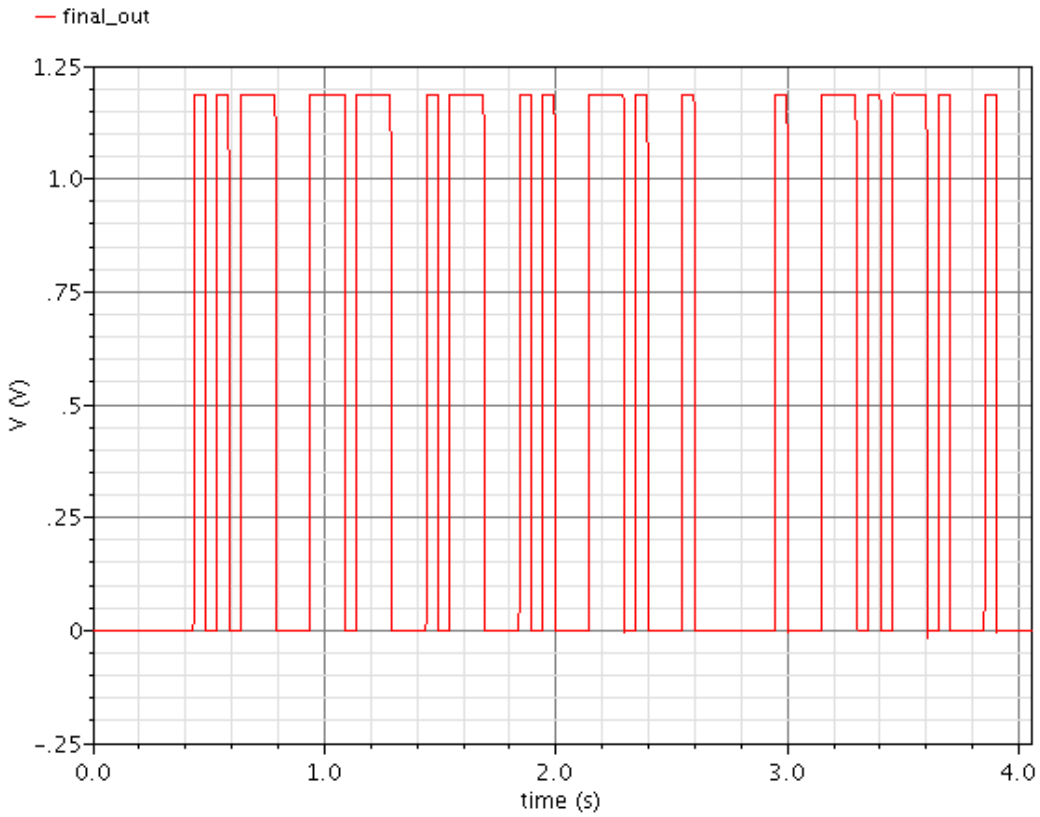

Figure 42: Transient response of ROM>MUX output after D flip-flop

4.4 Simulation of 433 MHz Oscillator

The transient response of the differential output of the 433 MHz oscillator, driving an off-chip antenna with impedance of 74 Ω, is shown in Figure 43 below. The differential signal has a peak-to-peak voltage of 325mV and frequency of 433.3 MHz which is within the ISM-band frequency spectrum. A close-up of the signal is shown in Figure 44. It can be seen that there is a slight distortion in the sinusoidal signal. This is caused by harmonics, but since the harmonics have a very low decibel level, they will not cause any interference. Simulations are done using the layout of the oscillator, including parasitics, to properly model the expected response.

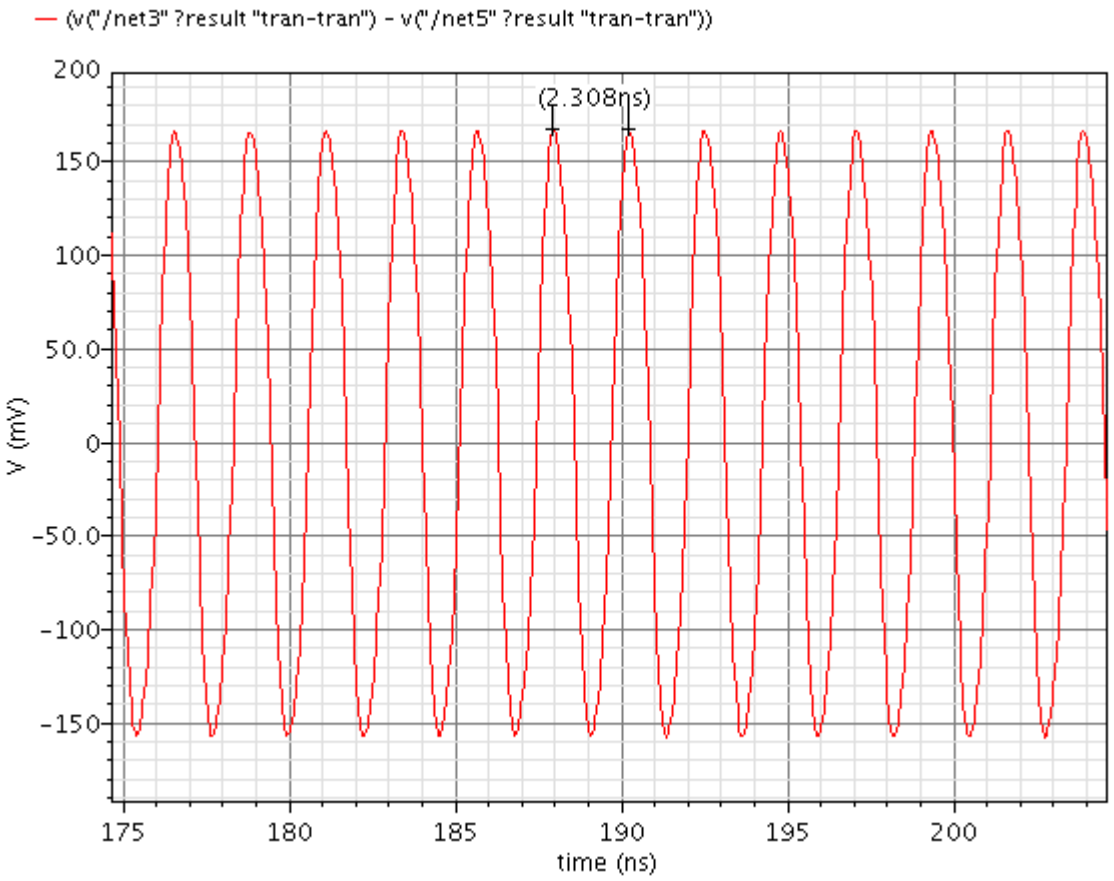

Figure 42: Differential output of the 433 MHz oscillator driving a 74 Ω antenna

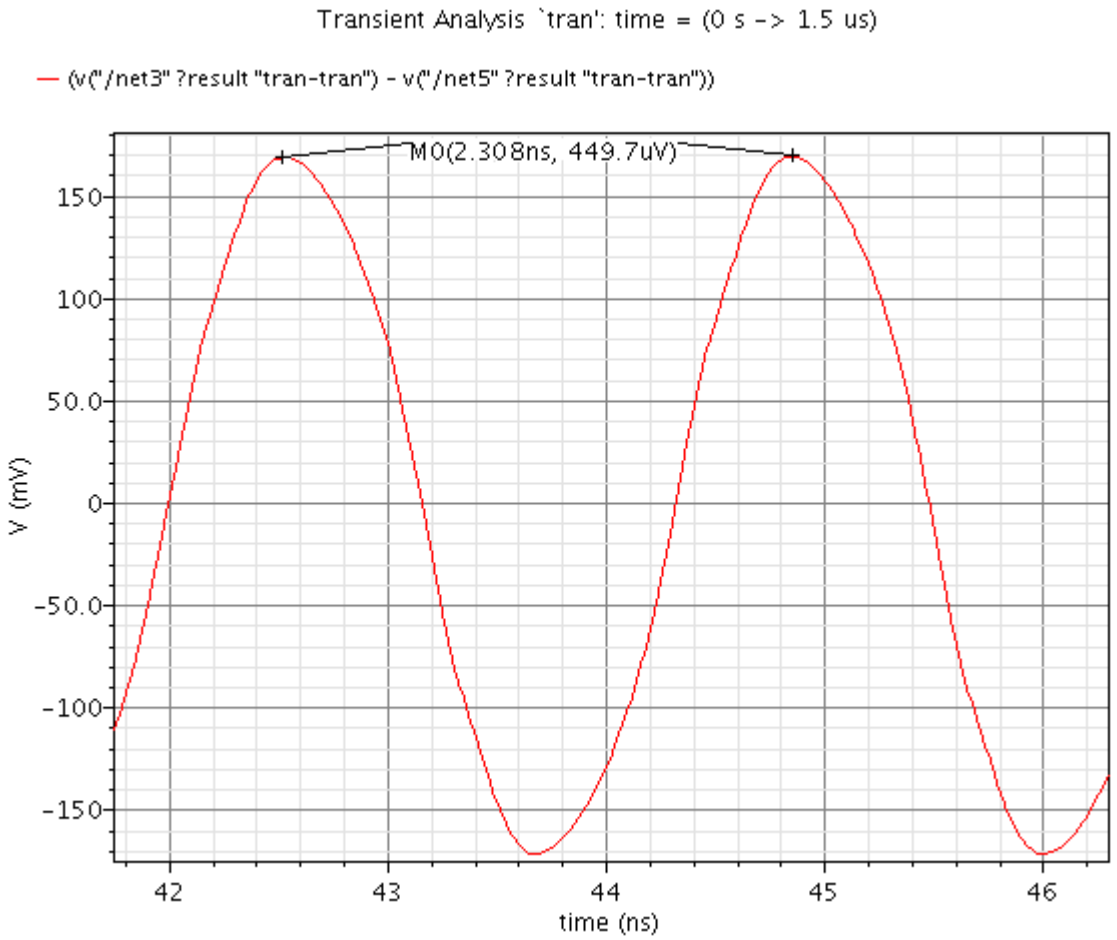

Figure 43: Close-up of the differential output of the 433 MHz oscillator driving a 74 Ω antenna

The oscillator was simulated with a control bit that varied from a Logic 1 to Logic 0 every 0.5 μs. Figure 49 clearly shows that the oscillator will start up with no initial conditions and will oscillate for every Logic 1 that is passed to the control circuit. Figure 50 shows that start-up response of the oscillator. It takes about 20 ns for the oscillation to reach a full peak-to-peak value of 325 mV.

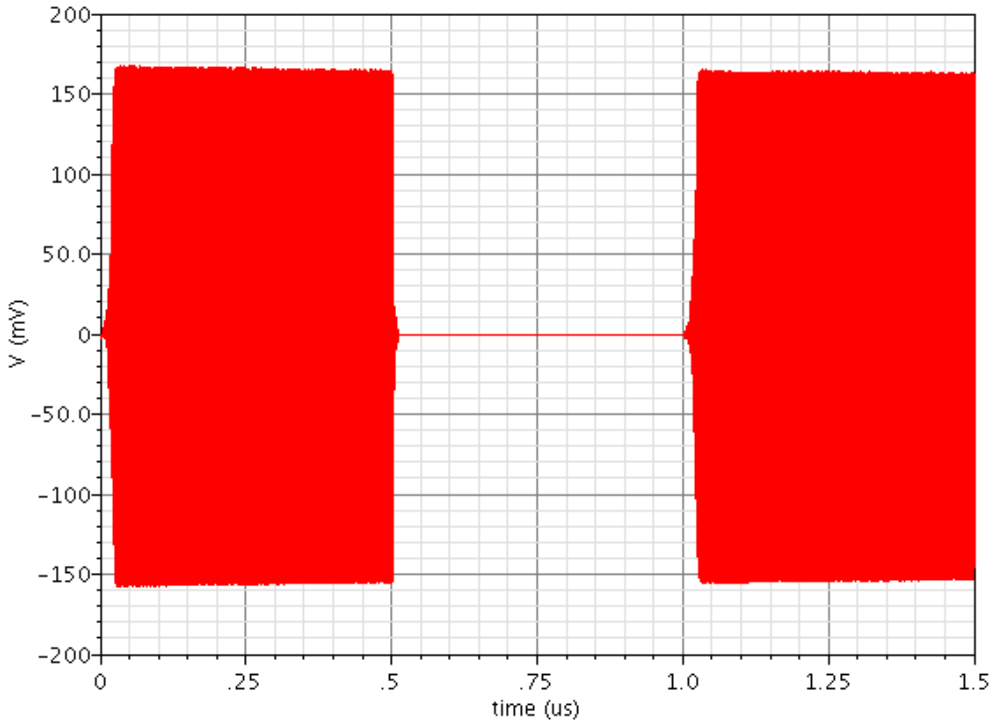

Figure 49: Differential output of the oscillator with control where a Logic 1 will cause the output to oscillate and Logic 0 will yield no oscillation on the output.

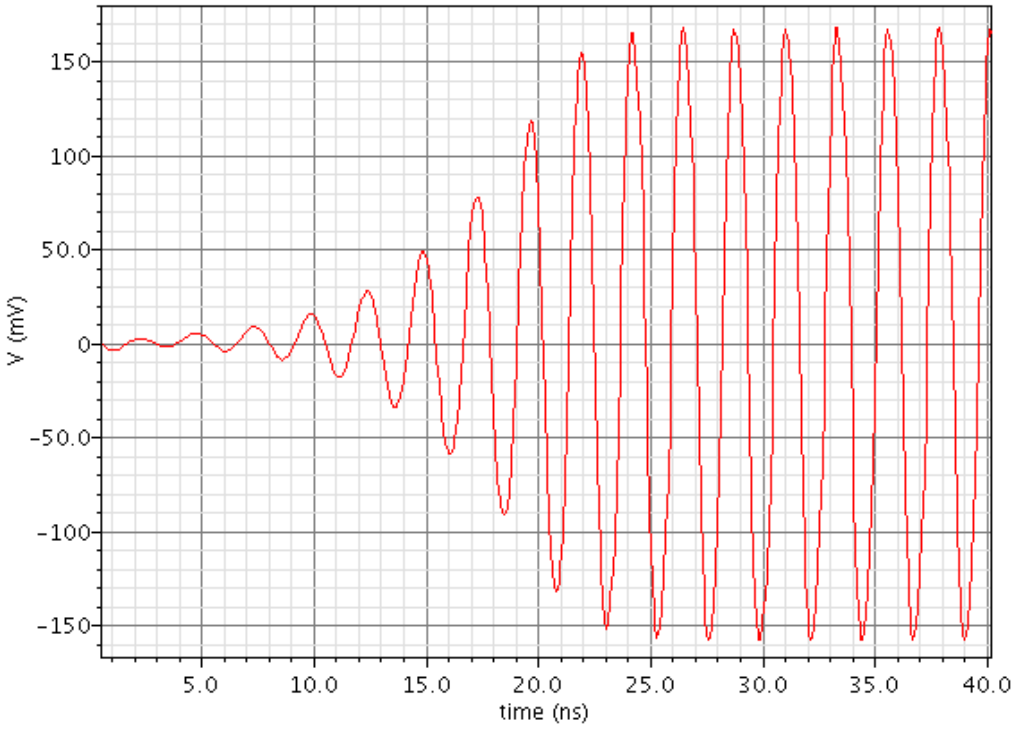

Figure 50: Differential start-up response of the oscillator output

5 Test and Verification of Device

Since the device only requires a few output pins, some key points in the circuit were tied to pins for verification purposes. Table 4 below shows each pin number and corresponding pin function. Pins 4-11 are connected to one copy of the circuit, and pins 24-31 are connected to an additional copy. Each chip contains two UMAINE ECE Morse Code ROM and transmitter circuits. Any unused pins were tied to ground. Verification of the band-gap reference, clocks, read only memory and multiplexer, and 433MHz oscillator are discussed in Sections 5.1, 5.2, 5.3, and 5.4 respectively. Text procedures should be followed for each circuit.

Table 3: Chip pins and pin functions

Pin Number	Pin Function	Pin Number	Pin Function
1	Ground	**21**	Ground
2	Ground	**22**	Ground
3	Ground	**23**	Ground
4	Input power to band-gap reference	**24**	Input power to band-gap reference
5	Output of band-gap reference	**25**	Output of band-gap reference
6	Ground	**26**	Ground
7	Output of voltage-controlled oscillator	**27**	Output of voltage-controlled oscillator
8	Output of clock bit CO1	**28**	Output of clock bit CO1
9	Output of ROM>MUX used to control 433 MHz oscillator	**29**	Output of ROM>MUX used to control 433 MHz oscillator
10	433 MHz oscillator output 1	**30**	433 MHz oscillator output 1
11	433 MHz oscillator output 2	**31**	433 MHz oscillator output 2
12	Ground	**32**	Ground
13	Ground	**33**	Ground
14	Ground	**34**	Ground
15	Ground	**35**	Ground
16	Ground	**36**	Ground
17	Ground	**37**	Ground
18	Ground	**38**	Ground
19	Ground	**39**	Ground
20	Ground	**40**	Ground

5.1 Verification of Band-Gap Reference

Power to the whole circuit is supplied by the band-gap reference circuit. The procedure to verify that the band-gap reference is operating as expected is given below.

1. The band-gap reference can run from a DC supply or from the charge on a capacitor. Initially, attach Pin 4 (or 24) to a DC supply.
2. Measure the output of the band-gap reference on Pin 5 (or 25). If the output seems unstable, connect a 470 μF capacitor (or one of similar value) from Pin 5 to Ground.
3. Sweep the input voltage and confirm that the band-gap reference output is independent from the power supply and over what range.
4. Sweep the temperature and confirm that the band-gap reference output is independent from the temperature and over what range.
5. Attach a charged capacitor to the input of the band-gap reference. Repeat steps 3 and 4.

5.2 Verification of Clocks

Although discrepancy in the exact period or frequency of the clocks does not matter, it needs to be confirmed that the clocks are working properly. The procedure to verify that the clocks are working properly is given below.

1. Measure the output of the voltage-controlled oscillator from Pin 7 (or 27) to confirm that it is oscillating. The output of the VCO is taken after the digital buffer so the internal capacitance of oscilloscope probes should not affect the signal. The VCO output should have a period of 3.125 ms.
2. Measure the output of the lowest clock bit, CO1, from Pin 8 (or 28). This clock should have a period of 50 ms.

5.3 Verification of ROM and Multiplexer Output

The output of the ROM and MUX are used as the control bit for the 433 MHz oscillator. If that oscillator does not operate properly, an off-chip oscillator can be used. An off-chip oscillator can run from the ROM>MUX output bit. To verify that the ROM>MUX output is providing the oscillator with the correct signal, measure the output from Pin 9 (or 29). The signal should be a digital representation of ‘UMAINE ECE’ in Morse code as discussed in Section 2.3.

5.4 Verification of 433MHz Oscillator

The procedure to verify the output of the 433 MHz oscillator is given below.

1. Measure the differential output of the oscillator from Pins 10 and 11 (or 30 and 31) without a load to confirm the correct operating frequency.
2. Connect the off-chip antenna and measure the differential output across it.
3. Sweep the input voltage and confirm that the oscillation frequency and magnitude of the output is independent from the power supply and over what range.
4. Sweep the temperature and confirm that the oscillation frequency and magnitude of the output is independent from the temperature and over what range.

The measurements resulting from the procedures in Sections 5.1-5.4 should be compared to the simulations in Sections 4.1-4.4.

6 Summary and Conclusion

The design, simulation and layout of a 'UMAINE ECE' Morse code Read Only Memory and transmitter were described. Simulations show less than $\pm$10mV variation around 1.185V in the band-gap reference output from -50°C to 125°C with a charge on an input capacitor ranging from 1.7V to 2.6V. The output of the overall circuit is a 325mV peak-to-peak sinusoid that oscillates at 433MHz (ISM-band frequency), where each character in the Morse code has a 50ms pulse width. Test and verification procedures were outlined and described.

6.1 Suggestion for Future Work

The distance that an off-chip antenna can transmit is proportional to the power that is supplied to it by the 433 MHz oscillator. One major improvement to the circuit would be to design an oscillator with higher peak-to-peak voltage and therefore higher power output.

Aside from this, the chip has been simulated to operate under a variety of conditions where temperature and input voltage will vary, and the output has remained consistent.

6.2 Biography

Jamie Reinhold grew up in South Portland, ME and graduated from South Portland High School in June 2007. She graduated from the University of Maine with a Bachelor's degree in Electrical Engineering in May 2011. Currently, Jamie is pursuing a Masters degree in Electrical Engineering at the University of Maine with a focus in nanotechnology with an expected graduation date of December 2012.

A Appendix

Final Circuit Schematic and Layout

The final schematic of the circuit is shown in Figure 51. The layout of the final circuit is shown in Figure 52. The full chip layout, including two copies of the circuit, is shown in Figure 53. References are also cited in this section.

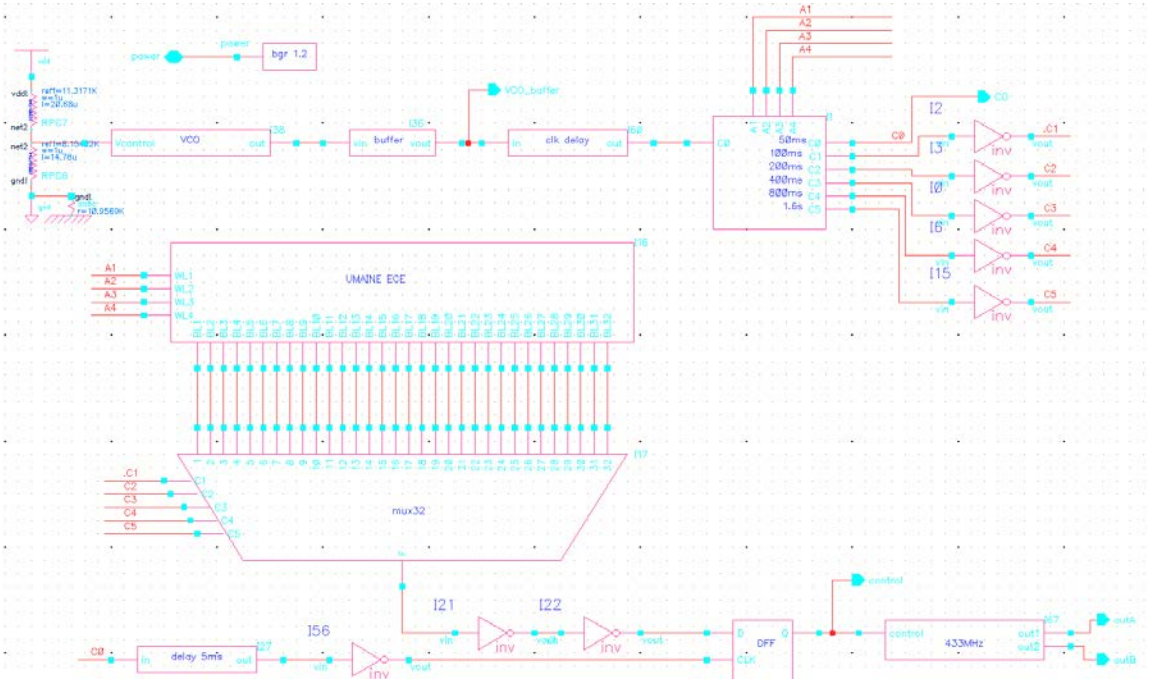

Figure 51: Top level design schematic

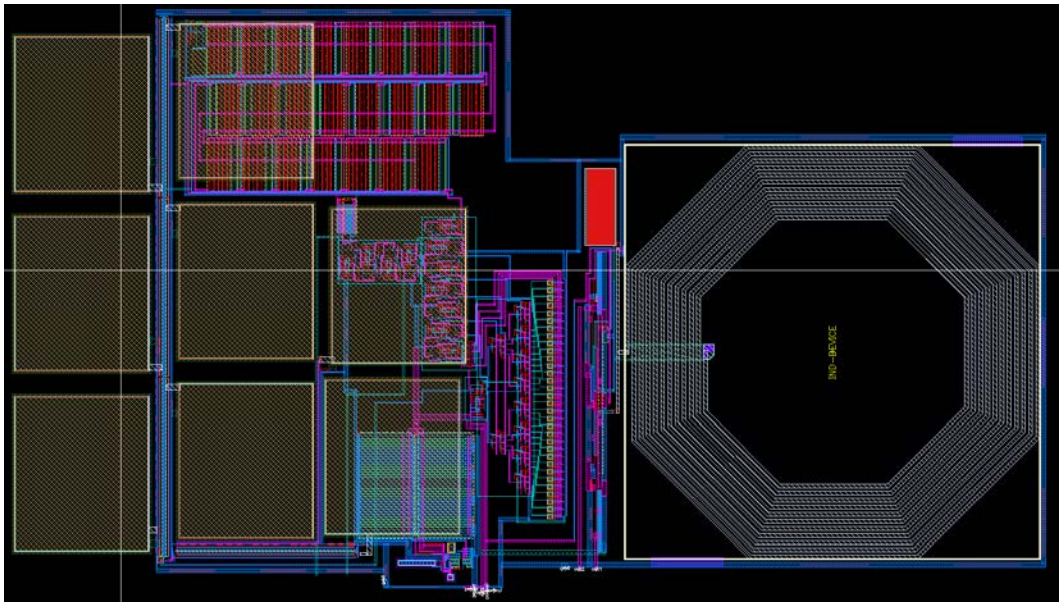

Figure 52: Design layout

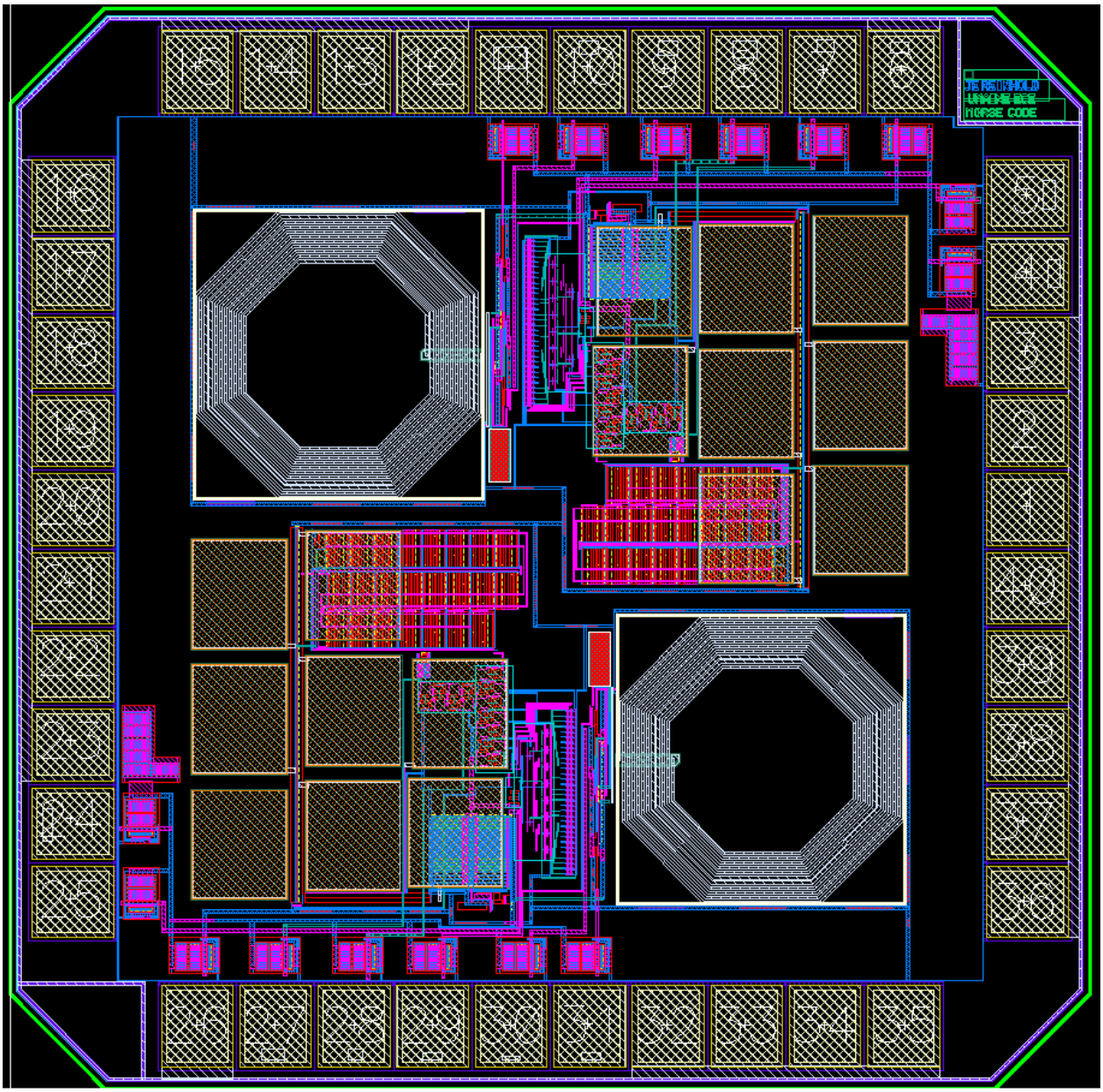

Figure 53: Full chip layout including two copies of the designed circuit

References

[1] Gray, Paul R.; Hurst, Paul J.; Lewis, Stephen H.; Meyer, Robert G. Analysis and Design of Analog Integrated Circuits, Fifth Edition. New Jersey: John Wiley & Sons, Inc. 2009.

[2] Maina, Anil K. Digital Electronics Principles, Devices, and Applications. New Jersey: John Wiley & Sons, Inc. 2007.