DIRECT DIGITAL SYNTHESIZER

Design of ROM

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AMBITION: A journey of thousand miles mostly ends well!

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Chapter 1

Introduction

1.1 Project Overview

Direct Digital Synthesizer (DDS) plays an important role in modern digital communications for sine wave generation. Direct Digital Frequency Synthesis has been recognized as a technology for generating highly accurate, frequency- agile (rapidly changeable frequency over a wide range) and low distortion output waveforms. At present, there are two principal forms of applications using DDS: waveform generation in *communications* and signal analysis in *industry and biomedicine[1]e*. The different components of a DDS are Accumulator, ROM and Digital to Analog converter. In this project, my design involves a 256 bit ROM which stores the sinusoidal values for DDS. It consists of four 6 to 2^6 bit tree decoders, four ROMs and 2:1 multiplexers. The multiplexers select the right ROM and their outputs are latched using D flip-flops. This ROM receives 8 bit input from a 12 bit, 50 MHz accumulator designed by Aravind Reghu. The latched outputs are then fed to a 10 bit Digital to Analog converter designed by Steve Fortune.



Fig 1.1 DDS guided by Prof.David Kotecki In ECE 547, Spring 2006

1.2 Objective

A DDS system generates one or more frequency from a single reference frequency using digital logic. In this project, my objective was to design a 256 bit ROM which stores the amplitude values for each phase of DDS output waveform. A 256 bit ROM could be designed by using four 64 bit ROMs which thereby minimizes the capacitance and also occupies less space on the chip.

1.3 Design Specifications

The different specifications that were given for the design of a ROM are as follows:

Name	Specification
Number of rows	256
Number of columns	9
Frequency	50 MHz
Voltage	0 to 5 V

Table 1.1 Design Specifications

1.4 Macros

MACRONUMBER	NAME
1	64 bit ROM A
2	64 bit ROM B
3	64 bit ROM C
4	64 bit ROM D
5	9 max_2 to1(2)
6	9 max_2 to 1 tall
7	ROM to DAC CONVERTER
8	DFLIPFLOP

Table 1.2 Macros

1.4 Pin Assignments

Supply net pins were assigned to the package pins with the greatest parasitic capacitance. This parasitic is actually beneficial since it provides additional bypass. Critical signals are assigned to the pins with the least parasitics. The pin assignments are listed in Table 1.3

PIN	PAD TYPE	NAME	DESCRIBTION
1	Padvdd	vdd	Vdd pin
2	Padio		
3	Padio		
4	Padio		
5	Padio		
6	padio		
7	Padio		
8	Padio		
9	Padio		
10	Padaref	out	Out pin
11	Padio	Clk	Clk pin
12	Padio		
13	Padio		
14	Padio	A4	4 th input from ACC
15	Padio	A5	5 th input from ACC
16	Padio	A6	6 th input from ACC
17	Padio	A7	7 th input from ACC
18	Padio	A8	8 th input from ACC
19	Padio	A9	9 th input from ACC
20	Padio	A10	10 th input from ACC
21	Padio	A11	11 ^h input from ACC
22	Padio	A3	3 rd input from ACC
23	Padio	A2	2 nd input from ACC
24	Padio	A1	1 st input from ACC
25	Padio	A0	0 input from ACC
26	Padio		
27	Padio		
28	Padio		
29	Padio		
30	Padio		
31	Padio		
32	Padio		
33	Padio		
34	Padio		
35	Padio		
36	Padio		
37	Padio		
38	Padio		
39	Padio		
40	Padgnd	Gnd	Gnd pin

Table 1.3 Pin Assignments

Chapter 2

Circuit Design

This chapter discusses the concept and design of the individual building blocks of the 256 bit ROM. The performance of each building block will determine the performance of the ROM and thus the ultimate performance of the DDS.

Blocks discussed in this chapter are:

- 1. 6 to 2^6 bit tree decoders
- 2. Four 64 bit ROMs
- 3. Sense Amplifiers
- 4. 2:1 Multiplexers
- 5. clocked D Latches

2.0 Description of Schematics

Refer to table 1.2 for all Macros used in this design. Refer to Appendix A for full size schematics of each cell.

2.1 6 to 2^6 bit tree decoders

The 256 bit ROM receives its 8 bit input from the pipelined 12 bit accumulator. The first 6 bits (starting from the LSB) are given to the line drivers. The line driver selects and drives only one line on the ROM. It uses the 6 to 2^6 bit tree decoder in which one of the 64 bit output is pulled high depending on the 6 bit address. On the output side of the selection lines, the line is tied to a pull-down NMOS and an offset inverter connected to a regular inverter. The gate of the pull-down NMOS is tied to the signal line so any 'high' floating lines are sufficiently pulled down. The offset inverter allows the real high signal to be accepted, since the NMOS will be trying to pull it low. The tree consists of NMOS pass gates, with the common end tied to VDD. The configuration of the tree is an expansion of the tree in [2] to allow for 6 inputs and 64 outputs. Figure 2.1 shows the zoomed in view of the tree decoder with 6 inputs.

	inbit<5>	inbit<4>	inbit<3>	inbit<2>	inbit<1>	inbit<0>						
	1 I 7 I I	📍			T	10 10 	8 (S 23) 			23, 29, 29, 29, 29 • 21, 40, 40, 40, 40, 40, 40, 40, 40, 40, 40		9. 38. 38 H. 14 44.
	_										n na na na na Na na na na na	
	LSB TreeInput	LSB TreeInput	LSB TreeInput	LSB TreeInput	LSB TreeInput	LSB TreeInput	14 14 14 14		er er er er fælge Killer er fælge fælge		e in se est	e e e
	10 10 <u>1</u>	जन्म हुत्		10 - 10 <u>-</u>	1 A 2	10 To _1	a a	8553333		10 N 14		1.1
8	LCD H	Bb an	LCD H		Å Å	LCD X	6 6			Pull Un	Pull Un	Pull Un
	LSD	LSB . 0	LSB. 0	Lap. 0	LSB	LSB						1 - 1 - F
	<u>m</u>				m	Outbor		🛛 In 🔹 Out 🖪	A<0>	Ward	Wand	Wind
	SJ. PodB	Bbar	Bbar -	Bbar	Bbar	-SB Bbar	10 (A) 14 (A)	Line		ROM. 1 H	ROM. 1 H	ROM. 1
5î	<u>-</u>	<u>ר</u> א י	S	- · · S	Outbar 9	in 🦉	14 14 1		A<1>	•	-	
	5 5 5 5 5 5	것 (전 전 전 전 전			Tree2nd	Tree1st	4 S.	Line	50.03.0	Word	Word	Word
				Outborl	ln							NOWL 1
	40 40 40	194 194 195	41.4	(A R) A	4 4 4	Outbor		In Dut	A<2>	1 A A	14.14.14	4.4
	10 10 10	56 St - 12	10.00.00	24 R R	133		ेव थ	Line	(araa)	Word	4.54	Wa
S2	2012	M H H	10 IZ IZ	52 57 av	A M G	Be	G 6			Bit2	Bit of a	12 22
2	22 22 28	N 13 13	M (M (M	81 B W	Out	In 역	10.00		A<3>			
1						Tree 1st		In Uut	10 10 10 10 10	Word		Wo
	41 - 41	194 194 - 49	40 G.	14 81 81	9 (9)	E R R	1.15	Line	14. AF 14. 14	£	¥	ж. э.
	AX 40 (4)	37-13 - 81	40 - 41 - 04	Tree3rd			- 54 - 18		4<45			
			10 10 10		8	Outbor		🖬 In 🕤 👘 Out 🛽	110.00	Word		Wo
		na na ku	1. I. I.	ta at as	17. 18	8		Line	an an ar na na	В	5	
	10 10 10 10 10 10		Outbarl	In	Outbar					- a		
	10 40 A	16 16 16		14 65 FG		Out	_	In · · · Out I	A<5>		10 10 E	·
	$k_{1}^{(1)}=k_{1}^{(1)}=0,$	(A. 19 - R)	$\Phi_{i}^{(1)}=\Phi_{i}^{(1)}=1/\Phi_{i}^{(2)}$	(A - R) (A)	Tree2nd	Tree1st	14 15	Line Line	4 9 9 9 9	word	10 10 B	ΨO
	410 - 40 10 - 10 - 10	17 18 E1	*: *	Out	■ln	10 AT 4	4 14	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1		Bitz	Bit	÷1 (+
		We had been	21.2.12	0.1	1992 - 17 - 12 1	Outhour		Tes Durk	A<6>		-	
25 +	5 5 5 5 5 5	28 년 원 28 29 29				Uutbar				Word		Wo
	10 AL 11		10 E 13		1.1	LSB SBbo			新 表 用 语 词	Bit2	BH1 as as	<u>4</u>] (†

Fig 2.1 Schematic of a Tree Decoder (Zoomed in view)

2.2 Four 64 bit ROMs

Figure 2.2.1 shows the pictorial representation of $2^6 \times 9$ ROM organization. The four 64 bit Read Only Memories are used to store bits in a structured manner. ROMs are nonvolatile; they retain their contents when power is removed. The mask programmed ROM's in this design use one transistor per bit whose presence or absence determines 0 or 1.

In a ROM every address specifies a preprogrammed output. In this design, NOR based ROM arrays are employed

Specifies 2⁶ unique data words



Fig 2.2.1 2⁶ x 9 ROM organization

Bit 0

This cell represents a zero bit in the ROM. It contains an NMOS that pulls the line low when it is active.

Bit 1

This cell represents a one bit in the ROM. Since the ROM lines are pulled high, this cell only contains wires to continue the ROM line

The tree decoder enables the selection of one of the 64 rows. Only the selected row is at logic"1" and all other rows are at logic "0". When this particular row has bit lines with Bit 0 or Bit 1 programmed in it, then the outputs go high or low accordingly.

NOR based ROM array

The design of the 64 bit ROM has a NOR based array as illustrated in figure 2.2.2. All word lines R_i are kept at logic "0" level, except the selected line is pulled up to "1" level.



Fig 2.2.2 NOR based ROM array

Programming of the ROM (Refer Appendix D)

Address of the ROM corresponds to the phase of the sine wave. The ROM contains a ¹/₄ stroke of a sine wave instead of a full stroke to save area. The output of the Accumulator is given

to a ROM pointer which helps the ROM to generate the sine wave. The ROM has the specification of 256 rows. This means that the amount of change per address is (90/256) = 0.3516 as shown in Fog 2.2.3. The starting point in degrees is (90/256)/2 = 0.1758. This sine of 0.1758 is the value which is stored in the first location. The next value that is stored in the ROM is sin $(0.1758 + (1x \ 0.3516))$. Thus the nth value stored is sin $(0.1758 + (n \ x \ 0.3516))$. The Matlab programming was used to calculate all the values in binary and all the values were normalized for better accuracy.



Fig 2.2.3 ROM Programming representation

2.3 Sense Amplifiers

A Sense Amplifier is an essential circuit in designing memory chips. Due to large arrays of cells, the resulting signal has a much lower voltage swing. To compensate for that swing, the output of the ROM is given to a sense amplifier which is used to amplify voltage coming out of the bit line. The schematic of the Sense Amplifier is shown in Fig 2.3.



Fig 2.3 Schematic diagram of the sense Amplifier

2.4 2:1 Multiplexers

Multiplexer is a device with multiple signal inputs, one of which is selected by separate address inputs to be sent to the single output. A multiplexer will have signal inputs, control input and output. They are used in building digital semiconductors such as CPUs and graphic controllers, and also in communications.

In this project, the selection of the four 64 bit ROMs is done using multiplexers. The MSB and the next most significant bit that are received from the accumulator act like control inputs for the multiplexers. The multiplexers are constructed using Transmission (TX) gates. The symbol for the multiplexer is as shown in Fig 2.4.1.The TX gates are particularly used for path selection. When the select signal is HIGH one input is passed and when it is LOW the other input is passed. The application of the transmission gate as the path selector can be used to implement multiplexers.



Fig 2.4.1 Symbol of 2:1 Multiplexer

Fig 2.4.2 represents a pictorial representation of the four 64 bit ROMs with multiplexers. The four 64 bit ROMs are marked as A, B, C and D. The 9 outputs from each of the ROMs A and B are given to nine 2:1 multiplexers connected in a parallel manner. Similarly, the 9 outputs from each of the ROMs C and D are given to another set of nine 2:1 multiplexers connected parallel to each other. The next most significant bit from the accumulator to the ROMs is used as the select line N for all the 2:1 multiplexers. This acts like a control input which selects (ROM A or ROM B) and (ROM C or ROM D). The MSB that is given to the ROM acts like the control input M which enables the selection of only one ROM at a time. Table 2.1 shows the selection of ROM based on input bits M and N.



Fig 2.4.2 Pictorial representation of 64 bit ROMs with multiplexers

Μ	Ν	Y(ROM selected)
0	0	D
0	1	С
1	0	В
1	1	А

Table 2.1 ROM selection based on input bits M and N

2.5 Clocked D Flip-flops

The outputs from the multiplexer are latched using clocked D flip-flops. The edge triggered D flip-flop can be easily constructed from the RS flip-flop. One essential point about the D flip-flop is that when the clock input falls to logic 0 and the outputs can change state, the Q output always takes on the state of the D input at the moment of the clock edge. This circuit has two D latches in a master- slave configuration driven by a clock. The different logic circuits used in this design are 2 inverters, 4 AND gates and 4 NOR gates. The sizing of the transistors was done for each of this digital logic. Fig 2.5.1 shows the schematic view of the D flip-flop used for latching.



Fig 2.5.1 Schematic view of D flip-flop

Chapter 3

Circuit Performance

Simulation results

3.1 Transmission Gate

The transmission gate has two transistors: one N channel transistor and one P channel transistor. Each one is capable of transmitting one of the levels accurately but neither device is capable of transmitting both high and low voltages. These two transistors are connected in parallel. The reason to use these two transistors is that they pass logic lows and logic highs. Transmission gates act as tristate buffers.

Fig 3.1.1 shows the test circuit of TX gate. When the select signal is high the output is high and when the select signal goes low the output goes low. The figure 3.1.2 demonstrates that the output is the same as the input when the transmission gate is enabled and that is it is floating when it is disabled.



Fig 3.1.1 Test circuit of Transmission gate



Fig 3.1.2 Output waveform of Transmission gate

The advantage of the CMOS transfer gate is that the degree of capacitive feedthrough is reduced. This is because it is clocked with the true and complement values of the enable signal.

3.2 2:1 Multiplexer

The 2:1 multiplexer is constructed using 2 Transmission gates (Fig 3.2.1). The idea of path selector can be used to implement multiplexers. Logically, the output of the path selector [3] can be written as

Z = AS + BSbar

When the selector signal S is high, A is passed to the output while a low on S passes B to the output. Fig 3.2.2shows the output waveform of 2:1 multiplexer.



Fig 3.2.1 Test Circuit of 2:1 Multiplexer



Fig 3.2.2 Output waveform of 2:1 multiplexer

3.3 Two input NAND gate

NAND gates consist of two parallel PMOS devices and two series NMOS devices. Test circuit of NAND gate is shown in Fig 3.2.1.Sizing the four transistors is based on achieving the same delay as the inverter when driving the same load capacitance under worst case input conditions [4]. All four devices in the NAND gate are 2W devices. When both the inputs A and B are high then the output of the NAND gate is zero. When both the inputs A and B are high or when one of the inputs is high, then the input is high. This could be proved by the simulation result in Fig 3.2.2.



Fig 3.3.1 Test circuit of 2 input NAND gate



Fig 3.2.2 Output waveform of NAND circuit

3.4 64 bit ROM

The 64 bit ROMs were tested (Fig 3.4.1) by giving the output of the accumulator to the input of the tree decoder. The test result was that the tree decoder helped the circuit to select the right row and the outputs were zero. The outputs were zero and one corresponding to that row. Fig 3.4.2, 3.4.3, 3.4.4 show the output waveforms of 64 bit ROM A, ROM B,ROM C, ROM D respectively. The outputs of the multiplexer 3 are latched and the waveform is shown in Fig 3.4.5.





Fig 3.4.2 Output waveform of 64 bit ROM A



Fig 3.4.3 Output waveform of 64 bit ROM B



Fig 3.4.4 Output waveform of 64 bit ROM C



Fig 3.4.5 Output waveform of 64 bit ROM D

3.4 Multiplexers

Fig 3.4.1 shows the overall ROM schematic. The outputs of ROM A and ROM B are given to multiplexer 1 and the in-bit 6 selects the ROM. Similarly the outputs of Rom C and ROM D are given to multiplexer 2 and the in-bit 6 selects the ROM. In bit 7 helps in the final Rom selection. The test results show that the multiplexers perform the correct selection of ROMs. Fig 3.4.2, 3.4.3, 3.4.4 show the output waveforms of multiplexers 1,2 and 3 respectively.



Fig 3.4.6 Overall circuit of 256 ROM



Fig 3.4.7 Output waveform of Multiplexer 1



Fig 3.4.8 Output waveform of Multiplexer 2



Fig 3.4.9 Output waveform of Multiplexer 3



Fig 3.4.10 Latched output waveform of 256 ROM

3.5 Sine Waveform

The overall chip circuit is shown in fig 3.5.1. The latched outputs of the ROM are given to the Digital to analog converter through a ROM to DAC converter. The output waveform was a sine wave but it had some glitches (Fig 3.5.2). When the circuit was tested with D flip-flops after the ROM to DAC converter, we obtained a pure sine waveform (Fig 3.5.3).



Fig 3.5.1 DDS overall circuit



Fig 3.5.2 Sine waveform with glitches



Fig 3.5.3 Sinewaveform of DDS circuit

Chapter 4

Physical Design

This chapter discusses the pin assignment, constraints and considerations taken into account while doing a layout and floor planning of the final chip.

4.1 Pin Assignment

The die size that was available for the current design was 0.153" x 0.133" and it was packaged as a 40 pin DIP. The physical design of the final chip and floor planning of the die can be found in Appendix B and Appendix C. Depending on the location some pins have higher parasitic impedance than others which has a negative effect on the signal transmission. Pins were assigned based on the sensitivity of the signals and electrical characteristic of the package used. Table 4.1 contains the electrical characteristic of the 40 pin DIP. For the pin assignment refer to Table 1.4 in Chapter 1. Pins with the lowest parasitic impedance were used for the critical signals, such as output input signals and clock, in order to minimize the noise that may be introduced by the pin trace.

Pin	R (ohm)	L (nH)	C (pF)	t _{of} (ps)
1,20,21,40	0.217	8.18	5.32	209
2,19,22,39	0.177	7.92	4.39	187
3,18,23,38	0.154	7.34	3.37	157
4,17,24,37	0.110	6.48	2.34	1213
5,16,25,36	0.103	5.69	2.16	111
6,15,26,35	0.0661	4.37	1.43	79.0
7,14,27,34	0.0646	4.54	1.48	81.9
8,13,28,33	0.0498	3.69	1.05	62.3
9,12,29,32	0.0378	3.54	0.863	55.3
10,11,30,31	0.0247	3.15	0.660	45.6

Table 4.1 Electrical Characteristic of 40 Pin DIP

4.2 Floorplanning Issues

The ROM occupies the major part of the DDS chip because of the numerous components. Since the ROM acts like the middle component, receiving its input from the accumulator and giving its output to the Digital to Analog converter, it was best to do the layout at the bottom rightmost corner of the chip. Metal 1 was used for all the VDD and GND connections and Metal 3 was used for the input, output and interconnections.

4.3 Component Layout and Outer Guard Ring

The overall chip size (layout area) was 900 x 900 microns of which the ROM alone measures 800 x 497 microns. In general, it was a goal to have the guard rings around cells and ample power connections. The layout of all components share some general characteristics like to reduce the cell size, minimize the noise and introduce large number of contacts. Multipliers and fingers were used wherever appropriate to help reduce the cell size. Ground (GND) and VDD rings were implemented to minimize the noise coupling between components. Also, to satisfy the design rules additional poly had to be added.
Chapter 5

Design Verification

5.1 Introduction

Physical design verification can be accomplished with two software checks: *Design Rule Checking (DRC)* and *Layout versus Schematics (LVS)*. DRC verifies that the layout does not violate a manufacturing rules and LVS verifies that the physical layout logically matches the schematic in the number of terminals, components, component sizes and interconnection. After the DRC is done for the layout, it is extracted and then succeeded by LVS. After design and layout verification, the analog extracted schematics could be created to verify the circuit performance with parasitics included.

5.2 Design Rule Verification (DRC)

DRC and *LVS* were performed on the individual components before running verification on the circuit level and finally on the top-level layout (complete chip). Top-level layout was *DRC* clean, meaning there were no errors. DRC could be performed in an incremental or full manner.

			DRC	
ок	Cancel D	efaults Ap	ly	Help
Checkin	ng Method	🔶 flat	◇ hierarchical ◇ hier w/o optim	vization
Checkin	ng Limit	🔶 full	\diamond incremental \diamond by area	
		Coordi	1210	Sel by Cursor
Switch	Names		Ι	Set Switches
Run-Sp	ecific Comm	and File		
Inclusio	on Limit		1000	
Join Net	ts With Same	Name		
Echo Co	ommands			
Rules F	ile		divaDRC.rulį	
Rules L	ibrary		U_TechLib_ami06	
Machin	e		🔶 local 🔷 remote 🛛 Mach	ine I.
				1

5.3 Layout versus Schematics Check (LVS)

LVS verifies that the physical layout logically matches schematics. As mentioned before, *LVS* verification was performed on the individual components before running top-level layout verification.

		LVS		
Commands				Help ;
Run Directory	rađ			Browse
Create Netlist	E schemati	ic 📕 (extracted	
Library	ROM		ROM	
Cell	256R0M_R	2Dtemp <u>í</u>	256R0M_R2	Dtemp
View	schemati	đ	extracted	L
	Browse	Sel by Cursor	Browse	Sel by Cursor
Rules File	divaLVS.	rulį	- **	Browse
Rules Library	ROM ROM			
LVS Options	Rewiring	. 📕	Device Fixing	
	Create C	ross Reference 🔳	Terminals	
Correspondence F	ile 💷	r/grads/ece547	/lvs_corr_	file Create
Correspondence F Switch Names	ile 🗆 🛙	r/grads/ece547	/l v s_corr_	file Create
Correspondence F Switch Names		r/grads/ece547	/lvs_corr_	file Create
Correspondence F Switch Names Priority	ile]	r/grads/ece547 al — I	/lvs_corr_	file Create
Correspondence F Switch Names Priority 0. Run	ile	c/grads/ece547 :al — Å. Error Display	/lvs_corr_	file Create

Once the LVS has succeeded the output could be seen from the Ouput button else we can open the Error display button.

Analys	is Job Succeeded	
Job '/usr/grads/ece547/LWS' that was	started at 'May 11 19:14:56 2006' has :	succeeded
ок	Cancel	Help

The Top- level layout of the circuit design does pass LVS.

		/usr/grads/ece547/LVS/si.out	1	1
File		Help	26	
@(#)\$CDS: LV5	§ version 5.	0.0 08/17/2004 08:35 (intelibm12) \$	-	1.2
Command line	/home/cade	ence/ic5033usr3/tools.lnx86/dfII/bin/32bit/LVS -dir /usr/grads/ece547/LVS -l -s -f -t /usr/grads/ece547/LVS/layou	t,	
Like matching	y is enabled	a.		
Net swapping	is enabled.			
Fixed device	checking is	s enabled.		
Using termina	al names as	correspondence points.		
Net-list	summary for	r /usr/grads/ece547/LWS/layout/netlist		
count	Secondaria Com			
1488		nets		
22		terminals		
999		pmos		
2756		TUNOS CONTRACTOR OF C		
Net-list	summary for	/ /ner/mrade/ene547/LVS/schematic/matlist		
count	Scalatory 101			
1488		nets		
22		terminals		
aaa				
2756		pinos		
-				-
Terminal	corresponde	ance points		
NO27 NO00	NOZ	IR(0) Test		
N9ZU MI4E	N93 NCO			
N145 N000	NOZ			
N229 NC00	N40 N70			
N047	M10			
ME22	M00			
MODO MOEO	N77			
N020	MEC			
MOE7	MOG			
M120	M/0			
M302	M20			
M720	M86			
N1357	N63			
N175	N85			
N1214	N22			
N111	N24			
N1052	N40			
N1436	N48	0ut(9)		
N669	N32	clk		
N554	NI	and		
N730	NO	vdd!		
The net-lists	s match.			
for get				
S			12	

File N669 N32 clk N554 N1 gnd! N730 NO vdd! The net-lists match. layout schematic instances un-matched 0 0 rewired 0 0 0 0 0 3755 375 375 375 size errors pruned active 3755 3755 total nets 0 0 un-matched 0 merged 0 pruned 0 0 1488 active 1488 total 1488 1488 terminals 0 un-matched 0 matched but different type 0 0 22 22 total Probe files from /usr/grads/ece547/LVS/schematic devbad.out: netbad.out: mergenet.out: termbad.out: prunenet.out: prunedev.out: audit.out: Probe files from /usr/grads/ece547/LVS/layout devbad.out: netbad.out: mergenet.out: termbad.out: prunenet.out: prunedev.out: audit.out:

Chapter 6

Conclusion

Thus the 256 bit ROM was designed and tested. The separation of 256 ROM into four 64 bit ROMs saved a lot of space and also reduced capacitance. The tree decoder enabled the selection of only one of the 64 rows. The multiplexers were first designed with NAND gates and it was found that there was better performance using Transmission gates. The D latches at the output of the ROM enabled us to obtain an edge triggered output. From the simulation it was found that placing the ROM to DAC converter after the D latches produced a sine waveform with glitches. However, the glitches could be removed when the output of the ROM to DAC converter is latched. The designed ROM met all the necessary specifications: 256 rows, 9 columns, 50 MHz frequency and a voltage range of 0 to 5 Volts. The overall layout of the DDS also met the size requirements. The entire schematic, symbol and layout of the chip are in APPENDIX C.

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Bibliography

- [1] http://www.analog.com/library/analogDialogue/archives/30-3/single_chip.html
- [2] "Class D Audio Amplifier Front End circuit" Wayne Slade, Steven Turner, 2002
- [3] CMOS circuits, Jacob Baker

[4]

http://www.eecg.toronto.edu/~roman/teaching/1388/2004/finalProj/2004_ECE1388_FP_www/Quadrature_Direct_Digital_Synthesizer/index.html

APPENDIX A

SCHEMATICS



Fig A.1 Inverter Schematic



Fig A.2 Transmission Gate

33	347	1. 3		- 12	389	13	<u>a</u> . 8	105	83	10	68	8	38 3	_×.	8 8	8 84	35	83	35	13	82 ÷	8 8	2	ł3	15	63	88	83	55	33
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100	334	16 IS	31	10	381	18	8	: :8	83	38	83	38	38 3	1 30		6 34	162	34	162	10		8.8	6	88	38	83	58	83	58	33
	33	12 12	84	133	84	18		2 193	20	82	20	84	88 8	6	0	ž 25	12	24	12	18		8 8	ŝ.	12	83	23	82	20	33	88
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	- 88 - 88	- 98 - 89 - 143 - 62	- 98° - 87	- 56	2.0	58 55		1 939 1 932	350	439 912	380		02 2	C (8)	088. 1951			28 60	198	88 36				503 516	435 642	390	435 932	250	439 942	00
	104	145 DS			-		· ·	0.02	200				TX.	_gate	9			04										¥1.7		
100	34	A		10	98) 199	10	8	8	8	-	8	- 1	a a		hut	34		38	ΞĘ.	10	18. ÷	8 3	-	15	88	82	88	82	8	88
2	85	3	-	13	35	53	2	88	<u>\$</u> 2	S.	<u>8</u> 2	1	38 8	1 2/	3	85		83	10	53	5 5	8 8	8	33	83	52	88	<u>8</u> 2	83	58
80	34	36 B	100	15	(#)	88	8	8	82	88	¥2		88 8		98	34	ж)	34	3Đ	15	a i	e s	8	12	8	82	88	82	8	83
23	85	8.8	15	53	35	2	8	88	<u>8</u> 2	88	22		26 8	8.	1	8 8	12	83	33	:2	s :	8 8	8	33	83	52	88	<u>8</u> 2	88	58
80	34	8 3	10	10	(á)	83	8	8	82	8	82	38	29 9	1 20	S	8 34	80	34	85	÷S.	a i	8 B	8	83	8	82	8	82	8	8
33	3.27	ac 13	28	12	28	12		5 28	25	23	58	82	a: 8			8 33	22	33	20	12		2 2	8	22	:::::::::::::::::::::::::::::::::::::::	58	23	25	18	83
12	84	12 13	- Gi	- 23	<u>.</u>	23			10		100	39		•	30	2 24	- 22	84	22	12		3 8		22	10	125	22	100	10	28
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æ	84	142 U		23	55	83	-	18	85	15	85	-33	71 2		8	8 84	22	84	22	43	98 ÷	8 8	•	-			-		Ou	rt
33 83	34 33			18 193	93 20	88 52	8 2		85 85	15 20	85 85	39 28				8 34 8 33	22 23	84 33	22 23	22 23	99 - 1 28 - 1	8 8 8 8	•	2	×	85	9		Ou o	rt S
12 N N	34 22 23				94 75 75		8 8 2		22 22 22 23	5 C	22 22 23	38 22 23			100	8 84 N 33 Z 33		34 32 33	22 22 22				•	12	3	25 25	9 0		Ou o	nt S
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Fig A.3 Transmission Gate



Fig A.4 9mux_2to1

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83	88	28	32	122	8	3	13	\sim	35	82	88	35	22	122	35. 22	3	2	0	33	83	25	33	10	52	8	3
8	15	98) 199	Зł	88	10	8	12	8	98) 199	31	16	98) 1	38	8	12	8	vd	ď	35	31	15	25	38. 	39	12	8
20	883	32	38 8	88	93.	\sim	85	¢.	32	20	285	32	100	88	32	1		Ø	32	33	385	32	38 28	88	82	12
8	N) 4		8	58	25		12	58	8	8	50	8	85		.ve in 1	1d!	ami	Ø6P	ŝ	82	50 10	8	85	58	8	88
84	8		3	48	12	T	48	21	98	84	85	98	3	48	not	15	=(m:	500 1	In	83 84	88 88	а 9	38 38	80 42	а 22	
-	20	14	82	87	22		33	28	82	25	20	82	62		net	15	M1 ami	Ø6P	36	85	20	82	82	137	12	83
in	2		-											_	-0		W=	6u	10	84	83	82	-58	13	25	10
34	10	(9)	28	15	8		8	8	18) 		12	(á)	94	18	° c	out	lm:	1	ni.	34	ĸ	<u>1</u> 20		10	- Ne	8
25	220	32	8	8 8	92		18	6	. (out	J ^M 4	I IØEN	38	10		ut	M3	ØEN	33	23	28	32			ų	12
83	85	20	88	8	8	1		-			W =	= 1.5	วัน ชัต	2			W=	1.5	Su-	82	88	33	38	52	8	3
31	ß	9	38.	88	10	8	88	8	qr	nd]		1	ng.	18	ġr	ndl	l m:	1 1	ui.	31	15	<u>æ</u>	ай.	18	10	8
20	22	22	100	1 22	92	2	88	\$2		24	¥8	38	22	£5	Ĩ.	2	gn	d	32	84	28	32	100	88	92	12
81	10	35	82	53	3	83	12	58	35	83	52	35	1	12	20	~	5	86	35	8	59	20	82	53	2	83
89	83	82	-88	t 8	85	15	5 3	38	82	84	83	82	153	8 8	35	10	68	38	8	84	83	82	-81	12	85	
84	85	98	-29	48	22	15	R 8	20	98	84	8	88	3	¥8	18	25	#8	25	98	84	85	98	-39	48	22	15
25	12	125	82	137	22	22	25	88	123	25	23	123	82	137	57	82	137	88	12	25	23	12	532	23	12	83

Fig A.5 NOR gate





35	88	15	385	18	30	81	10	38	33	38	85	88	18	35	31	10	31	38	38	35	88	85	25	:0	10	31	30	38	88	88	35	88	18	38
20	83	20	14	33	22	21	12	82	88	82	20	83	33	14	25	22	81	-	-	10	22	20	6	33	12	21	22	62	88	83	20	83	33	121
85	88	8	191	18		31	10	аł	33	88	85	88	12	3	31		31	33		vdd	-	15	35	10	152	31	(1)	38	88	88	ŝ	88	8	191
28	\sim	22	32	83	92	22	92	33	\$2	12	28	\sim	185	32	22	92	22	-		28	2	28	32	88	32	23	32	22	\$2	12	25	\sim	83	32
83	10	83	82	13	25	84	33	-58	32	85	83:	85	63	32	83	25	83	32		88	10	83	82	63	33	23	35	:58	32	85	83	10	53	82
8	12	15	55	13	32	84	32	33	25	12	8	15	18	F				-							1	23	32	39	25	82	8	12	18	12
88	3	88	33	22	83	83	8	32	~	3	25	3	12		- 51	8	83	20	184	28	3	88	28	120		32	83	32	8	3	25	3	12	38
8	1	8	55	23	32	84	32	-	23	22	8	12	vdd	!	MØ		84	25	-39	85	22	85	9.0	vdd	1	M1	-	-39	25	82	8	12	Ŕŝ	38
53	83	22	35	33	3	85	3	12	1			in2	dſ	. 1	w=3	ын Ц	_					_	in i			w=3	U.	12	58	83	53	82	33	35
83	8	82	39	83	8	34	10	38		88	82	88	ÀU.		=6§ π:1	0Øn	34	33	-	82	8	82	ġŔ;	out	٦	l=60 m:1	Øп	-	8	8	82	8	83	(18)
20	83	20	14	33	22	25	12	82		82	20	83	····	T	1	12	22	88	82	10	22	20	12		T	1	22	62	88	82	20	83	33	52
85	88	ŝŝ	195	10		31	52	З¥.		88	85	88	18		31	13	31	33	38	15	88	16	35	18		31	()	3k	88	88	15	-		18
20	82	20	121	33	12	25	22	62		83	20	83	18		24	2	24	- 83	14	280	83	8	32	185		24	12	34	83	-88	10		2.9	>ųt
82	12	82	32	13	25	83	33	18		35	83	25	53	82	83	18	24	30	2	12.	35	83	32	13	33	62	33	:58	32	25	83	15	53	58
28	\sim	28	32	88	32	22	92	22		22	28	\sim	88	33	22	22	83. 84		out	MZ	Meh	28	32	88	32	22	32	22	\$3	22	23	\sim	83	32
in	1-		-						+							-		nı	18	W=	=30	18	22	13	33	8	33	:58	32	85	83	10	53	32
8		1	55	13	32	84	32	3		22	85	35	43	35	84	32	84	'ne	et6	l= m;	1	Π.	55	48	32	84	32	3	25	22	8	12	10	38
88	3	85	38	12	8	83	8	32		3	88	3	153	38	82	8	83	2		18	3	88	33	58	8	83	85	32	¢	3	85	3	12	38
82	8	82	(9)	83	λį.	34	80	38		8	83	8	10	(9);	34	λį.	3	8	-	8	8	82	(á)	15	ιų.	3	80	38	83	8	82	8	83	16
53	83	<u>8</u> 2	35	33	3	85	10	85		83	52	83	53	1	83	25	83	\$ 8	9.5	12	88	<u>8</u> 2	35	52	12	85	1	85	53	83	ல	83	33	35
83	8	8	(\$);	13		34	8	38		88	82	88	10	(á)	24	λį.	24	Dé	ate	M7	8	82	39.	88	80	34	λį.	-	8	88	82	8	83	(4)
20				33	12	84	22	84		22	20	83	23	22	24	22	-1	n2	1	am	IØ6N	23	6	33	12	38	12	82	88	83	20	83	33	1
8	nz.	-	4	18	10	34	-52	38		-	35	-	-	2	31	10	81	83		=	600	n	95	10		31	÷0	аł	8	88	8	88	13	19
28	\sim	222	32	88	92	22	92	38	\$2	22	28	12	88	32	22	92	22	gr	nd!	m:	1	an Và	33	85	32	23	32	32	\$2	2	22	\sim	88	32
83	10	83	82	53	35	84	35	:58	33	85	88;	15	63	82	84	25	84	33	-33	88	10	83	32	13	35	84	35	-58	32	15	83	10	53	82
282	2	22	32	88	32	22	82	33	\$2	22	28	2	83	32	23	82	22	\$2	38- 1	122	2	285	32	85	82	23	32	33	\$3	12	28	12	83	32
88	3	88	33	12	83	83	8	32	~	3	88	3	18	38	83	8	33	8	94	.gr	ıd.	88	10	58	8	83	8	22	0	3	85	3	12	38
005	22	22	22	43	32	84	32	39	23	22	82	32	43	35	84	32	84	33	7	7.	25	8	53	43	32	84	32	39	25	22	83	22	43	525

Fig A.7 NAND gate

1	22	18.75	1. 1	2.04	- 93	12	14	\$ 64	-92	- 287					20.2	1. 64	88	- 4	1.1	22	1876
92	2	D<Ø>		-	_		an.	_	-		DACK	Dillotion		·0	-	6		-D	< <u>€</u> < <u>8</u>	20	•238
33	×.	200	elk			1	1		-		alk ::	- Nurkneb	1	bar -		100	35		0.00	20	100
-28	365	P.25.6.	13-27	66254	385	- 53	28	1234	36	181					15-28	1054	365	P	1.121	345	•
	1				1	1	3		8	10			10	0.0	10		8			2	
-		10.02	18-04	10101	32		05	\$805	141	101				-	16.91	4804	12	1000	1000	- 28	1002
		D<1>	-			1	~		-	_	Ö	the standards		0	-		_	-0	B<10		
2			10	100.04	345		-	_	-	_	cik -	Dfliptlop	. 6	bar -		1.154	86	. 7		343	
-88	13	535	12-33	1923	35	68	3	127		-5	11202	-	-		8.9	1000	8	535		23	535
25	38	10.02	2635	922	22	23	85	\$2.24	22	235	2 (2005)	SE 2002 200	5 99	24 - 92	2638	\$222	22	10.02	\$2535	98	1992
82	1	10.05	15-21	10.0	12	*	<u>8</u>	80.54	8	:63	6 8632	R FOR RO	1 3	158 BF	16-21	80.54	8	· 38	86.53	12	• (K
	2	na	R	1998	10	1	10	80.85	-	101	Desco	1.2 29.07 00.0	0 100	-0	1001	2015	30	-	0-0	3	100
100		0.27	1	2000	- 00				-		clk	Dflipflop		bar		and.	~				1000
99	4	1.00		1.4	2	100	22	\$2.Q	a.	18	ALANC -CO	05 10003 823	0 100		100	\$	2	1.12		12	
38			53	10.0	æ	*	28	80.0	Æ	123	6 8638	1. 1. 1. 1. 1.	1 6	(e 18)	52	80.54	æ	•	8638	33	
292	2		10.1		14	2	82		4	38/2	3 30.0	10 1876 P.S	2 12	26. SC	10.04		66			2	
22	÷2	1000	2	100	98) (19)	*	2	8639	8	-87	14			100	1001	1000	<u>ж</u>	-	100	100	•238
33	Š	₽ <3≽		18-19	- 551	8				5	D	Dflipflop				200.0	931		0<3	2	300
			42-54	542.004			1				CIR	discontration and a second		insur				1000	10.000	æ	
3					8	1	3		8	20	10%3	16 18/3 800	i (s	83. W			8	1			
-	R)	-038	10.00	40.4	(a)	×	2	8839	民	-03	100	R 838 RS	i i	29 BR	10.03	8003	(R)	100	8008	20	
15	2	1232	17.05	203	35	1	13	5033	8	123					455.8	2033	3	-	2012	23	3233
38	*	D<4>		_	-	-			-	-	D	Dilinition		-0-		4		-D	0<4	2	•
8	100	1	10.00	23	8	1		10000	-	-	cik 3		5 5	Ibar -			8			100	
		20.02		10000	200	0			200	2010	2 9000	10 2012 201		105 107	22.00	0000	22	20102	0.000	125	2000
028 1. A		1000		10000			22				s coros. • auna	105 50000 2002 100 10005 2002	2 (2) 2 (2)		10002	00000					
					20		2				5 0508	12 8385 2.0	N V9				2			2	
32	2	D<5>	-	_	_	- 53		_	-		0	Dilletter	1.3	·Q-	-	-		->	0<5	>	200
23	80	15.92	18995	322	a.	1	-		-	-	clk -	nuhuch	. 6	bar -		ana.	à	1994	2000	120	1992
	1	•	53	3.1	8	1	8		P.	1	1000	1.5 5552 1003	1 64	0. 0	100		8	•		13	•
0.5	- 23	2002	2005	4504	100		105	6206	50	2655	2 6395			04 14 04 18	2003	6806	55	2002	60.05	æ	2002
		10000	*****		545. 104	0				1000	5 0000				100.00	200-02 200-02	200	10.000			*****
33		D<6>	D-	0500	- 20	1	50 E	7808	-8		D	10 AN 10 A	8 143	-0-	-	March .	- 222	-0	0<6	5.	
33	145	•	1.5	10000	38		-	_	-	-	elk ::	Urliptiop	. 0	bar -	0	1000	8	. 7		18	• 35
22	2	18/12	1007	200			64		4	101				_	2002	. S.	14	1975	1.14	22	18/15
22	Ŕ	10.08	1002	1134	198. 1	*	22	80.39	<u>1</u> 8	•83)	8 8838	N 608 80	8 8	23 K	1000	80.35	ЭR.	10.08	8008	展	•238
	3				8	1		223	8		2802	NE 5268 400	4 (S	18 A.	100		8			3	
	140	Dr7>				1.	~			-				.0	10	1000			Re T	-	
32	4	1.0	. .	923	32	1	-		-	- 2	clk	Dflipflop	. 0	bar		200	22	. 7	0.00		
38		1008	638	1.1	18	100	1	8000	10	-61	805		- 67		-	8839	18	10.08	8658	1	
15	2	5232	500 B	201	35	10	1	9//8	3	128	3 36 8	N 1948 AM	1 12	81 K	100 A	5033	3	5288	503	12	5283
28	æ	P	15-27	883 F	345	-	8	1354	36	13		N 101 102	8 243	34 M	13-28	1.54	36	P		345	•
33	8	0.00	-	983	10	1	88	200	2	14	DOM:	0.500 103	1 0		1524	4553	88	-		3	100
38		or as	-		10				-		r.k	Dflipflop		har		1.000	84	2	aco.	-	1010
1	3	1		32	88	1	1	8876	1		Sent A	-34 H-40 8102		and t	100		8			3	1
-	÷.	-038	1000	100	19. 19.	*	×.	80.34	族	100	10:08	R 1098 109	i i	134 BR	1000	8039	族	1008	8005	R	
38	8	1235	898	353	35	3	18	153	35	:23	a	8 130 133	8	52 18	858	0.53	35	1200	<u>a 23</u>	1	120
38	243	-		38534	36	13	28	1.54	345	Pica -	-				15-27	2054	36		1.1	385	P-234
	*	0<9>		1000	60	1			2	- 3	D	Dflipflop		2		2002	164		0<9	2	100
05		10.02	1000	4804	10	20		\$805		169	CIK .			ioar -		Seco.	10	1000	60.05	48	1000
		50115	1001			- 20	0.4	0,000		5000		a		102 12	1001	0.000	100	10110	0.000		10100

Fig A.8 10 DFF



Fig A.9 Tree first schematic

ł	8	32		55	3		88	12	38	32	23	88	Ë	5	3		88	12	88		22	38	95	8	59	38	88	8	88	
	22	82	25	88	33	35	¢2	12	3	in	52	33	A	88	33	35	<u>#</u>	12	2	20	52	32	35	88	33	3	<u>#</u>	52	3	20
	1	84	125	88	25	121	88	10	83	τη.	23	84	5	¥8	25	363	88	32	83	121	33	84	121	¥9	25	83	88	22	89	12
ł	£	98	40	83	39	52	88	83	88		83	22	-	8	3	14	88	83	88	35	83	38		83	39	98	88	83	38	R
;	88	3	98	63	84	342	**	-		Y	In		Y	63	24	342	16	•8	15	98	58	-53	347	68:	82	85	32	12	10	(4)
	12	84	28	10	25	164	In		\geq		- 5	14		10	1.		In	N	12		10	89	141	10	25	83	88	10	83	12
	13	-	142	8	84	88	30	23	1		83	-22			LS	Bbar	4	. M	miØ8 /=1	รุณ .5ป	23	-	88	8	84	15	20	23	15	143
ł	8	38	10	_		-31	88	12	38		-	88		154	Tre	eoud	114 than	11	=60 n:1	lØn-	Tre	00	utt	ar				10	88	5
	38	18	12	10		dd.	58	13	8		22	25		82	82		.D.G.I	1		33	12	18	35	<u>8</u> 7	-	2,8	Juti	pai		3
	ŝŝ	33	88	8	28	22	42	88	32		88	38 28		22	Tre	eout	tbar	h	14		85	33	22	23	34	82	10	85	32	38
ł	8	38		55	31	8	88	18	88	+	_	-	+		_	LSB		. M	/=1	.5u	10	38	8	85	31	38	88	12	88	
	22	22	20	85	33	25	<i>1</i> 2	12	3		22	35		88	33		ہـــا! المأمر	1	=60 n:1	10n	52	32	38	88	33	1	<i>\$</i> 2	12	33	20
1	11	84	125	21	12	121	88	10	12		33	84		¥8	25				and	121	33	89	121	¥8	12	83	88	18	89	12
	88	38	$\left \mathbf{k} \right $	10	.91	nd.	88	10	88		-83	-		83	3	19		5	gna	ξį.	83	93	8	8	39	88	88	10	88	30
	8	-88	28		7.	34		53			:8	:58		83	88	(*)	31	-3		18	53	18	89	88	88	10	33	53		98
	38	88	10	<u>83</u>	83	15	88	13	8		12	5.1		<u>8</u> 2	83	15	3		13	10	53	88	35	<u>8</u> 3	82	83	88	13	88	12
	13	33	348	8	84	846	35	18	1		12	1		8	3		In	JN		ENI	73	33	345	8	84	12	33	88	12	36
	8	38		15	3	25	88	18	88	-			+		_	LSB		. M	/=1	.50	18	31	85	15	38	38	88	12	38	33
	38	10	20	53	82	350	88	13	88	10	53	88		52	85	Tree	Pul		= 6¥ n:1	pip	ree	eou	t.	<u>8</u> 2	F	1		53	88	12
	88	33	98	25	33	\mathbb{R}^{2}	\$2	88	32	98	85	23		28	23			T	12	32	33	<u>"</u> *	N.	28	8	2.5	Jut	85	32	38
ł	83	98	ξį.	18	3	9 2	88	15	18	35	83	38		83	10	Tree	out		15 mi@P	N	83	98		83	13	98	88	13	88	30
	2	22	8	85	33	35	<u>1</u>	52	3	8	83	32	-		LO	BDur	-	W	/=1	.5u	22	33	35	88	33	3	<u>#</u>	12	3	20
	12	84	125	¥8	25	161	88	10	83	121	23	84	121	¥8	25		ہا! المور	1	= 68 n:1	10n	18	84	125	¥9	25	83	88	10	89	12
ł	8	38	40	83	3	(R)	88	83	38	45	83	98	(R)	8	3	(R)	11.44	T	ind	3Q	83	98	(R)	83	3	98	89	10	38	R
	8	-8	28	8	33	342	33	13	15	25	53	3	312	8	88	35		5	and a	18	53	8	34	83	83	15	33	53	15	983
,		a.	95	52	32	372	50	88	82	35	53	:1	372	52	82	32	33	133	12	35	53	3	32	52	32	122	50	55	12	.05

Fig A.10 Tree 4 th schematic



Fig A.11 Tree line schematic

8		SS	22	35	8	88 8	53	50	2	35	<u>1</u>	88	SS	12	35
ÿ	L	SB			_					-	28	80	25	84	14
8		84	32	12	88	88	85	88	1	32	49	28	38	38 8	N
3		24	95	<u>9</u>	ΞĮ.	82	85	84	98	18. .	1	82	24	99	8
ŝ		8	32	85	5	ß	-	31	88		88	ŝ	8	38	1
ő		88	-8	81	10	88	18	8	11 H		31	8	9 1	-58	35
ż		83	82	15	10	<u>8</u> 2	13	1	13	×		<u>8</u> 2	81	/	35
i		85	84	121	121	¥3	18	. \	83	÷t		80	./	894	14
8		84	37	84	94Ŝ	8	88	84	1	Ne		/		-29	88
8		8	95	(R)		12	15	8	. /		. /		8	93	8
ð		84	-83	81	25	88.	62	81	12	V	/	83	84	-58	81
8		89	35	8	8	88	52	32	æ	C)	85	38	12	25
ż		82	88	35	10	<u>8</u> 2	101	8		Dut	<u>88</u>	<u>8</u> 3	82	9.6	\$
8		84	2	22	38	88	88	88	32 A	۲ <u> </u>	100 1	22	84	28	N
8		89	-	84	343	63	88	84	ist.	F	ľ	8	8	-29	88
ŝ		8	32	10	11	15	88	8	88			15	8	8t	10
8		88	-88	8	28	8	52	84	11	200		681	S.	-58	81
ż		82	5.6	171		<u>10</u>	53	8	83	· a	·.	<u>8</u> 2	82	10	35
ÿ		25	84	12	12	¥3	10	24	83	14	-28	¥8	84	84	141

Fig A.12 Tree input schematic



Fig A13 Sense amplifier schematic

APPENDIX B

LAYOUT



Fig B.1 Inverter Layout



Fig B.2 Tx gate layout



Fig B.3 Mux_2to1





Fig B.5 NAND gate layout



Fig B.6 NOR layout











Fig. B.10 64 bit ROM layout

2.8	201	83	19	- 25	12	88	<u>8</u> 2	<u>80</u>	10	83	83	98	83	-25	191	121	88	88	85	38	18	83	10	1	88	357	12	5
84	88	88	15	15	12	53	<u>8</u> 2	<u>8</u> 2		- Gran							38	53	<u>8</u> 2	53	53	85	88	88	88	35	(2)	đ
84	84	83	121	161	121	88	¥8	¥8					41	J			23	88	¥6	53	23	25	14	83	89	949	151	2
22	33	2	10	1	92	\$2	22	38	-								\$2	\$2	38	88	88	88	23	2	32	22	88	11
-39	3	12	54	36	16	20	15	85	22		•		22	345	345	343 1	23	21	85	18	13	84	33	12	15	34	94Ê	
-39	3	12	54	12	38	20	87	85	- 6						7777X		20	20	15	78	23	84	33	92	15	38	145	1
98	95	88	19	192	20	88	82	182	-				-				80	88	182	85	85	34	99	98	88	88	3Ú	1
38	32	38				88	15	15									88	88	15	10	10	3	8	38	58	10		1
32	32	88		15		88	55	15	-			T					88	88	15	10	10	3	82	88	38			1
-88	-33	15	34	347	16	20	68.	83	-								20	20	83	52	63	88	-33	15	15	89	98	A.
28	22	2	10	85	20	20	85	85	2			X/A					20	<u>@</u>	182	52	52	83	83	82	2	25	20	110
88	1	88	8	15	10	\$ %	<u>8</u> 2	<u>8</u> 2	3			V					9%	93	<u>8</u> 3	53	53	83	88	88	88	35	(2)	5
84	88	83	15	$ \mathcal{T} $	10	53	<u>8</u> 2	<u>8</u> 3	3			V.					58	53	<u>8</u> 3	53	53	83	88	88	88	357	12	đ
84	84	83	121	121	125	83	¥8	¥8	2			¥					83	88	¥8	22	20	25	84	83	83	94) 	151	2
23	33	2	22	22	32	\$2	38	38									\$2	\$2	38	88	88	83	28	32	32	22	88	12
28	33	2	N	5	82	\$2	35	28	12) 12	23	22	28	1	S.			\$2	\$2	18	88	88	88	23	55	3	N	38	201
-39	3	14	88	98	ж.	20	83	85	28	8	88	-39	22	346			20	21	85	18	13	84	33	12	12	86	348	10
38	98	88	<u>19</u>	(á)		88	82	18	83	3	29	- 25	88	(R)			88	88	8	88	85	3	9ž	98	98	99) 	-R	10
38	8	58		18		88	15	15	10	31	31	33	58	18		i i	88	88	15	83	10	31	32	38	88			N.
88	8	38		18		88	15	15	10	3	31	32	88	18		i i	88	88	15	10	10	8	8	38	88			20
:88	8	10	35	35	25	31	83	68:	58	8	88	188	10	88			31	31	10	53	53	88	18	35	85	35	25	20
32	22	2	35	35	8	<u>#</u>	25	85	53	33	32	32	2	35			<u>#</u>	\sim	25	52	52	8	22	2	2	25	8	7.00
22	12	2	35	35	8	<u>\$</u> 2	88	88	\$2	33	33	32	22	35			\sim	<u>#</u>	88	82	82	33	8	2	2	35	8	100
88	84	83	15	151		88	<u>8</u> 2	<u>8</u> 2	53	83	82	88	83	$ \mathcal{T} $			58	58	<u>8</u> 2	53	53	85	83	83	83	35	2	ŝ
84	84	83		161	121	83	10	¥8	38	25	25	84	83	121	14		83	83	¥9	23	28	25	84	83	83	94) 1	12	3
					_																							

Fig.B.11. ROM pull up layout



Fig B.12 Tree input layout



Fig. B.13 Tree 1st layout



Fig B.13 Tree 2nd layout



Fig B 14 Tree 4th layout



Fig B.15 D flip flop



Fig B.16 9 D flip flop layout



Fig B.17 256 ROM layout
APPENDIX C

DDS CHIP



Fig C.1 DDS



Fig C.2 Top level layout of DDS



Fig C.3 Top level schematic of DDS



Fig C.4 Top level symbol of DDS

APPENDIX D

VALUES OF PROGRAMMED 256 ROM

ROM D	ROM C	ROMB	ROM A
00000010	011000101	101101010	111011001
00000101	011001000	101101101	111011010
000001011	011001011	101101111	111011011
000001000	011001110	101110001	111011100
000001110	011010001	101110011	111011101
000010001	011010011	101110101	111011110
000010100	011010110	101110111	111100000
000011000	011011001	101111010	111100001
000011011	011011100	101111100	111100010
000011110	011011111	101111110	111100011
000100001	011100010	110000000	111100100
000100100	011100100	110000010	111100101
000100111	011100111	110000100	111100110
000101010	011101010	110000110	111100111
000101101	011101101	110001000	111101000
000110001	011101111	110001010	111101001
000110100	011110010	110001100	111101001
000110111	011110101	110001110	111101010
000111010	011111000	110010000	111101011
000111101	011111011	110010010	111101100
001000000	011111101	110010100	111101101
001000110	10000000	110010110	111101110
001000110	10000011	110011000	111101111
001001001	100000101	110011010	111101111
001001101	100001000	110011011	111110000
001010000	100001011	110011101	111110001
001010011	100001101	110011111	111110010
001010110	100010000	110100001	111110010
001011001	100010011	110100011	111110011
001011100	100010101	110100100	111110100
001011111	100011000	110100110	111110100
001100010	100011011	110101000	111110101
001100101	100011101	110101010	111110101
001101000	100100000	110101011	111110110
001101011	100100010	110101101	111110111
001101110	100100101	110101111	111110111
001110001	100101000	110110001	111111000
001110101	100101010	110110010	111111000
001111000	100101101	110110100	111111001
001111011	100101111	110110101	111111001
001111110	100110010	110110111	111111010
010000001	100110100	110111001	111111010
010001010	100110111	110111010	111111011
010000111	100111001	110111100	111111011
010001010	100111100	110111101	111111011

010001101	100111110	110111111	111111100
010010000	101000001	111000000	111111100
010010011	101000011	111000010	111111100
010010110	101000101	111000011	111111101
010011001	101001000	111000101	111111101
010011100	101001010	111000110	111111101
010011111	101001101	111001000	111111101
010100010	101001111	111001001	111111110
010100101	101010001	111001011	111111110
010101000	101010100	111001100	111111110
010101011	101010110	111001101	111111110
010101110	101011000	111001111	111111110
010110001	101011011	111010000	111111111
010110100	101011101	111010001	111111111
010110110	101011111	111010011	111111111
010111001	101100001	111010100	111111111
010111100	101100100	111010101	111111111
010111111	101100110	111010110	111111111
011000010	101101000	111011000	111111111