Testing and Improvement of Low Noise Amplifier for Wireless Interrogation of UMaine Surface Acoustic Wave Sensors

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Abstract

The testing and improvement of the Low Noise Amplifier (LNA) designed in ECE 547 for wireless interrogation of one port Surface Acoustic Wave (SAW) resonator based sensors is described in this report. UMaine SAW sensors have resonant frequencies >300MHz and a high quality factor. The receiver front-end for wireless interrogation of SAW sensors requires a low-noise amplifier for signal conditioning. A narrowband LNA was designed to operate between 303MHz and 356MHz using 0.18µm CMOS technology in Cadence and fabricated by MOSIS integrated circuit fabrication services. DC testing was performed on unpackaged and packaged chips. High frequency analysis to measure the S_{11} parameter of the unpackaged chip was also performed. DC analysis on unpackaged devices showed a bias current of 4mA, which was slightly lower than the designed 6mA. In addition, the unpackaged device had a S_{11} response of approximately -8dB. This report also includes an improved design to improve LNA performance, reduce stray and parasitic resistance, and added debugging features to address the design defects from the previous design.

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1.Introduction

As continuation of ECE 547, VLSI design course, the designed Low Noise Amplifier (LNA) for wireless interrogation of Surface Acoustic Wave (SAW) resonators used in sensor applications was tested and redesigned under this ECE 599 course. A one-port SAW resonator is an acoustic device which consists of interdigital transducers (IDTs) fabricated on a piezoelectric substrate which generate acoustic waves traveling along its surface and reflector gratings to reflect the waves and confine it in its resonant cavity as shown in Figure 1; thus providing a high quality factor (Q) device critical for communications as filters and resonators and widely used in a multitude of sensor applications.

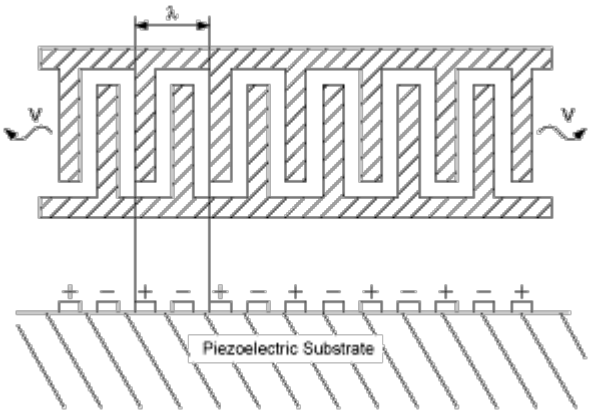

Figure 1. SAW Resonator Structure

University of Maine harsh environment SAW resonators are fabricated on Lanthanum Gallium Silicate (LGS) substrates using thin film fabrication technology and operate at frequencies greater than 300MHz. Due to the harsh environment needs (often mounted on moving parts such as turbine blades) and battery-free nature of these devices, they need to be wirelessly interrogated. The receiver front-end of the SAW sensor interrogation system as shown in Figure 2 requires addition signal condition such as filtering and amplification of the signal in the desired

frequency band; thus, a LNA with high gain and low noise figure is critical for a good sensor system.

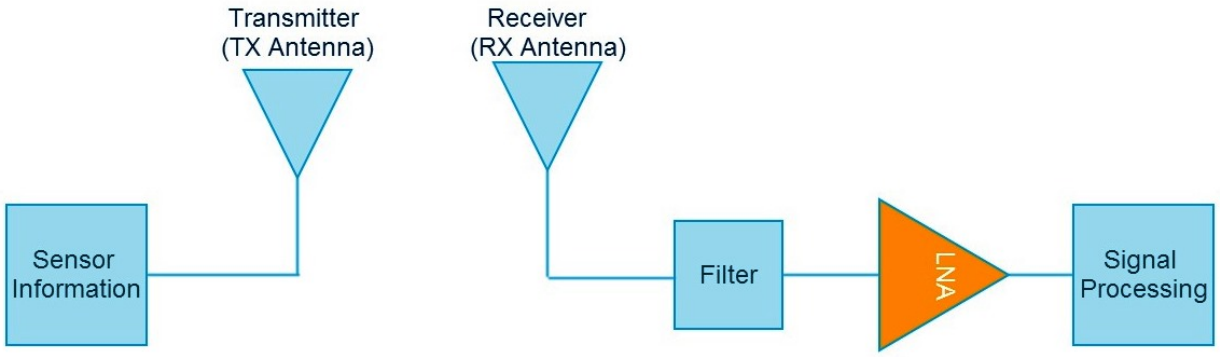

Figure 2. RF Communication Block Diagram

The work carried out under this course was divided into two sections, namely: (i) LNA testing; and (ii) LNA redesign. Firstly, the fabricated LNAs (both packaged and unpackaged) were tested and their DC as well as AC behavior was analyzed. During testing, a number of design flaws and issues were encountered and addressed as part of the LNA redesign procedure. Section 2 provides the background and short explanation of the LNA designed in ECE 547. The DC and AC testing carried out on packaged and unpackaged LNAs is presented in Section 3. Section 4 discusses the design issues and solutions that were implemented in the redesigned LNA to address the issues. Section 5 presents the updated schematic, layout, and simulation results of the improved LNA. Lastly, Section 6 concludes this report.

2. LNA designed in ECE 547

During the spring semester of 2014, a tunable LNA was designed using 0.18µm technology using Cadence. Five major factors that were considered in the design of the LNA were high forward gain, low return loss, low noise figure (NF), stability, and high input matching. There

are commonly six LNA topologies reported in literature, namely: (a) Resistive Termination; (b) Common Gate; (c) Series Shunt Feedback; (d) Current Reuse; (e) Inductor Neutralization; (f) Inductive Degeneration. The advantages and disadvantages of these topologies were studied and the inductive degeneration topology shown in Figure 3 was chosen because of its properties such as good narrowband match ideal for SAW sensors which have high Q values (>3000) and small NF to minimize noise. The drawback of inductive degeneration topology is its large size; however, since the chip implemented was 1.5mm by 1.5mm, size wasn't an issue.

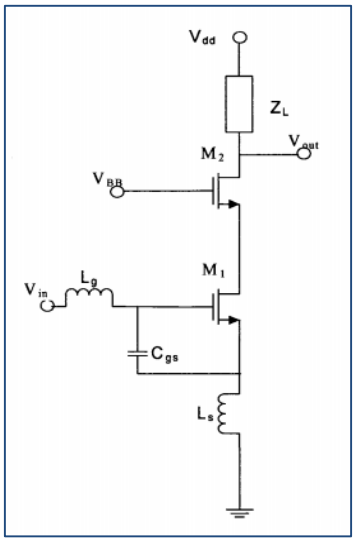

Figure 3: Inductive degeneration LNA topology

Based on the basic inductive degeneration LNA topology, the LNA was designed using current mirroring for biasing and varactor for frequency tunability as shown in the schematic in Figure 4. The components used in the LNA design were from the CMRF7SF library. Frequency tuning was obtained using a DIFFHAVAR varactor implementation as shown in Figure 5. Refer to Appendix B for more detailed analysis on input matching, noise figure optimization and implementation of frequency tuning as stated in the ECE 547 report.

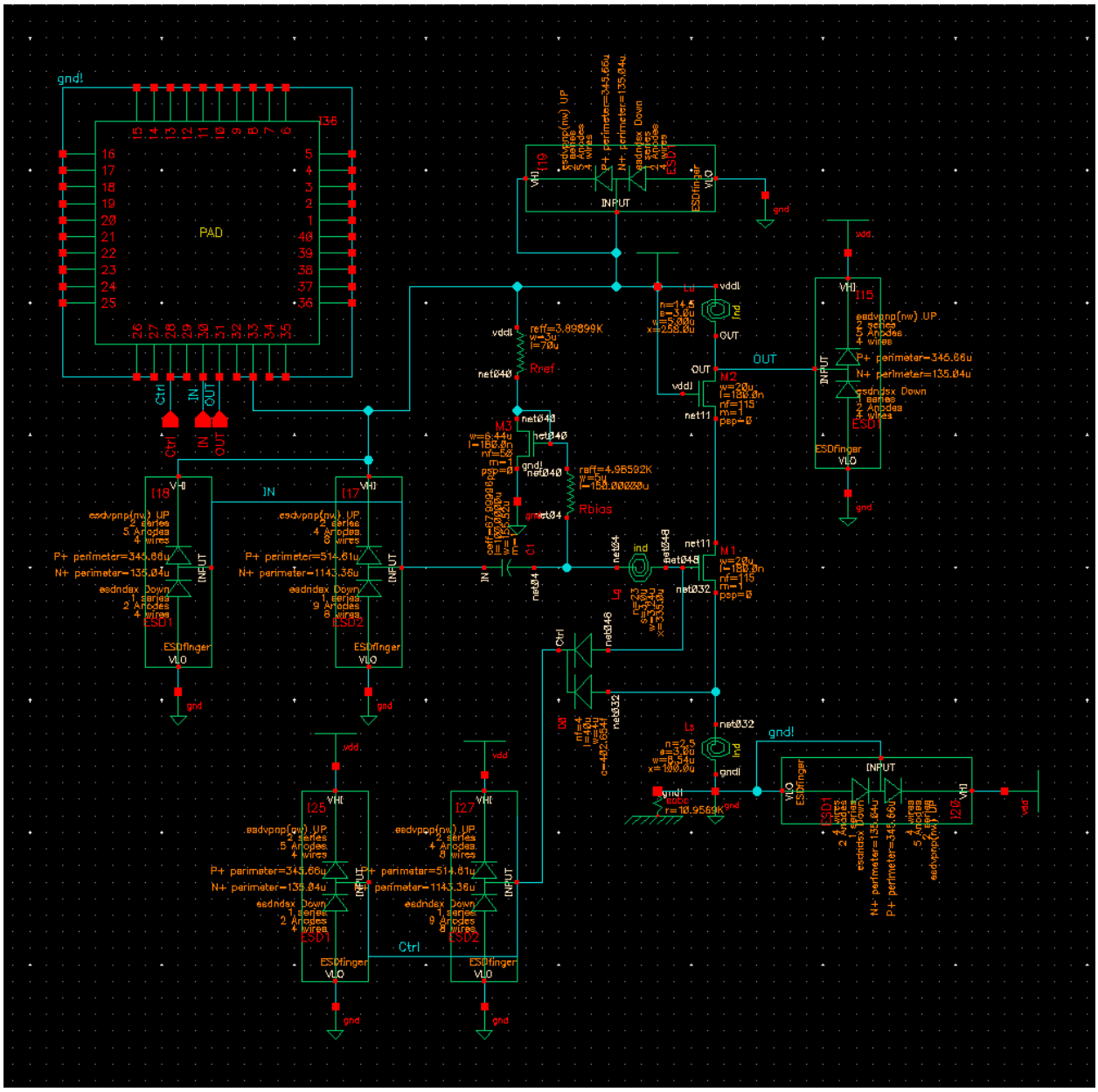

Figure 4: Designed LNA schematic

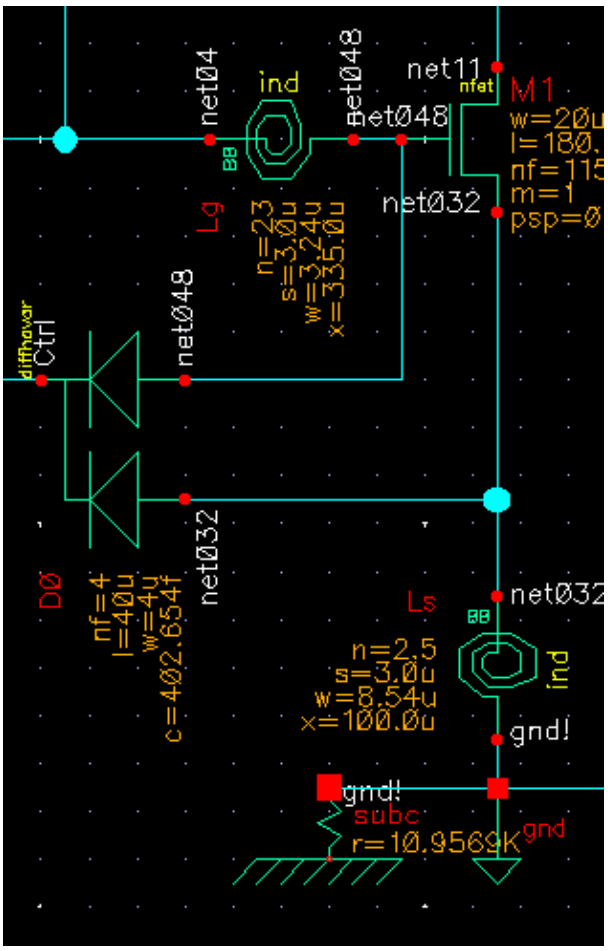

Figure 5. Implementation of Frequency Tuning using DIFFHAVAR

Figure 6 shows the final layout of the designed LNA. The LNA was designed to operate between 303MHz and 356MHz with an external control voltage between 0V and 6V to tune the frequency of operation.

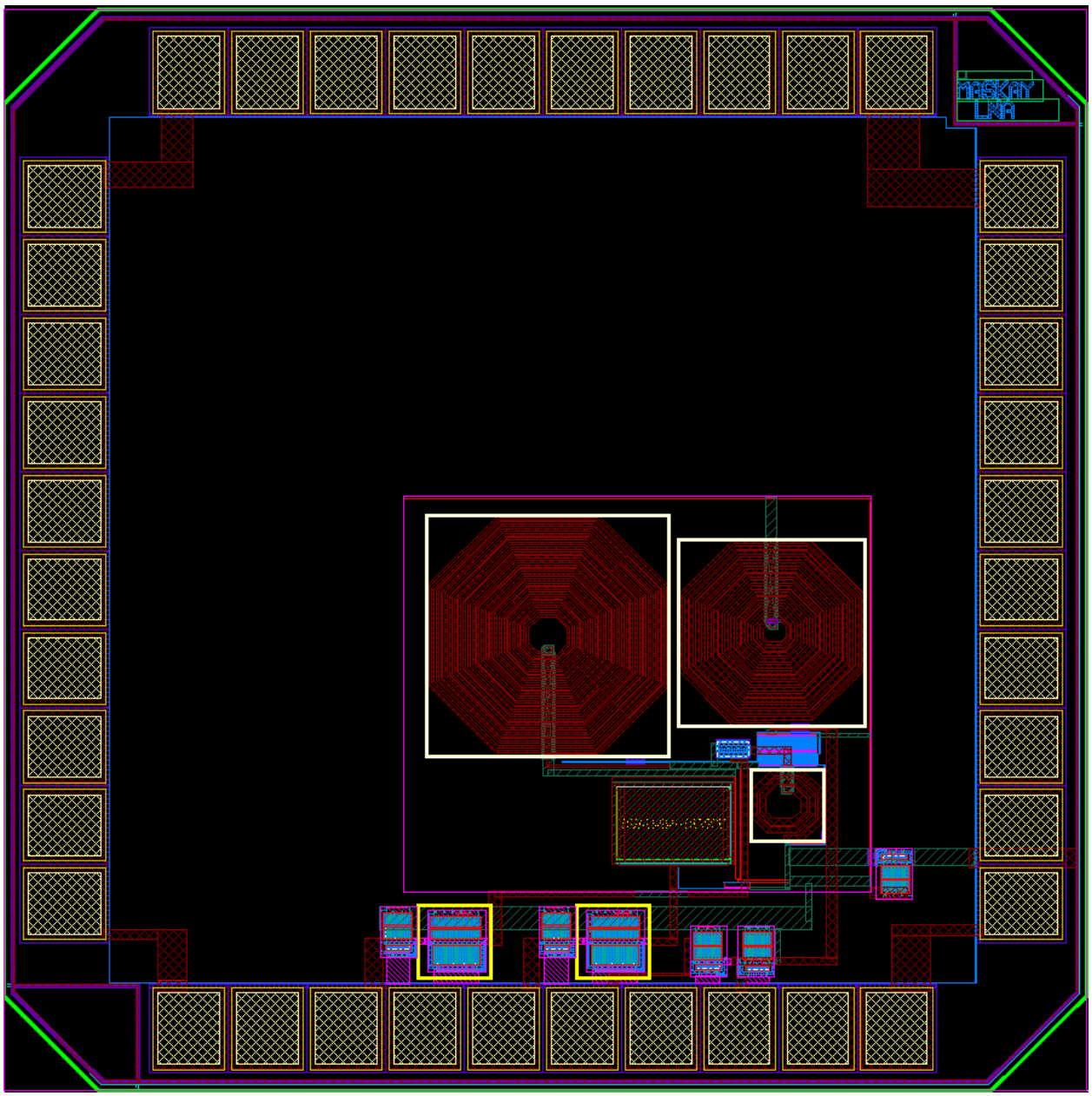

Figure 6: Designed LNA layout

The simulation of LNA was performed using two-port analysis to verify that the designed LNA had a relatively decent gain, low noise figure and narrowband frequency tuning capability as shown Table 1. The resistors and transistors were sized and optimized to draw a current of approximately 5.9mA as shown in Figure 7. At 330MHz the LNA has a gain of 12.8dB and

Noise Figure (NF) of 3.65dB. The lowest gain for the design is 11.5dB at 303MHz and the highest noise figure is 3.74dB at 356MHz.

Table 1. Simulation Results

Control Voltage (V)	Operating Frequency (MHz)	S_{11} (dB)	S_{21} (dB)	NF (dB)
0	356	-24.2	17.1	3.74
6	303	-31.0	11.5	3.57
1.5	330	-28.4	12.8	3.65

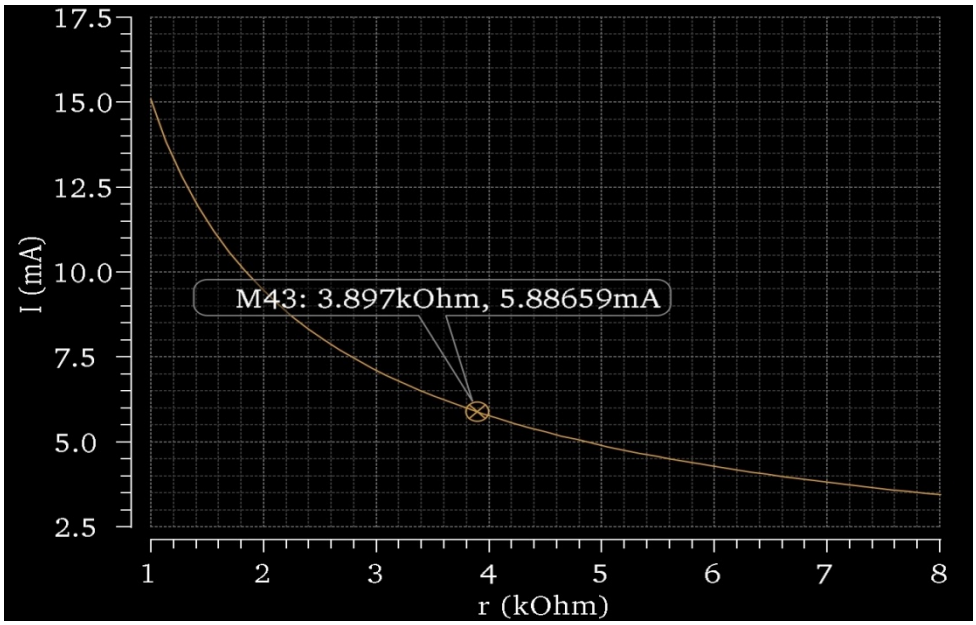

Figure 7. Plot illustrating the designed bias current

3. LNA Testing

Upon successful design and simulation of the LNA in ECE 547, the design was sent out to MOSIS for fabrication. 20 samples each of unpackaged and packaged (DIP40) chips were

obtained for testing. Figure 8 and Figure 9 show images taken using a Cascade Microtech microscope of the complete unpackaged chip and a zoomed region of the LNA, respectively.

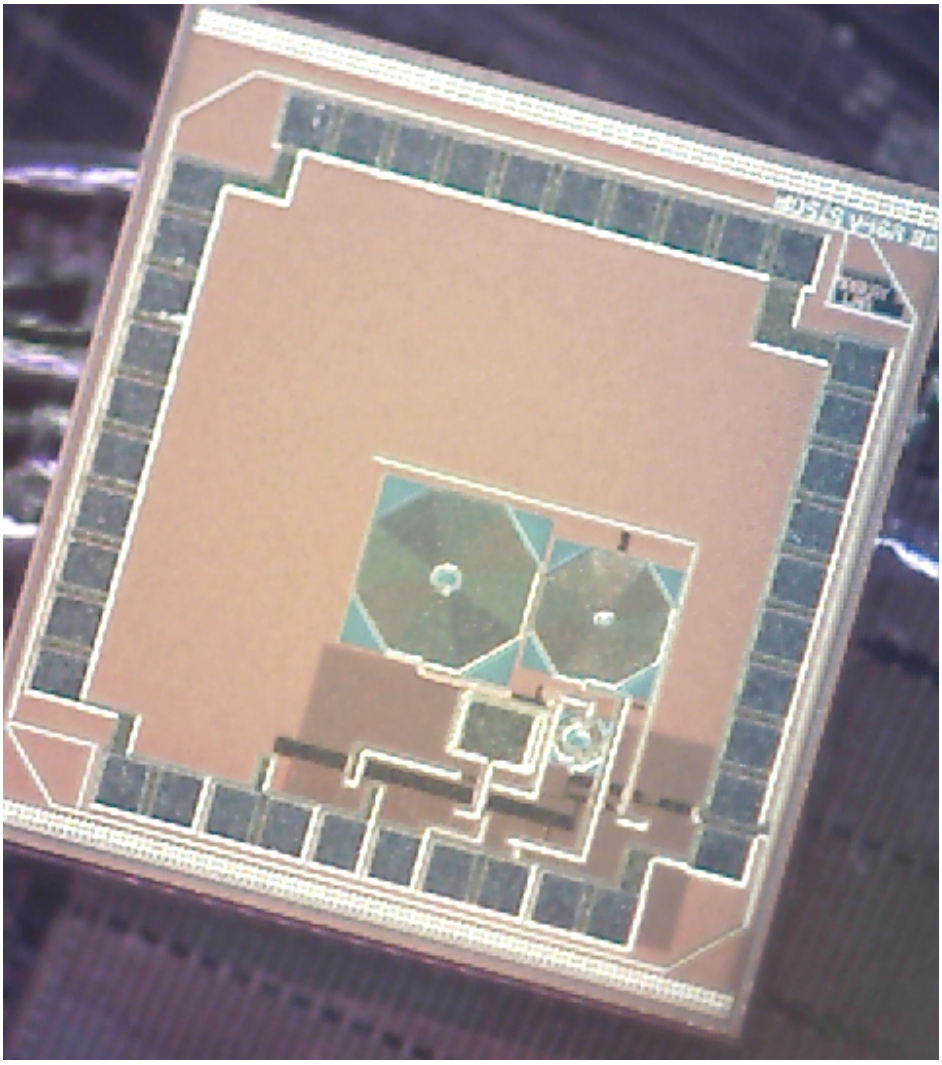

Figure 8: Full photograph of unpackaged LNA

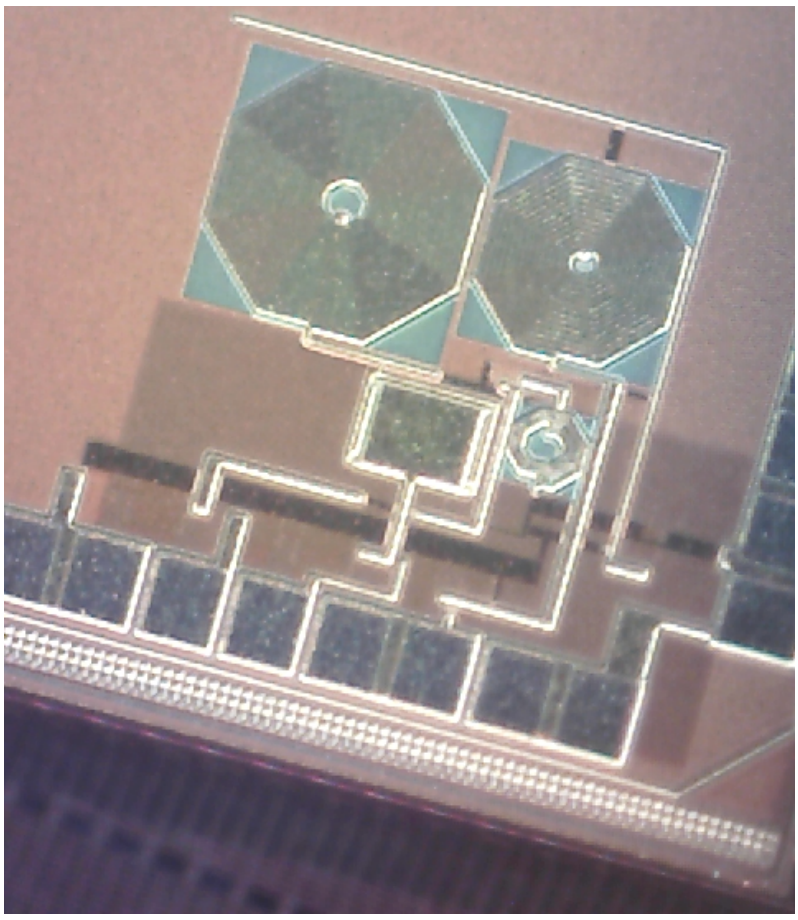

Figure 9: Zoomed in photograph of the active section of LNA

DC analysis was carried out on both packaged and unpackaged chips; whereas AC analysis was only carried out on the unpackaged devices. The measurement procedure and results of the DC analysis are discussed in Section 3.1 and the methodology and results of the AC analysis are discussed in Section 3.2.

3.1. DC Testing

DC testing to check the current drawn by the chip was first carried out using a packaged device. The device was mounted on a breadboard. The 1.8V supply voltage was provided using a BK Precision 1761 DC power supply, whereas the control voltage ranging from 0V to 6V in 1.5V steps was provided using a BK Precision 1788 DC power supply. The idea was that the current

drawn from the BK Precision 1761 power supply could be measured as the control voltage was varied from 0V to 6V. However, there was no current drawn by the chip for any amount of control voltage. This observation was verified by testing several other packaged chips. Since there was no pin available to provide easy access to measure the bias voltages, additional testing was not possible. However, this flaw has been addressed in the updated design discussed in Section 5.

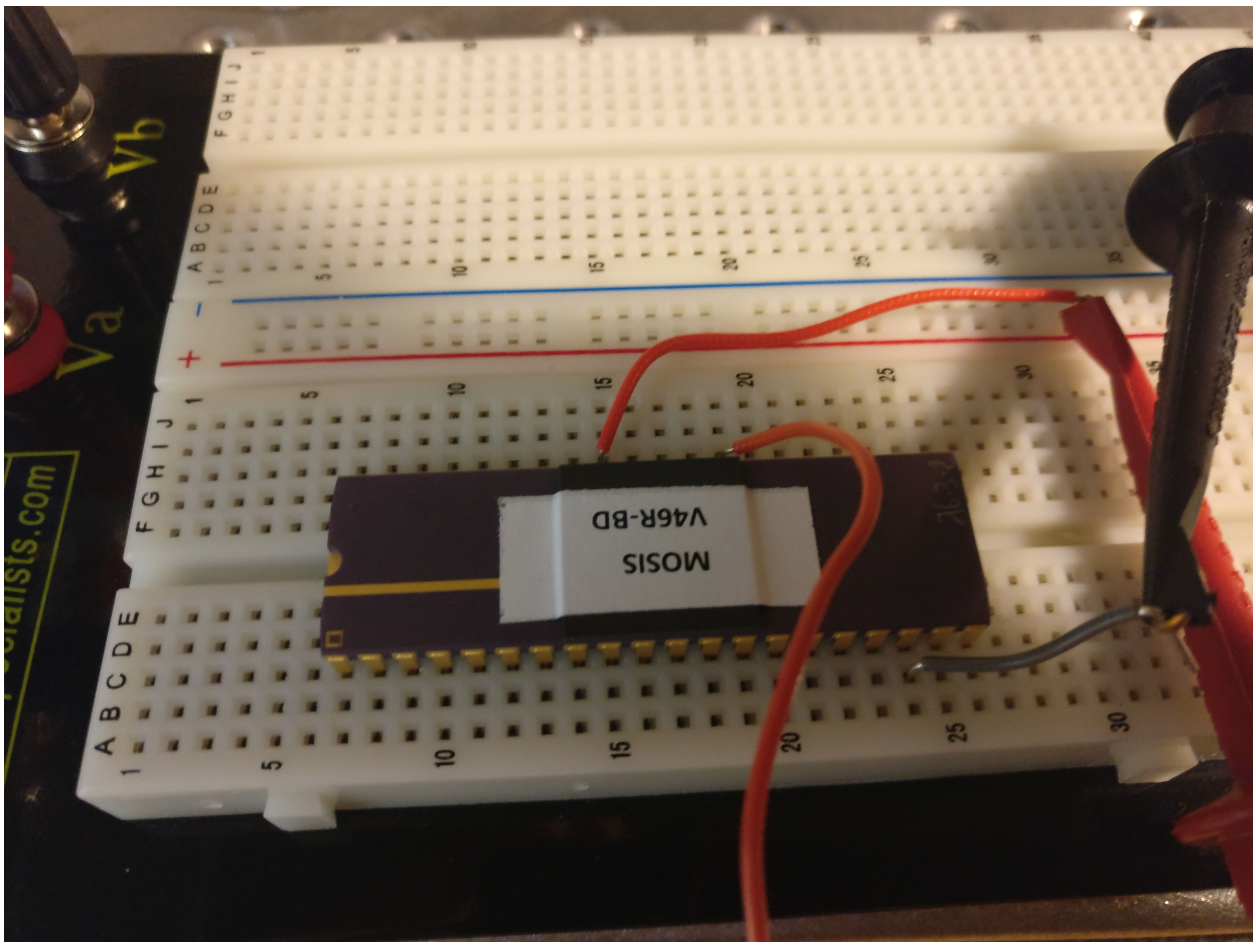

Figure 10: DC test setup for packaged LNA

Since the packaged chips were not working, testing on unpackaged chips was proceeded incase the bond leads on the packaged chips were causing measurement issues. Figure 11 shows the test setup for DC analysis of unpackaged LNAs. The LNA was superglued onto a 4 inch silicon

wafer and placed in a Cascade Microtech probe station. The bondpads were probed using DC DCM precision positioner probes. The 1.8V supply voltage was provided using an Agilent E3642A DC power supply, whereas the control voltage ranging from 0V to 6V in 1.5V steps was provided using a second Agilent E3642A DC power supply.

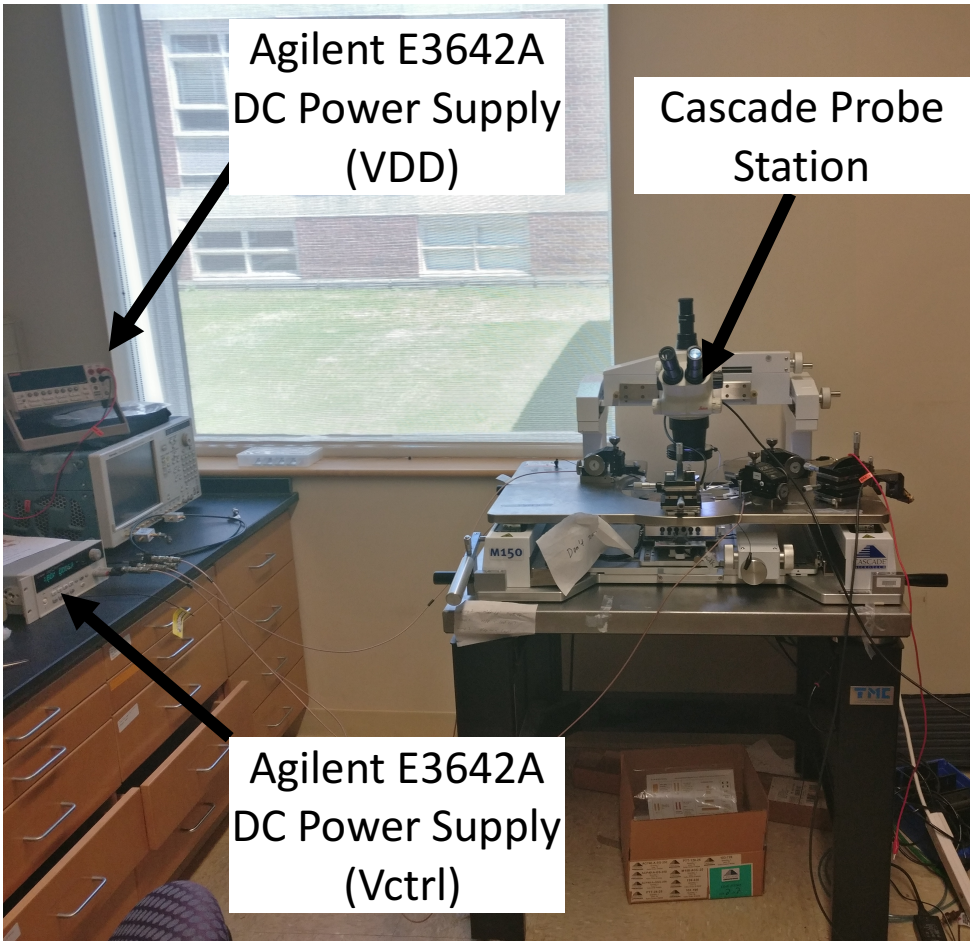

Figure 11: DC test setup for unpackaged LNA

The summary of results of DC analysis carried on an unpackaged LNA is shown in Table 2. As the control voltage (V_{ctrl}) was varied from 0V to 6V in 1.5V steps, the current drawn from the DC power supply was measured. For all cases the current drawn by the LNA was 4mA, which is

slightly lower than the designed bias current of 5.9mA. These results were confirmed using measurements from another LNA as well.

Table 2: DC test results on unpackaged LNA

V_{ctrl}	I_{drawn}
0V	4mA
1.5V	4mA
3V	4mA
4.5V	4mA
6V	4mA

3.2. AC Testing

Since DC testing was only successful on the unpackaged LNAs, AC analysis was only carried out on unpackaged devices. Figure 12 shows the test setup for AC analysis of unpackaged LNAs. The LNA was superglued onto a 4 inch silicon wafer and placed in a Cascade Microtech probe station. The DC bondpads (V_{DD}, Gnd, and V_{ctrl}) were probed using DC DCM precision positioner probes, whereas the AC bondpad (Input) was probed using a Cascade Microtech 200µm pitch/spacing signal-ground (SG) high frequency probe. The 1.8V supply voltage was provided using an Agilent E3642A DC power supply, whereas the control voltage ranging from 0V to 6V in 1.5V steps was provided using a second Agilent E3642A DC power supply. The RF response was measured using an E5071C vector network analyzer (VNA). The VNA was

calibrated using a Cascade Microtech standard 103-726 substrate for a center frequency of 350MHz and a span of 100MHz.

During ECE 547, the idea probe pitch was not known, hence the LNA was not designed with the RF input and output bondpads spaced 200µm away from a ground pad to allow RF measurements. The pin assignment for the LNA design is shown in Table 3 and there is no ground pin spaced 200µm away from the IN and OUT pins.

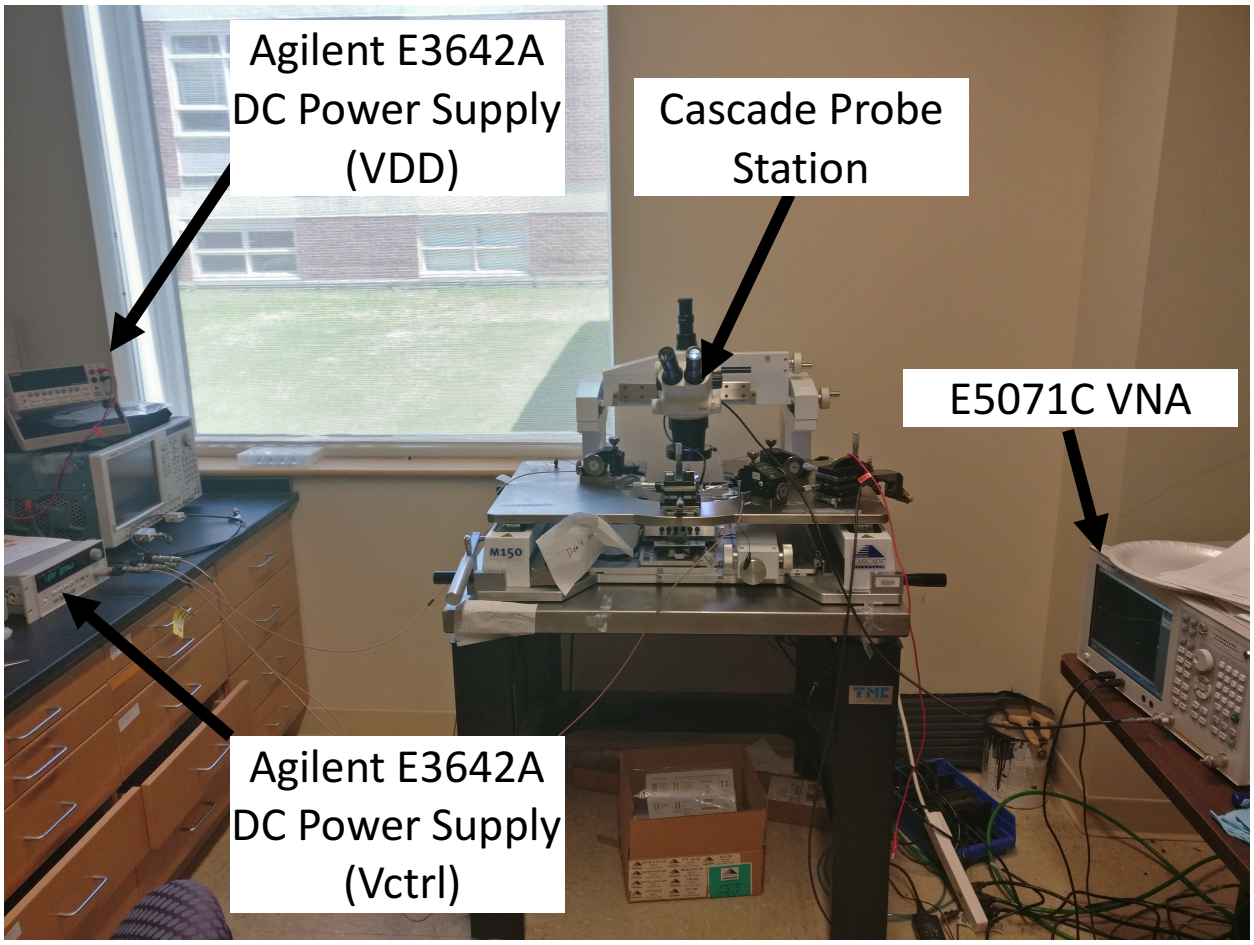

Figure 12: AC test setup for unpackaged LNA

Table 3. LNA Pin Assignment

Pins	Assignment
30	IN
31	OUT
28,29	CTRL
32,33	VDD
1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19, 20,21,22,23,24,25,26,27,34,35,36,37,38,39,40	GND

Due to this pin placement issue, currently only one parameter can be measured i.e. S_{11}. This was possible by using the CTRL pin (normally for the varactor control voltage) as a ground pin so that the Cascade probe ground tip could be placed on the CTRL pin and the signal tip be placed at the IN pin as shown in Figure 13. This limitation has been addressed more in detail in Section 4 and a fix has been implemented in the redesigned LNA in Section 5 to allow measurement of S_{21} parameter along with S_{11}.

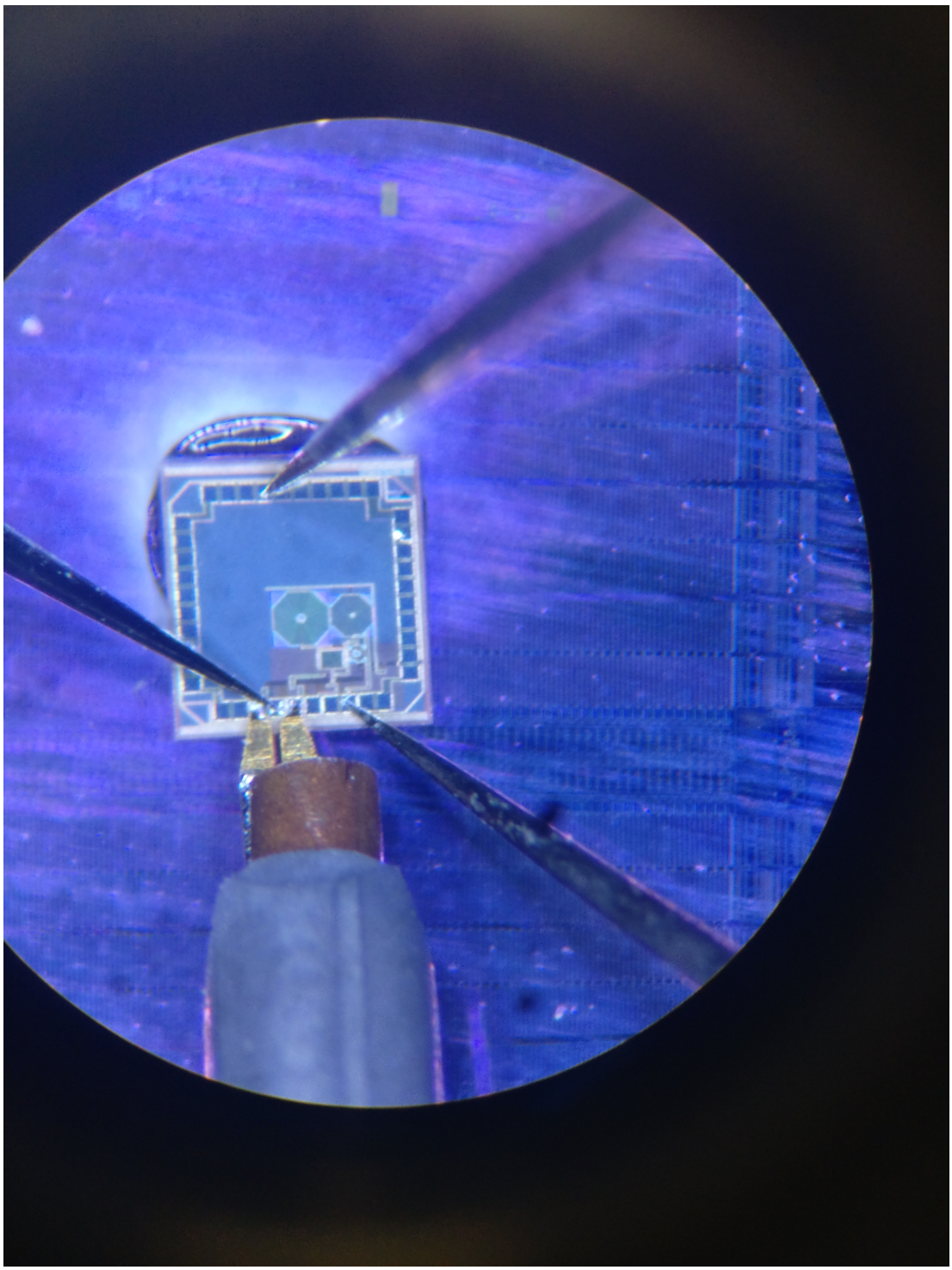

Figure 13: Probe placement for AC analysis of LNA

Figure 14 shows the magnitude of S_{11} in decibels (dB) response of the LNA with a control voltage of 0V. At the designed frequency of 356MHz, the LNA has a return loss of approximately -7.8dB, which is much lower than the simulated S_{11} value of -24dB. Possible issues leading to this discrepancy and the overall reduced performance of the LNA will be discussed in Section 4.

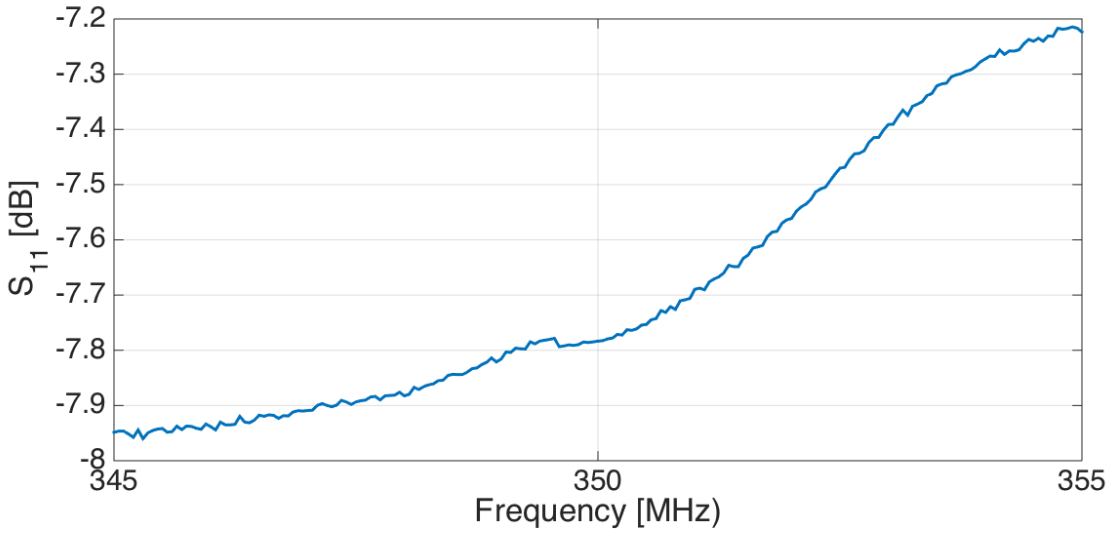

Figure 14: S_{11} response of LNA with 0V control voltage

4. Design Issues

4.1. Parasitics

Although the LNA designed in ECE 547 was designed by reducing parasitics by making short traces and using higher level metals whenever possible; upon further inspection, the transistors M_1, M_2, and M_3 and the V_{DD} line had traces connected at the M1 and M2 metal layers as shown in Figure 15 and Figure 16 which are highly resistive and adds a considerable amount of parasitic resistance to the design.

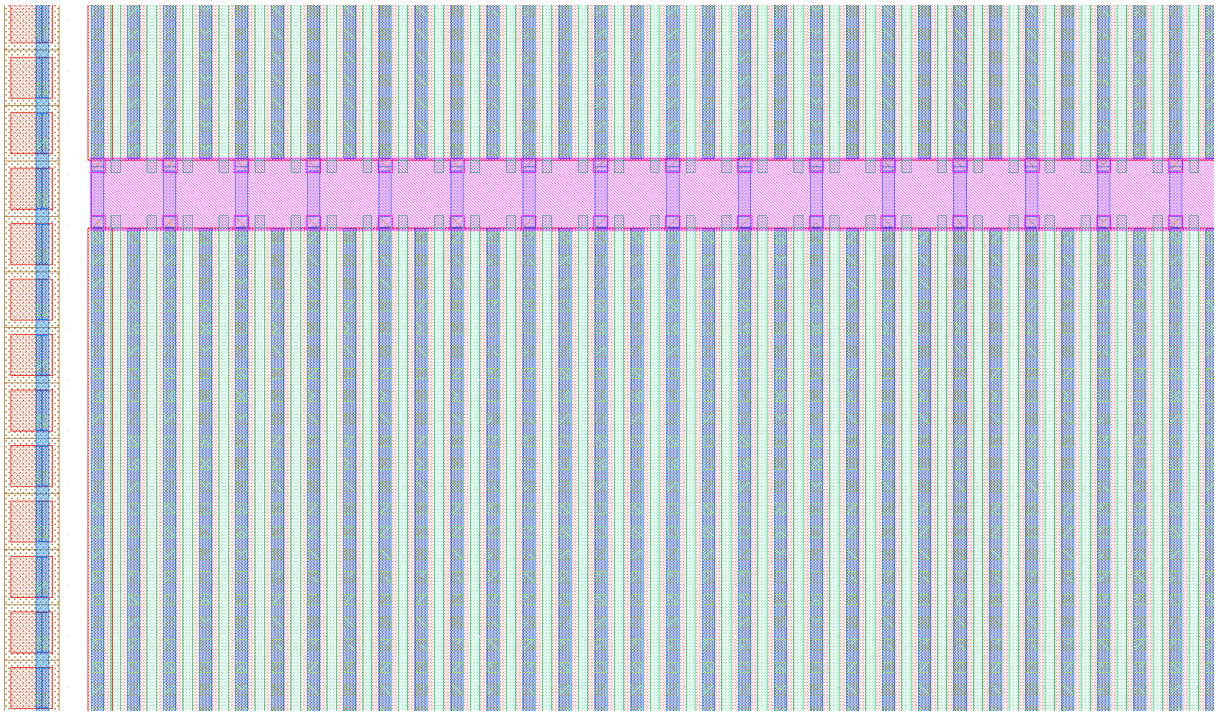

Figure 15: Metals M1 and M2 connected traces for V_{DD} and M_1 transistor

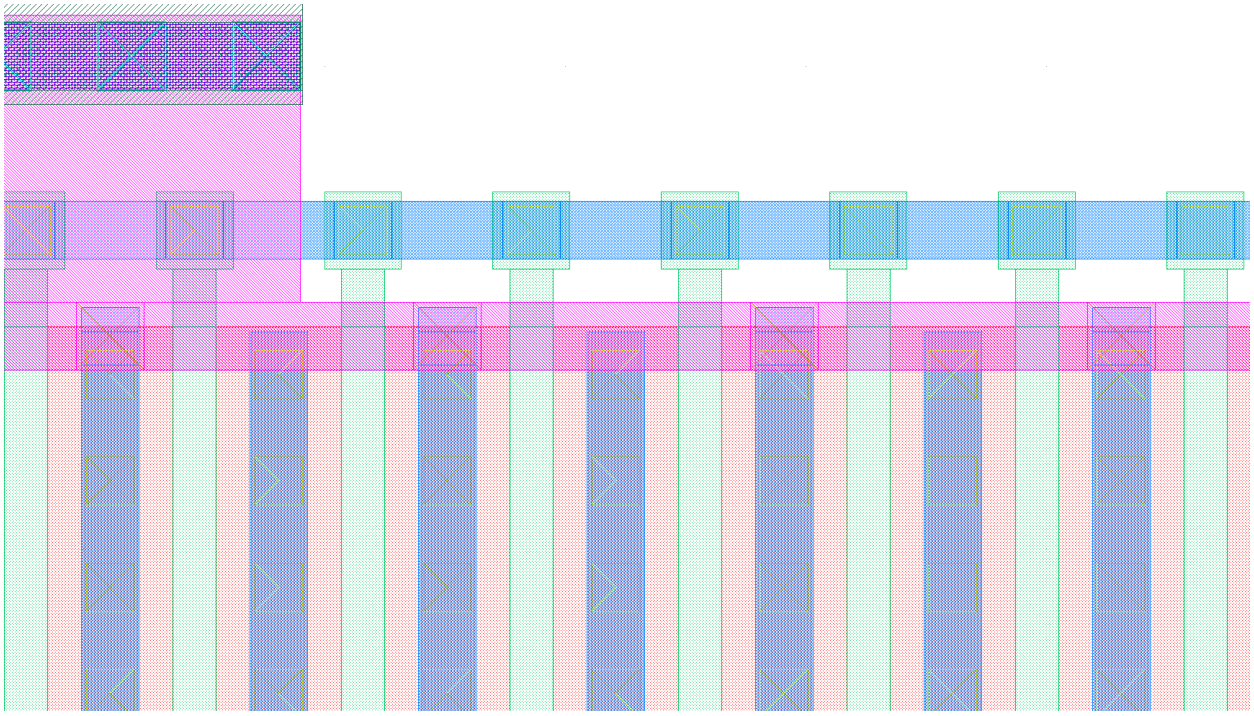

Figure 16: Metals M1 and M2 connected traces for M_2 transistor gate and drain

In order to minimize these parasitic resistance due to traces, the LNA design was revisited and modified such that transition from metal layer M1 to either the MT or AM layer were made using appropriate vias in all contact zones as illustrated in Figure 17.

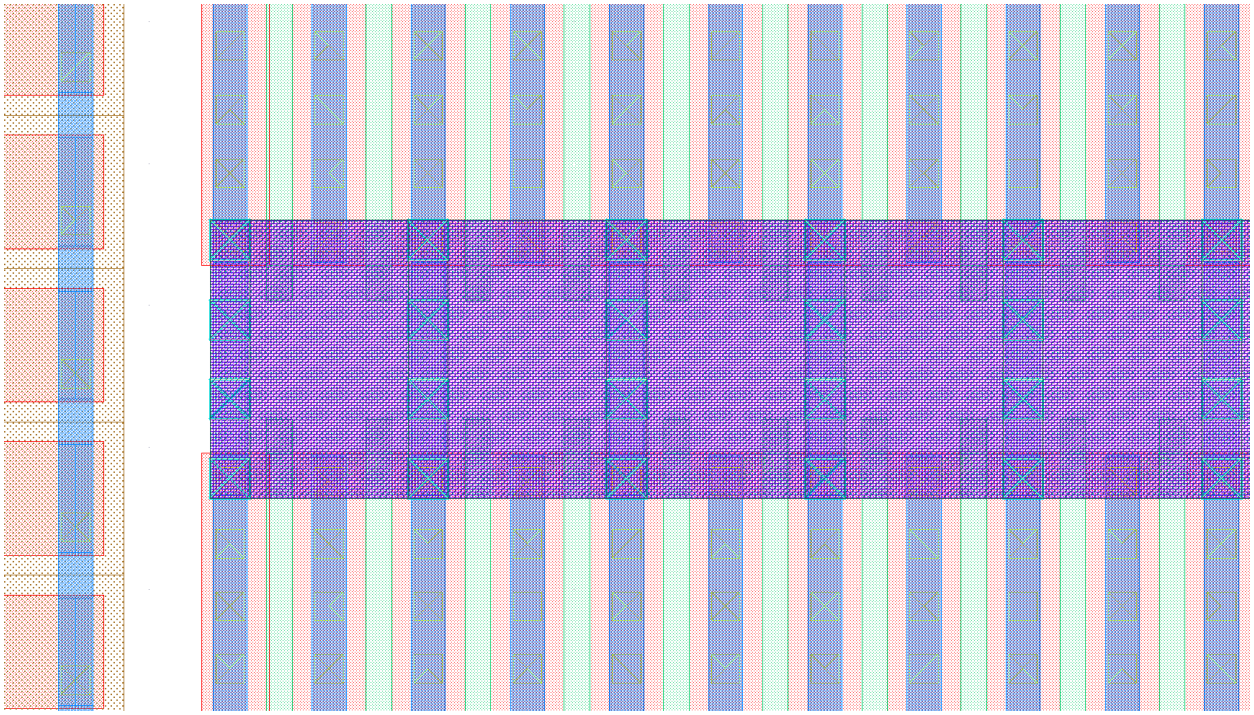

Figure 17: Modified design showing connection made in the MT metal layer to avoid parasitic resistance

4.2. Bondpad placement

Due to lack of knowledge about probe pitch and their availability at UMaine facilities, the LNA design was flawed in this respect and as mentioned in Section 3.2, AC measurements were limited to S_{11} due to placements of the bondpads. Therefore, the LNA design was modified to address this issue; pad assignments for GND and VDD as shown in Table 4 so that RF SG probes from cascade with a pitch of 200µm could be used to measure all four S-parameters (S_{11}, S_{22}, S_{21}, and S_{12}). The bondpad layout showing the spacing between the IN and OUT pins and the GND pads is shown in Figure 18.

Table 4: Pin assignment for redesigned LNA

Pins	Assignment
30	IN
31	OUT
39	VBias
36	VDD
32,33,34,35,37,38	GND

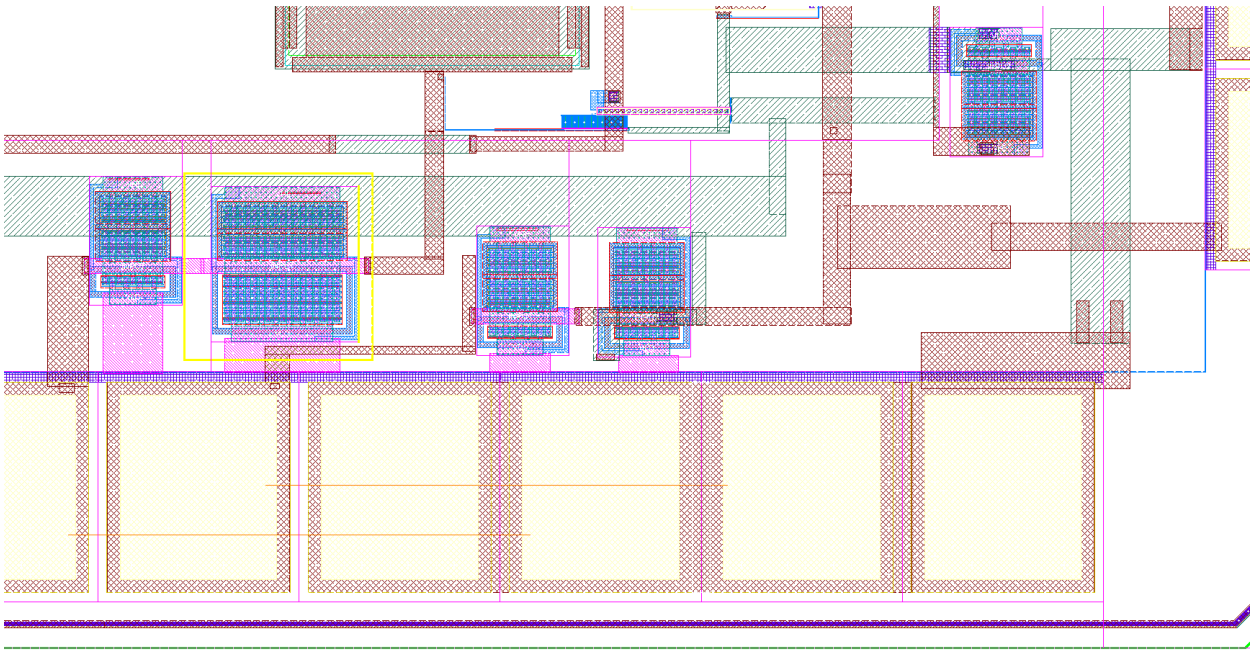

Figure 18: Redesigned pin layout showing spacing between ground pads (four on the right) and the IN and OUT pins

4.3. Varactor

Although the varactor implementation allowed frequency tuning and added operational flexibility, its implementation adds extra complexity and could be one of the causes of unreliable LNA behavior. Hence, after discussing with Dr. Kotecki, it was deemed that the varactor should be removed. Thus, in the modified design, the varactor implementation was removed completely so that the LNA operated at a fixed frequency of 356 MHz.

4.4. External Bias

One of the main features that was missing in the original LNA design was the ability to probe the bias voltage at the L_g inductor. This feature was clearly hampering testing both packaged and unpacakaged LNAs since it limited debugging the LNA. Therefore, in the updated design, a DC pin was added at the input of the L_g inductor so that the voltage at that point could be probed and/or an external bias could be applied in case the expected voltage was not seen at that node. This allows added robustness and flexibility to the LNA design.

5. Redesigned LNA

After careful considerations of the issues mentioned in Section 4, a modified schematic and layout of the LNA was generated to address the aforementioned issues. The updated LNA schematic is shown in Figure 19 and the corresponding layout is shown in Figure 20. The ability to tune frequency was removed; however, probing and initiating the bias voltage at L_g was implemented in this design. In addition, parasitic resistance was significantly reduced in this design by using upper level metals instead of the previously used lower level metals. Moreover, bondpads were realigned and reassigned to allow complete RF testing in the future design.

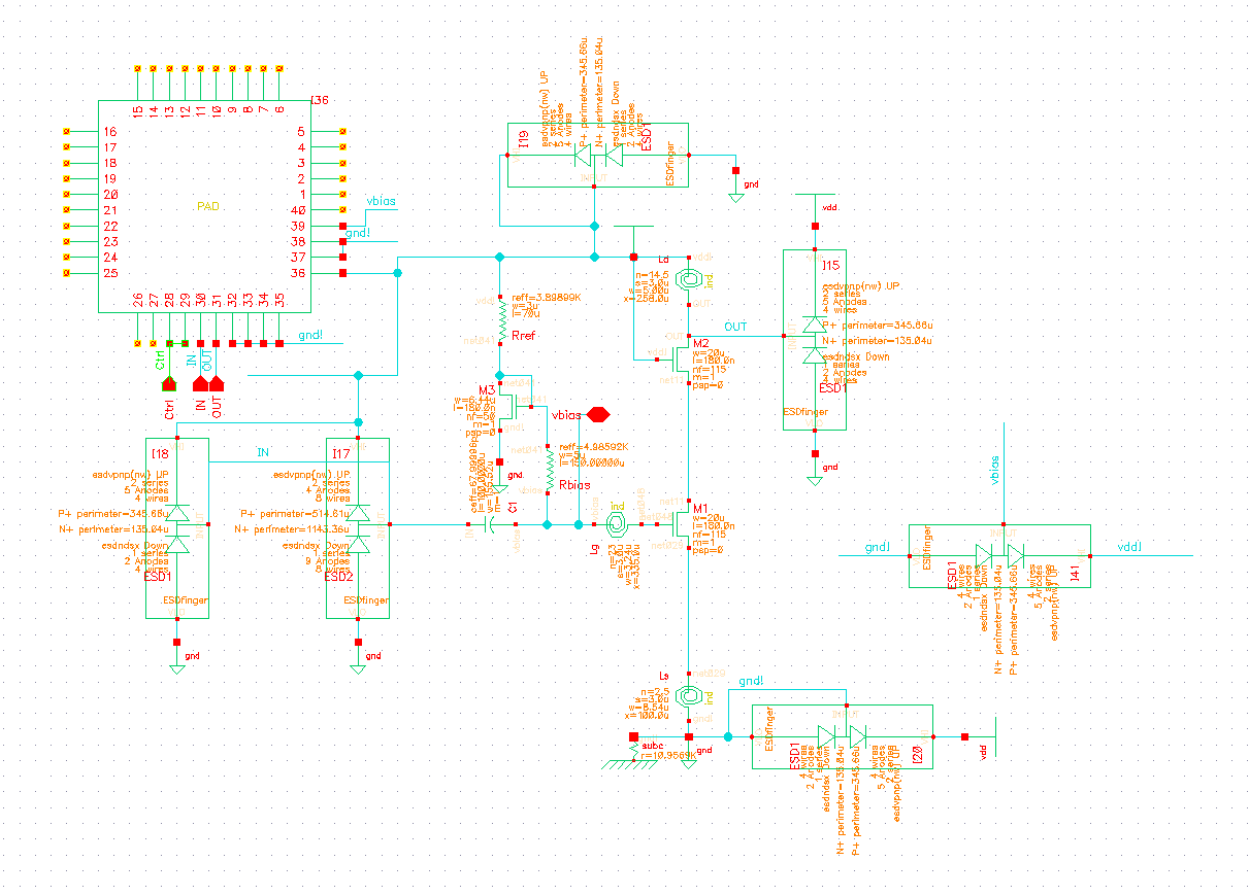

Figure 19: Updated LNA design

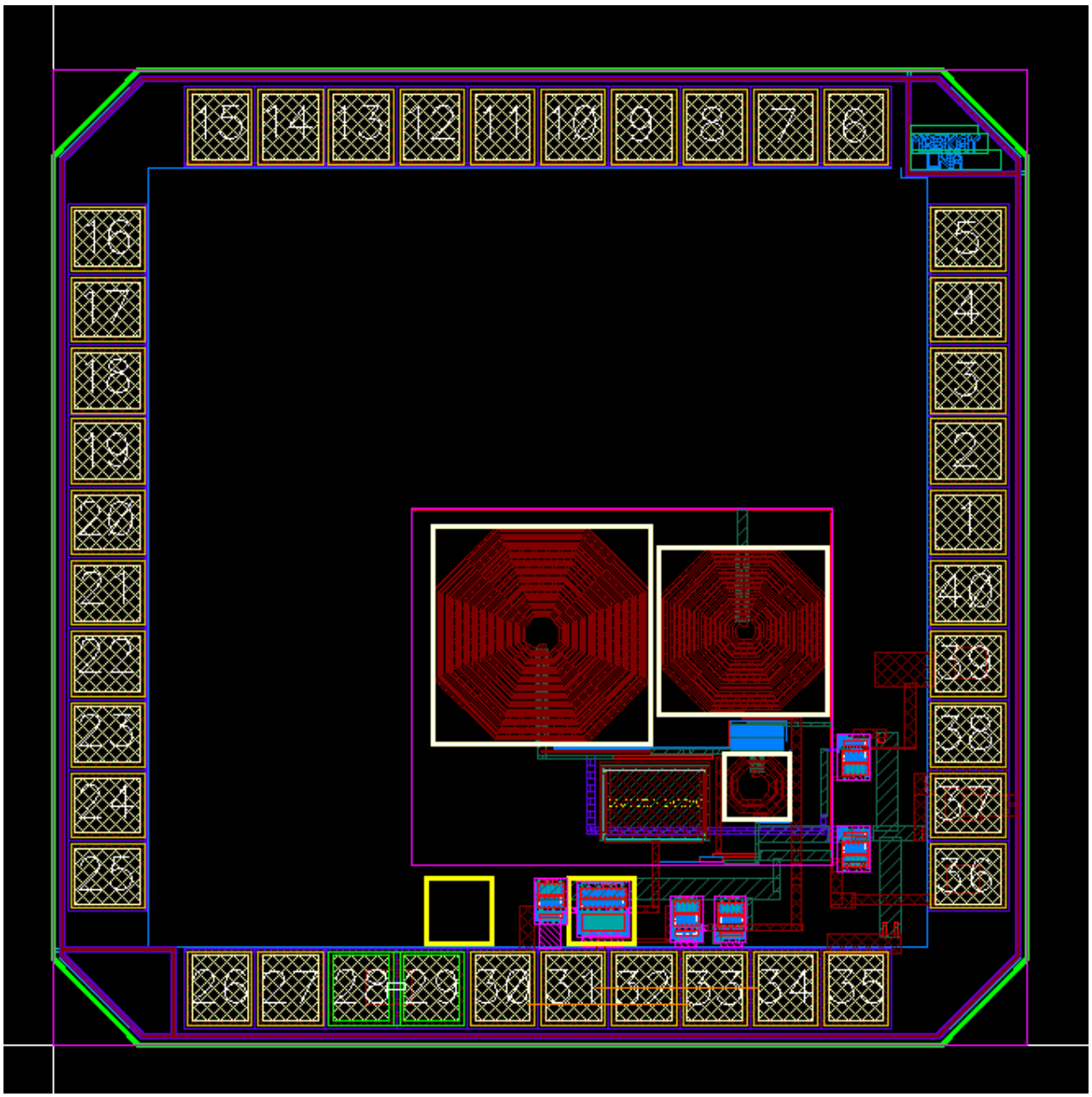

Figure 20: Updated LNA layout

The modified design occupies approximately 847µm by 675µm. The pins with the lowest parasitics were chosen for the input and output signal. The final design passed DRC, ESD DRC, floating gate, and LVS checks. Upon completion of the necessary checks, the complete layout was simulated to compare the S-parameters and noise figure with the original design. Two-port analysis carried out and reported in the ECE 547 report was repeated for the modified LNA.

Figure 21, Figure 22, and Figure 23 show the S_{11} (return loss), S_{21} (gain), and noise figure (NF) responses, respectively, for the updated LNA. The comparison of performance of the updated design and the original LNA design in terms of S_{11}, S_{21}, and NF is shown in Table 5. The updated design had a superior return loss and 1dB lower NF when compared to the original LNA, which is most likely due to the reduced stray and parasitic resistance in the new design. Although the gain of the updated LNA is 1dB lower than the original design, the tradeoff is a reduced NF and is the more important factor in harsh environment applications.

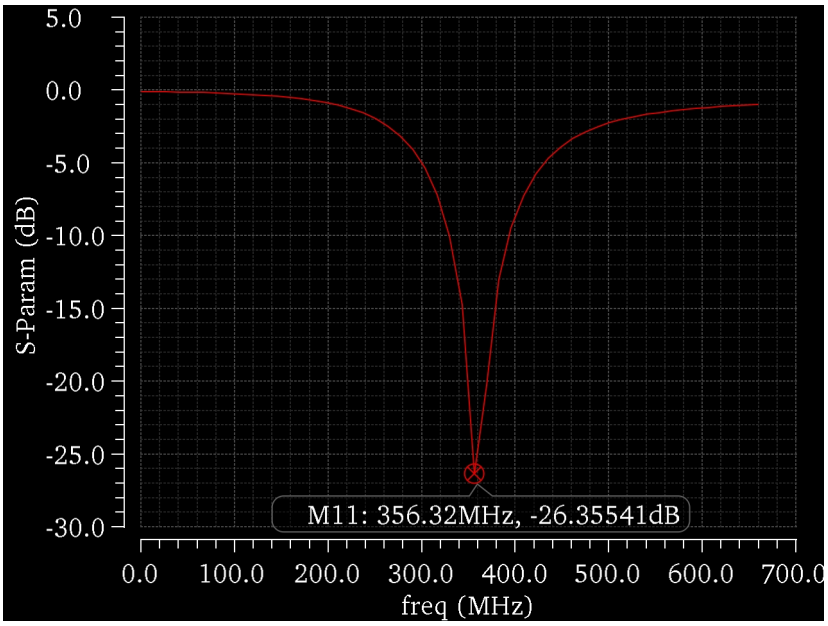

Figure 21: S_{11} for updated LNA

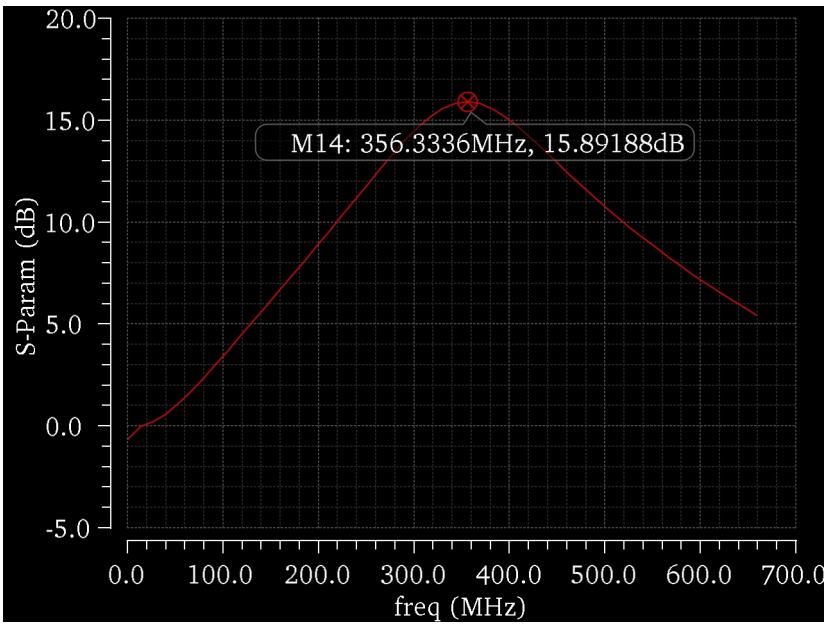

Figure 22: S_{21} for updated LNA

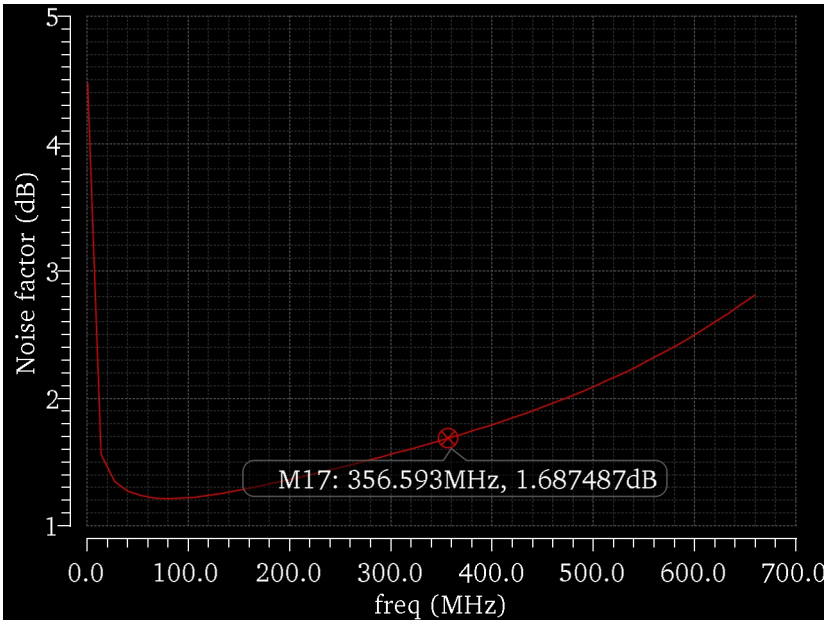

Figure 23: NF for updated LNA

Table 5: Comparison of the performance of the original design and updated design

Parameter	Original Design	Updated Design
S_{11}	-24dB	-26.4dB
S_{21}	17.1dB	15.9dB
NF	2.74dB	1.69dB

In addition to the improved performance, the updated design has significant advantages in terms of ease of testing due to the inclusion of the bias pin, RF probe compatibility, and removal of the control voltage pin.

6.Conclusion

In this course, the LNA designed in ECE 547 was tested and its DC and AC performance was gauged. Unpackaged LNA was tested for an operational range of 350±50MHz. The LNA drew 4mA of current and had a return loss of approximately -8dB. The limitations and issues of the designed LNA were considered and an updated design addressing the major issues was generated in Cadence. The updated LNA has reduced parasitic resistance, improved return loss, lower noise figure, and the ability to probe and provide an external bias voltage.

References

[1] A. Maskay, Tunable Low Noise Amplifier for Wireless Interrogation of a UMaine Surface Acoustic Wave Sensor (Spring 2014, ECE 547)

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Appendix A

(Added here from ECE 547 report for easy referral)

The preliminary design [2] based on inductive source degeneration is shown in Figure 24, which is derived from [3]. An additional bias network consists of M_3 forms a current mirror with M_1 and R_{REF}, which controls the reference current through M_3. Table 6 describes the functions of different components in the LNA.

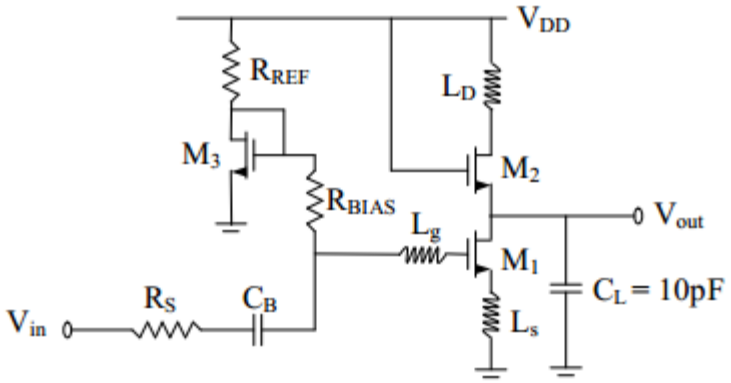

Figure 24. Preliminary Design of LNA based on Inductive Source Degeneration

Table 6. Description of components in LNA Design

Component	**Functionality**
L_s	Input Matching
L_g	Setting operating frequency (Tuning)
L_d	Tuning gain and acting as a bandpass filter with the capacitive load
M_3	Bias transistor
M_2	Increases reverse isolation, reduces the effect of M_1's gate to drain Miller capacitance
C_B	DC blocking capacitor

R_{REF}	Bias resistor to set the current in the current mirror
C_L	Capacitive Load
R_{BIAS}	High resistance so that its equivalent noise current can be neglected

Input Matching

The input matching network for an inductive source degenerated LNA is shown in Figure 25a and its small signal equivalent model is shown in Figure 25b. Input matching in this design only occurs at the frequency where the inductors at the gate and source act in conjunction with the source to generate resonance.

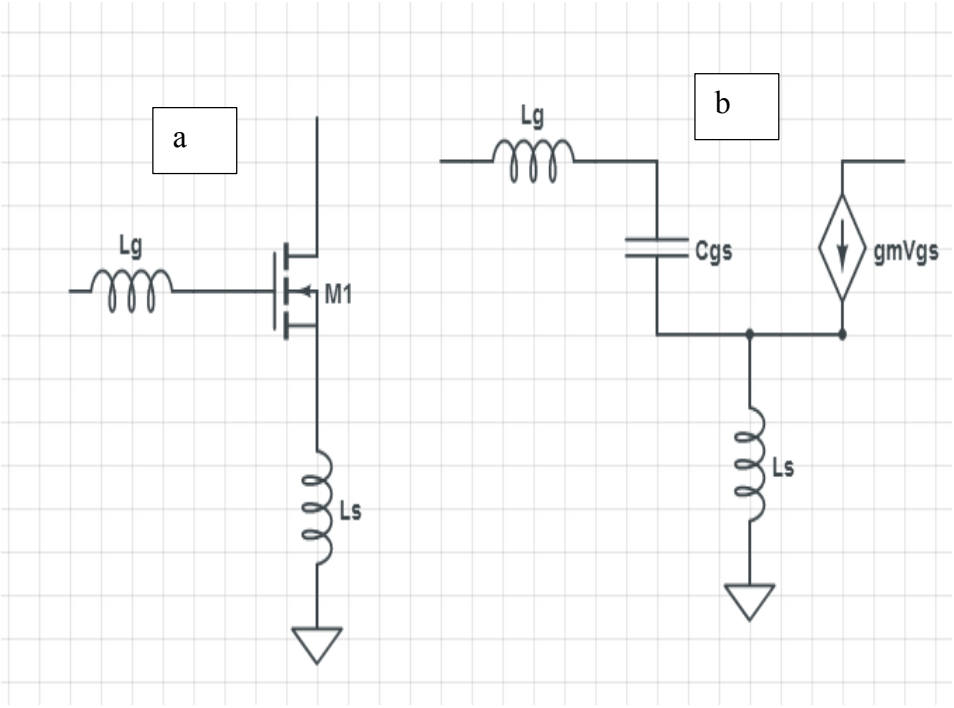

Figure 25.Input Matching for an Inductive Source Degenerated LNA

If a voltage, V_{in}, is applied at the input node in the small signal model, the voltage is given by

$$V_{in} = \frac{I_{in}}{j\omega C_{gs}} + L_g I_{in} + j\omega L_s\left(I_{in} + g_m V_{gs}\right). \quad (1a)$$

By relating V_{in} to the input current, I_{in}, the input impedance is

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{g_m L_s}{C_{gs}} + j[\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}] . \quad (1b)$$

Since, the unity gain frequency is related to the transistor parameters by

$$\omega_T \approx \frac{g_m}{C_{gs}}, \quad (1c)$$

(1b) can be rewritten as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \omega_T L_s + j[\omega\left(L_s + L_g\right) - \frac{1}{\omega C_{gs}}]. \quad (1d)$$

Resonance for this design occurs at

$$\omega_o = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}}, \quad (1e)$$

where, the imaginary part of (1d) disappears and hence matching at this frequency can be obtained using its real part as

$$Z_{in} = \omega_T L_s \quad (1e)$$

Noise Figure/Noise Factor

The noise performance of a LNA can be expressed in terms of either Noise Figure (NF) or Noise Factor (F). Classical two-port noise theory [1] defines noise factor as

$$F = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} . \quad (2a)$$

On the other hand, noise figure is defined as

$$NF = 10\log(F). \quad (2b)$$

For a linear circuit, the noise factor can be expressed in terms of four-noise parameters [1] as

$$F = F_{min} + \frac{[(G_S - G_{opt})^2 + (B_S - B_{opt})^2]R_n}{G_S}, \quad (2c)$$

where, F_{min} is the minimum noise factor, G_s and B_s are real and imaginary parts of the source admittance, G_{opt} and B_{opt} are real and imaginary parts of the optimum source admittance and R_n is the equivalent noise resistance for the circuit.

The absolute minimum possible noise factor is

$$F_{min} = 1 + 2.3[\frac{\omega}{\omega_T}] \quad (2d)$$

Tunable Frequency Implementation

L_g along with C_{gs} controls the operating frequency of the LNA. Frequency tuning capability can be added to the design by adding a variable capacitor in parallel to C_{gs} to increase the effective capacitance between the gate and source terminals of M_1 as shown in Figure 26.

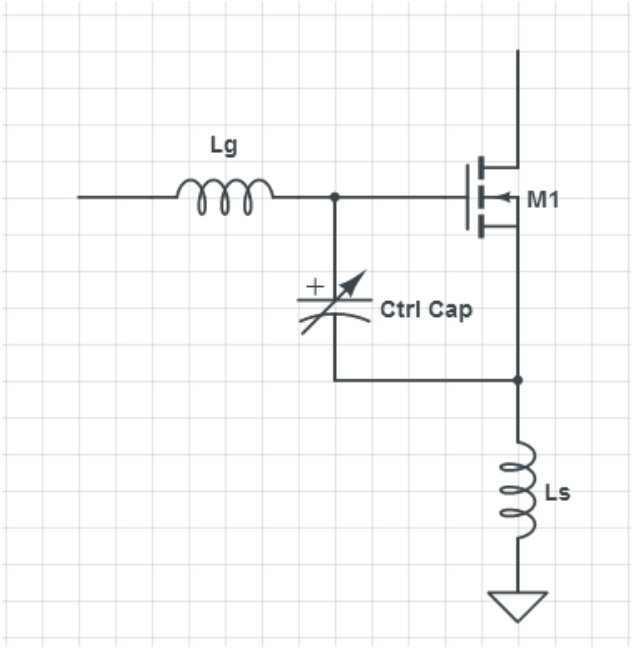

Figure 26. Frequency Tuning capability using a variable capacitor

Circuit analysis was carried out using a two-port network model and S-parameter analysis. It is not practical to measure voltage and currents directly when operating at microwave frequencies (300MHz-3GHz), therefore the best tool to use for this application is S-parameter, which is based on impedance and power considerations. A standard two-port network model based on s-parameters is shown in Figure 27. S_{11} represents the Port 1 reflection coefficient and S_{21} represents the gain from Port 1 to Port 2. For a LNA, the input return loss needs to be minimized whereas, the forward gain has to be maximized.

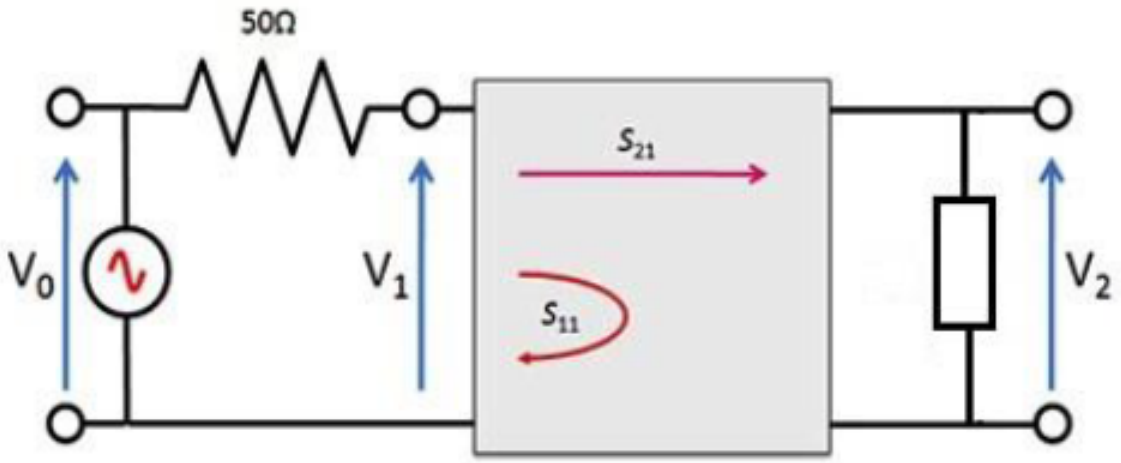

Figure 27.Two Port Network (S-Parameters)

Derivations

The preliminary LNA was designed to operate at a nominal frequency of 330MHz and implemented using 0.18µm CMOS process in Cadence. The primary goal was to design a LNA that could operate at a fixed frequency and the feature of tuning the operating frequency was added later in the design process. Table 7 shows the technology parameters used in the derivations.

Table 7. Technology Parameter Values

Parameter	Value
ε_r	4
ε_o	8.854×10^{-12}F/m
T_{ox}	4.5nm
l	0.18µm
μ_n	0.04

Sizing M_1

Firstly, the capacitance of the gate oxide layer for this technology is

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{T_{ox}} = 7.9 \frac{mF}{m^2}, \tag{3a}$$

[2] shows that the optimum width for the M_1 for noise optimization is

$$W_{OPT} = W_{M1} = \frac{1}{3\omega l C_{ox} R_s} = 2.3mm \ , \tag{3b}$$

where, $l = 0.18\mu m$, $R_s = 50\Omega$, and C_{ox} as derived in (3a).

The other transistor properties that are necessary in the LNA design are C_{gs}, g_m, and ω_T.

$$C_{gs1} = \frac{2}{3} W_{M1} l C_{ox} = 2.14pF \tag{3c}$$

Designing for a M_1 drain current, I_{D1}, of 5mA gives

$$g_{m1} = \sqrt{2\mu_n C_{ox} \frac{W_{M1}}{l} I_{D1}} = 0.2009 \tag{3d}$$

The unity gain frequency, ω_T, can then be calculated using (1c) as

$$\omega_T = \frac{g_{m1}}{C_{gs1}} = 0.929 \frac{Grad}{s^2}. \tag{3e}$$

Inductor Parameters

Designing for an operating frequency, f_o, of 330MHz gives

$$\omega_o = 2\pi f_o \ = 2.07 \frac{Grad}{s^2} . \tag{3f}$$

Using (1e) and the necessity to match the input impedance, R_s, to 50Ω,

$$L_s = \frac{R_s}{\omega_T} = 0.54nH\ . \tag{3g}$$

Rearranging (1e) to solve for L_g provides

$$L_g = \frac{1}{\omega_o{}^2 C_{gs1}} - L_s = 108nH. \tag{3h}$$

As previously mentioned, the inductor at the drain of M_2 (L_d) acts as a bandpass filter with the capacitive load (C_L). Assuming that the capacitive load will have a value close to 10pF,

$$L_d = \frac{1}{\omega_o{}^2 C_L} = 23.3nH \tag{3i}$$

Sizing M_2, M_3, R_{BIAS}, and C_B

Since, the same current flows through M_2 and M_1, M_2 width was chosen to be

$$W_{M2} = 2.3mm. \tag{3j}$$

[1] mentions that sizing M_3 around 7 times smaller than M_1 minimizes power consumption, hence,

$$W_{M3} = \frac{W_{M1}}{7} = 329\mu m.$$

As previously discussed, the noise due to resistors can be reduced by choosing a large resistor so,

$$R_{BIAS} = 5k\Omega\ . \tag{3k}$$

The DC blocking capacitor is chosen to be

$$C_B = 68pF\ i.e.\ X_{C_B} = \frac{1}{\omega_o C_B} \approx 7\Omega\ , \tag{3l}$$

so, that the equivalent reactance due to the capacitor at resonance is insignificant.

Noise Figure

Utilizing the ω_T and ω_o obtained from (3e) and (3f) respectively, (2b) and (2d) can be used to calculate the theoretical minimum noise figure possible for this design as

$$NF_{min} = 10 * \log\left[1 + 2.3\left[\frac{\omega}{\omega_T}\right]\right] = 3.08dB \quad \text{(3m)}$$