Tunable Low Noise Amplifier for Wireless Interrogation of a UMaine Surface Acoustic Wave Sensor

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Abstract

The design, schematic, layout, and simulation of a tunable Low Noise Amplifier (LNA) for wireless interrogation of a one port Surface Acoustic Wave (SAW) resonator based sensor is described in this report. The SAW sensors have resonant frequencies ranging from 285MHz to 345MHz and a high quality factor. The narrowband LNA, which operates between 303MHz and 356MHz, is designed using a 0.18μm CMOS technology in Cadence. Two port analysis of the LNA shows that at 330MHz the LNA has a gain of 12.8dB and Noise Figure (NF) of 3.65dB while drawing 6mA of current. The lowest gain for the design is 11.5dB at 303MHz and the highest noise figure is 3.74dB at 356MHz.

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1.Introduction

This report describes the design, layout, and simulation of a Low Noise Amplifier (LNA) designed for wireless interrogation of Surface Acoustic Wave (SAW) resonators which are used in sensor applications.

A SAW resonator is a one port device which consists of interdigital transducers (IDTs) fabricated on a piezoelectric substrate which transmits information via acoustic waves traveling along its surface as shown in Figure 1. The widths of the IDTs dictate the operating frequency for the resonator.

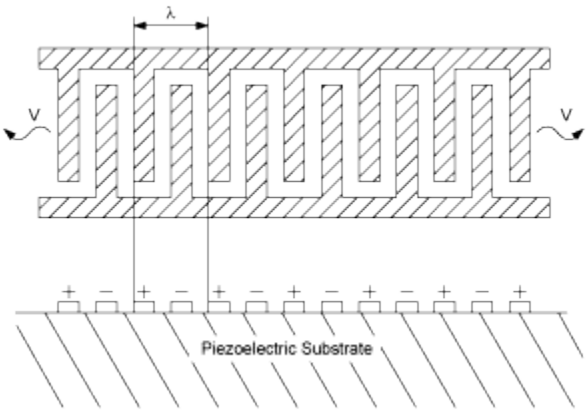

Figure 1. SAW Resonator Structure

University of Maine SAW resonators are fabricated on Lanthanum Gallium Silicate (LGS) substrates using thin film fabrication technology and vary in IDT widths from 2μm to 2.40μm which correlate directly to resonant frequencies ranging from 345MHz to 285MHz. These resonators are used as sensors in harsh environments; hence, the sensor information needs to be transmitted wirelessly. In order to condition the signal at the receiver end, a bandpass filter is

typically used to select the bandwidth of interest and a Low Noise Amplifier (LNA) with the necessary gain and low noise figure to amplify the signal before processing the signal as shown in Figure 2.

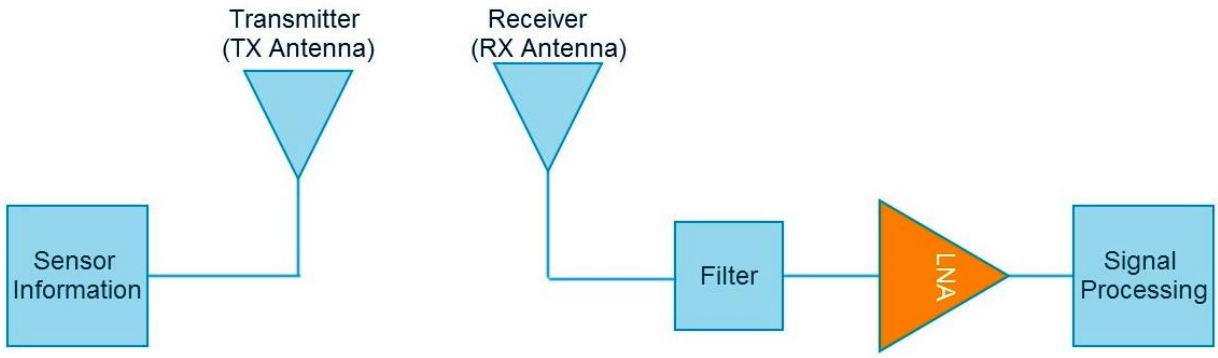

Figure 2. RF Communication Block Diagram

2.Background of LNA

LNA is an essential block in any communication network because it helps condition the information contained in the signal. Five major factors that need to be considered while designing a LNA are high forward gain, low return loss, low noise figure, stability, and high input matching. Based on literature review, there are six common topologies [1] used in the design of a LNA, which are shown in Figure 3.

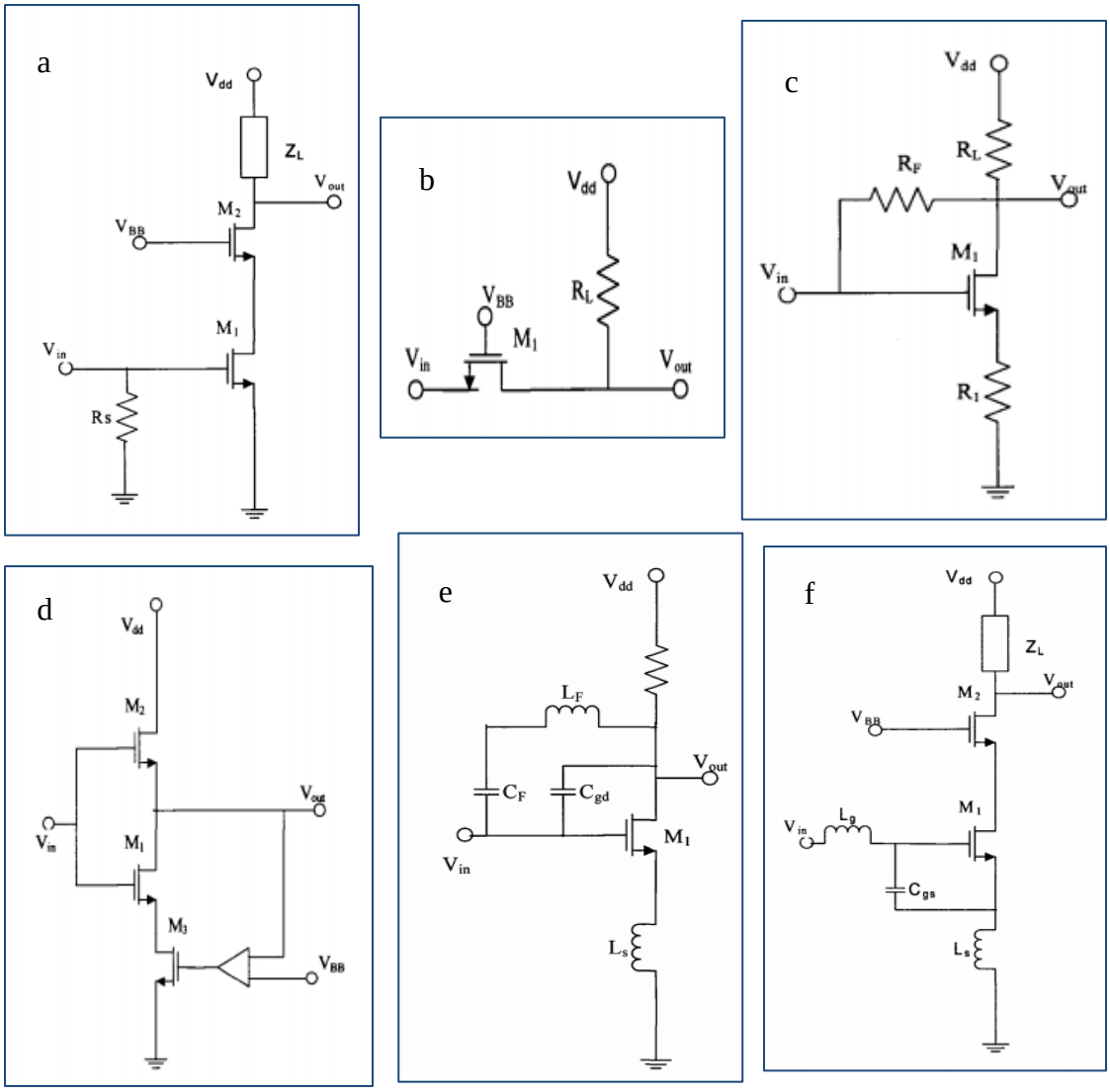

Figure 3. LNA Topologies from Literature : (a) Resistive Termination; (b) Common Gate; (c) Series Shunt Feedback; (d) Current Reuse; (e) Inductor Neutralization; (f) Inductive Degeneration.

Each topology has pros and cons and design issues; Table 1 compares the advantages and disadvantages of the topologies.

Table 1. Comparison of the performance of different LNA topologies

Topology	**Advantages**	**Disadvantages**
Resistive Termination	Good input match	Large NF
Common Gate	Excellent input match	Huge NF and power

Series Shunt Feedback	Broadband I/O match	Stability Issues
Inductive Degeneration	Good Narrowband Match, Small NF	Large Area
Current Reuse	High Gain, Low Power	External Matching Network
Inductor Neutralization	Good Reverse Isolation	Large Area, Stability Issues

Since, the quality factor of SAW resonators is very high (in the order of several thousands), narrowband LNAs are more appropriate than wideband LNAs for this application. Moreover, since space is not an issue as the chip dimension is 1.5mm by 1.5mm, inductive source degenerated LNA is the best choice for a as it allows a low noise figure and good narrowband match as shown in Table 1.

3.LNA Design

The preliminary design [2] based on inductive source degeneration is shown in Figure 4, which is derived from Figure 3f. An additional bias network consists of M_3 forms a current mirror with M_1 and R_{REF}, which controls the reference current through M_3. Table 2 describes the functions of different components in the LNA.

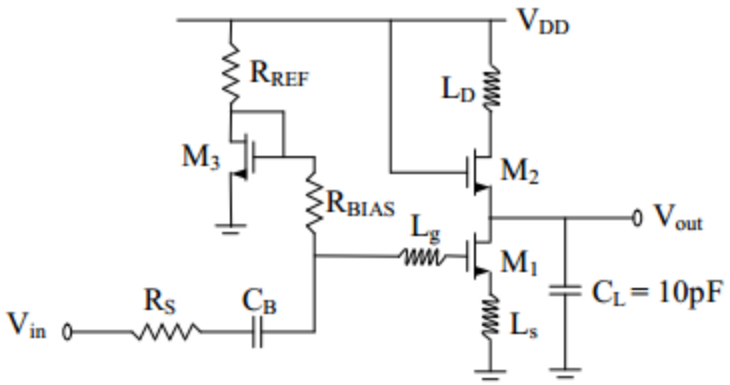

Figure 4. Preliminary Design of LNA based on Inductive Source Degeneration

Table 2. Description of components in LNA Design

Component	**Functionality**
L_s	Input Matching
L_g	Setting operating frequency (Tuning)
L_d	Tuning gain and acting as a bandpass filter with the capacitive load
M_3	Bias transistor
M_2	Increases reverse isolation, reduces the effect of M_1's gate to drain Miller capacitance
C_B	DC blocking capacitor
R_{REF}	Bias resistor to set the current in the current mirror
C_L	Capacitive Load
R_{BIAS}	High resistance so that its equivalent noise current can be neglected

3.1. Theory

Section 3.1.1 to Section 3.1.3 discuss the theory behind input matching, noise figure optimization and implementation of frequency tuning respectively.

3.1.1. Input Matching

The input matching network for an inductive source degenerated LNA is shown in Figure 5a and its small signal equivalent model is shown in Figure 5b. Input matching in this design only occurs at the frequency where the inductors at the gate and source act in conjunction with the source to generate resonance.

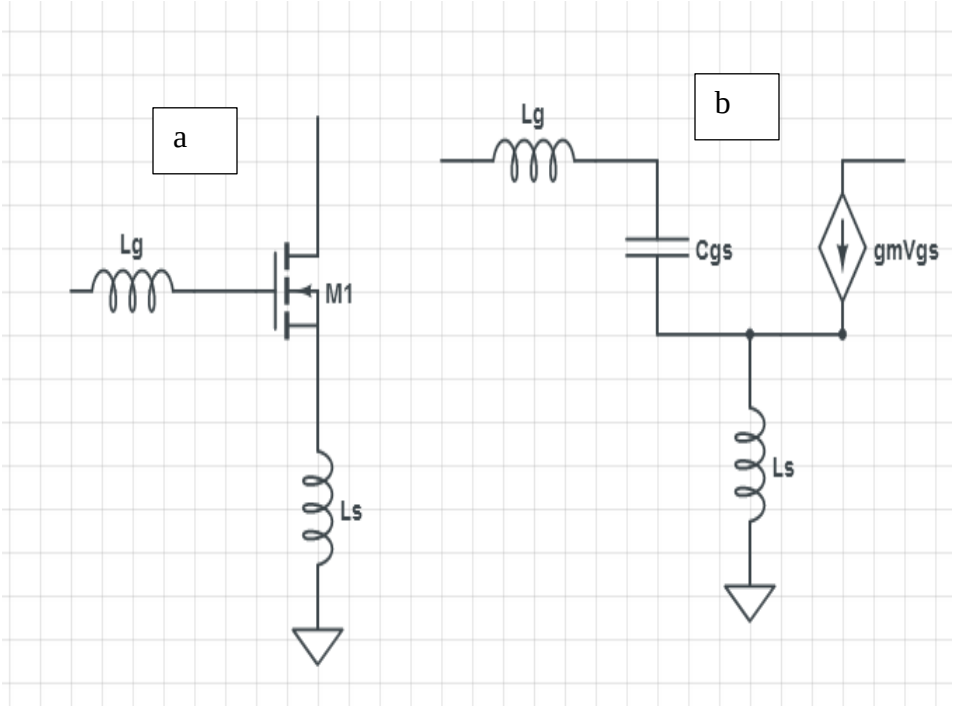

Figure 5.Input Matching for an Inductive Source Degenerated LNA

If a voltage, V_{in}, is applied at the input node in the small signal model, the voltage is given by

$$V_{in} = \frac{I_{in}}{j\omega C_{gs}} + L_g I_{in} + j\omega L_s\left(I_{in} + g_m V_{gs}\right). \quad (1a)$$

By relating V_{in} to the input current, I_{in}, the input impedance is

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{g_m L_s}{C_{gs}} + j\left[\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}\right]. \quad (1b)$$

Since, the unity gain frequency is related to the transistor parameters by

$$\omega_T \approx \frac{g_m}{C_{gs}}, \tag{1c}$$

(1b) can be rewritten as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \omega_T L_s + j[\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}]. \tag{1d}$$

Resonance for this design occurs at

$$\omega_o = \frac{1}{\sqrt{(L_s+L_g)C_{gs}}}, \tag{1e}$$

where, the imaginary part of (1d) disappears and hence matching at this frequency can be obtained using its real part as

$$Z_{in} = \omega_T L_s \tag{1e}$$

3.1.2. Noise Figure/Noise Factor

The noise performance of a LNA can be expressed in terms of either Noise Figure (NF) or Noise Factor (F). Classical two-port noise theory [1] defines noise factor as

$$F = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source}. \tag{2a}$$

On the other hand, noise figure is defined as

$$NF = 10\log(F). \tag{2b}$$

For a linear circuit, the noise factor can be expressed in terms of four-noise parameters [1] as

$$F = F_{min} + \frac{[(G_s-G_{opt})^2+(B_s-B_{opt})^2]R_n}{G_s}, \tag{2c}$$

where, F_{min} is the minimum noise factor, G_s and B_s are real and imaginary parts of the source admittance, G_{opt} and B_{opt} are real and imaginary parts of the optimum source admittance and R_n is the equivalent noise resistance for the circuit.

The absolute minimum possible noise factor is

$$F_{min} = 1 + 2.3[\frac{\omega}{\omega_T}] \quad (2d)$$

3.1.3. Tunable Frequency Implementation

L_g along with C_{gs} controls the operating frequency of the LNA. Frequency tuning capability can be added to the design by adding a variable capacitor in parallel to C_{gs} to increase the effective capacitance between the gate and source terminals of M_1 as shown in Figure 6.

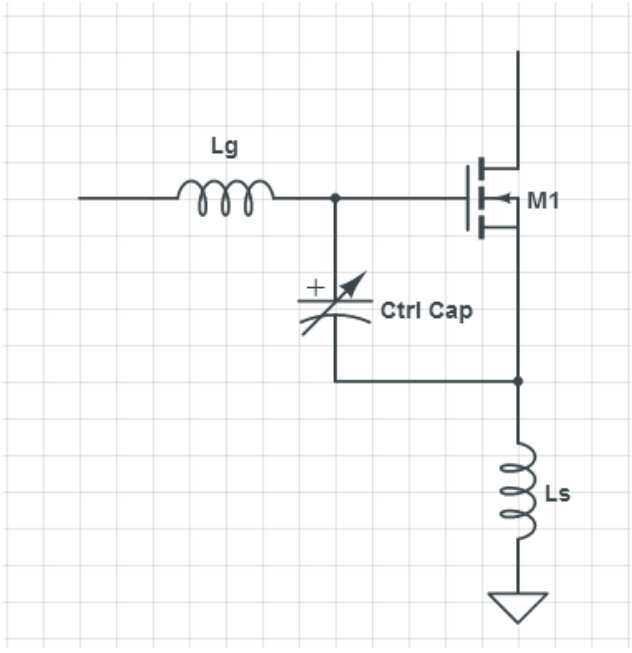

Figure 6. Frequency Tuning capability using a variable capacitor

3.2. Circuit Analysis

Circuit analysis was carried out using a two-port network model and S-parameter analysis. It is not practical to measure voltage and currents directly when operating at microwave frequencies (300MHz-3GHz), therefore the best tool to use for this application is S-parameter, which is based on impedance and power considerations. A standard two-port network model based on s-parameters is shown in Figure 7. S_{11} represents the Port 1 reflection coefficient and S_{21} represents the gain from Port 1 to Port 2. For a LNA, the input return loss needs to be minimized whereas, the forward gain has to be maximized.

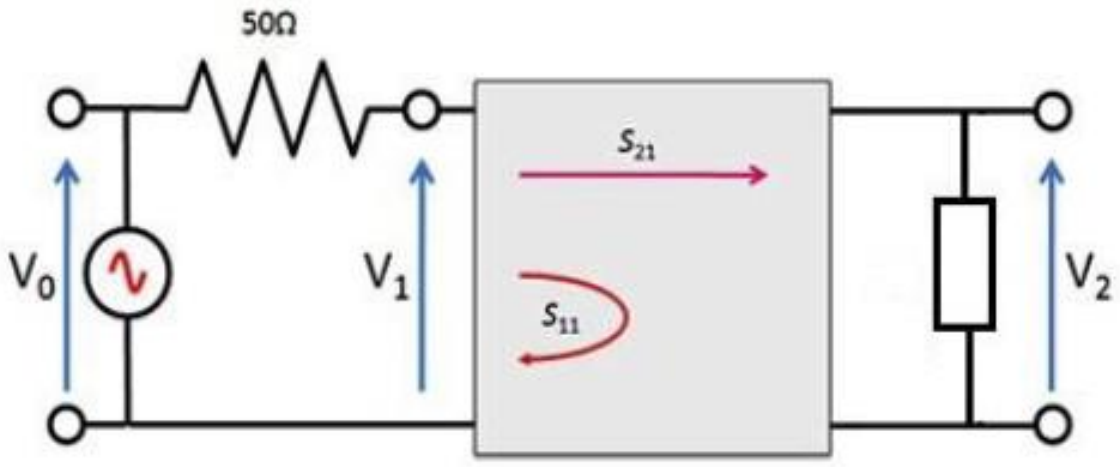

Figure 7.Two Port Network (S-Parameters)

3.3. Derivations

The preliminary LNA was designed to operate at a nominal frequency of 330MHz and implemented using 0.18µm CMOS process in Cadence. The primary goal was to design a LNA that could operate at a fixed frequency and the feature of tuning the operating frequency was

added later in the design process. Table 3 shows the technology parameters used in the derivations.

Table 3. Technology Parameter Values

Parameter	Value
ε_r	4
ε_o	8.854×10^{-12}F/m
T_{ox}	4.5nm
l	0.18μm
μ_n	0.04

3.3.1. Sizing M_1

Firstly, the capacitance of the gate oxide layer for this technology is

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{T_{ox}} = 7.9 \frac{mF}{m^2}, \quad (3a)$$

[2] shows that the optimum width for the M_1 for noise optimization is

$$W_{OPT} = W_{M1} = \frac{1}{3\omega l C_{ox} R_s} = 2.3mm \ , \quad (3b)$$

where, l = 0.18μm, R_s = 50Ω, and C_{ox} as derived in (3a).

The other transistor properties that are necessary in the LNA design are C_{gs}, g_m, and ω_T.

$$C_{gs1} = \frac{2}{3} W_{M1} l C_{ox} = 2.14pF \quad (3c)$$

Designing for a M_1 drain current, I_{D1}, of 5mA gives

$$g_{m1} = \sqrt{2\mu_n C_{ox} \frac{W_{M1}}{l} I_{D1}} = 0.2009 \quad (3d)$$

The unity gain frequency, ω_T, can then be calculated using (1c) as

$$\omega_T = \frac{g_{m1}}{C_{gs1}} = 0.929 \frac{Grad}{s^2}. \quad (3e)$$

3.3.2. Inductor Parameters

Designing for an operating frequency, f_o, of 330MHz gives

$$\omega_o = 2\pi f_o = 2.07 \frac{Grad}{s^2}. \quad (3f)$$

Using (1e) and the necessity to match the input impedance, R_s, to 50Ω,

$$L_s = \frac{R_s}{\omega_T} = 0.54nH. \quad (3g)$$

Rearranging (1e) to solve for L_g provides

$$L_g = \frac{1}{\omega_o{}^2 C_{gs1}} - L_s = 108nH. \quad (3h)$$

As previously mentioned, the inductor at the drain of M_2 (L_d) acts as a bandpass filter with the capacitive load (C_L). Assuming that the capacitive load will have a value close to 10pF,

$$L_d = \frac{1}{\omega_o{}^2 C_L} = 23.3nH \quad (3i)$$

3.3.3. Sizing M_2, M_3, R_{BIAS}, and C_B

Since, the same current flows through M_2 and M_1, M_2 width was chosen to be

$$W_{M2} = 2.3mm. \quad (3j)$$

[1] mentions that sizing M_3 around 7 times smaller than M_1 minimizes power consumption, hence,

$$W_{M3} = \frac{W_{M1}}{7} = 329\mu m.$$

As previously discussed, the noise due to resistors can be reduced by choosing a large resistor so,

$$R_{BIAS} = 5k\Omega \ . \tag{3k}$$

The DC blocking capacitor is chosen to be

$$C_B = 68pF \ i.e. X_{C_B} = \frac{1}{\omega_o C_B} \approx 7\Omega \ , \tag{3l}$$

so, that the equivalent reactance due to the capacitor at resonance is insignificant.

3.3.4. Noise Figure

Utilizing the ω_T and ω_o obtained from (3e) and (3f) respectively, (2b) and (2d) can be used to calculate the theoretical minimum noise figure possible for this design as

$$NF_{min} = 10 * \log[1 + 2.3\left[\frac{\omega}{\omega_T}\right]] = 3.08dB \tag{3m}$$

4.Implementation in Cadence

Upon completion of the derivation of parameters, the 330MHz LNA was implemented in the schematic view in Cadence as shown in Figure 8. As expected some parameter adjustment was necessary as schematic was based on the CMRF7SF library instead of ideal components. Sections 4.1 and 4.2 discuss the analysis process and design optimization respectively.

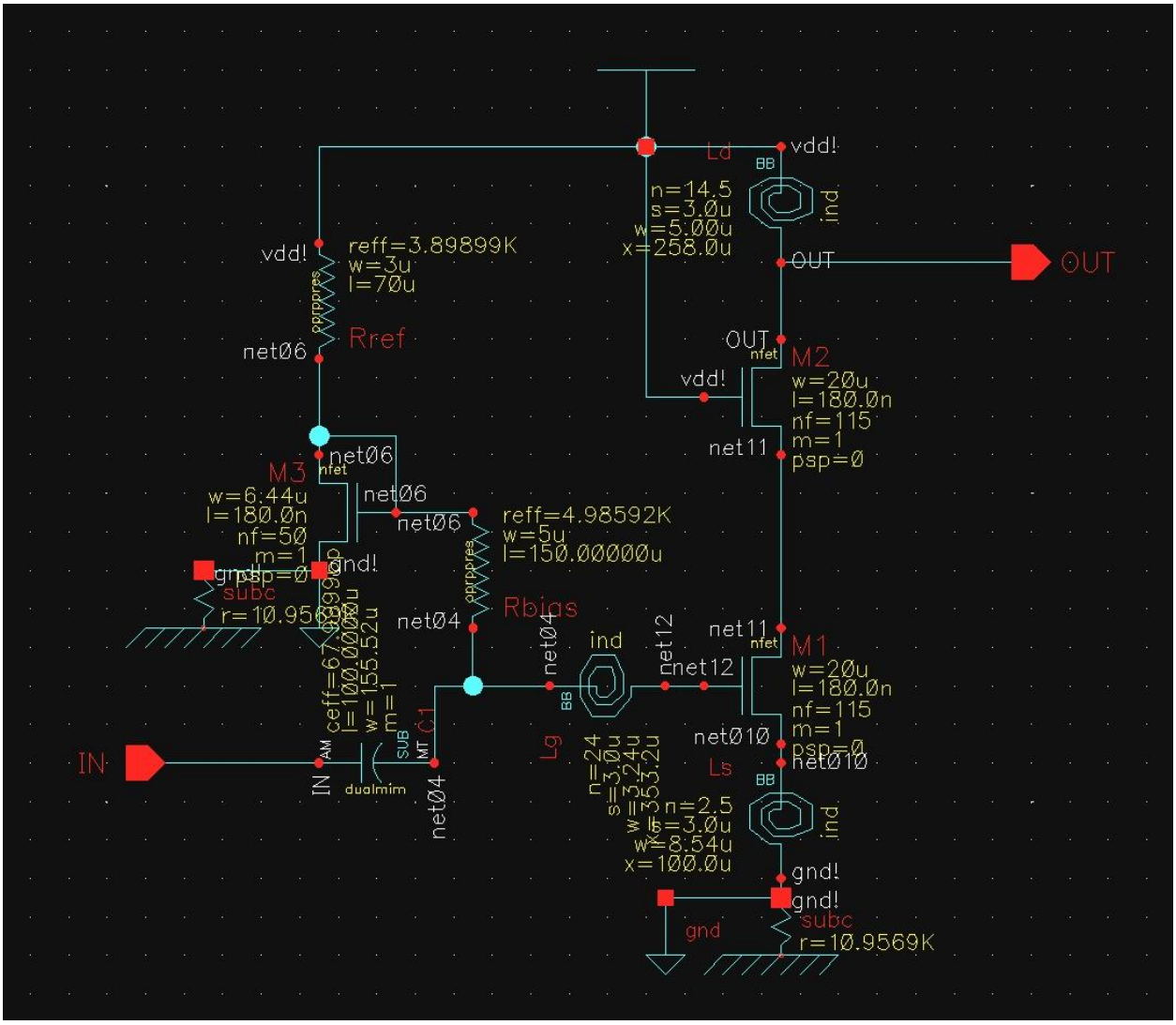

Figure 8. 330MHz LNA Schematic in Cadence

4.1. Analysis

As mentioned in Section 3.2, S-parameter analysis is the best tool for circuit analysis at microwave frequencies. The test circuit in Figure 9 was implemented in Cadence using the LNA in Figure 8 and two ports. Port 1 had an impedance of 50ohms and Port 2 had a reactance of

48.2ohms (10pF C_L).

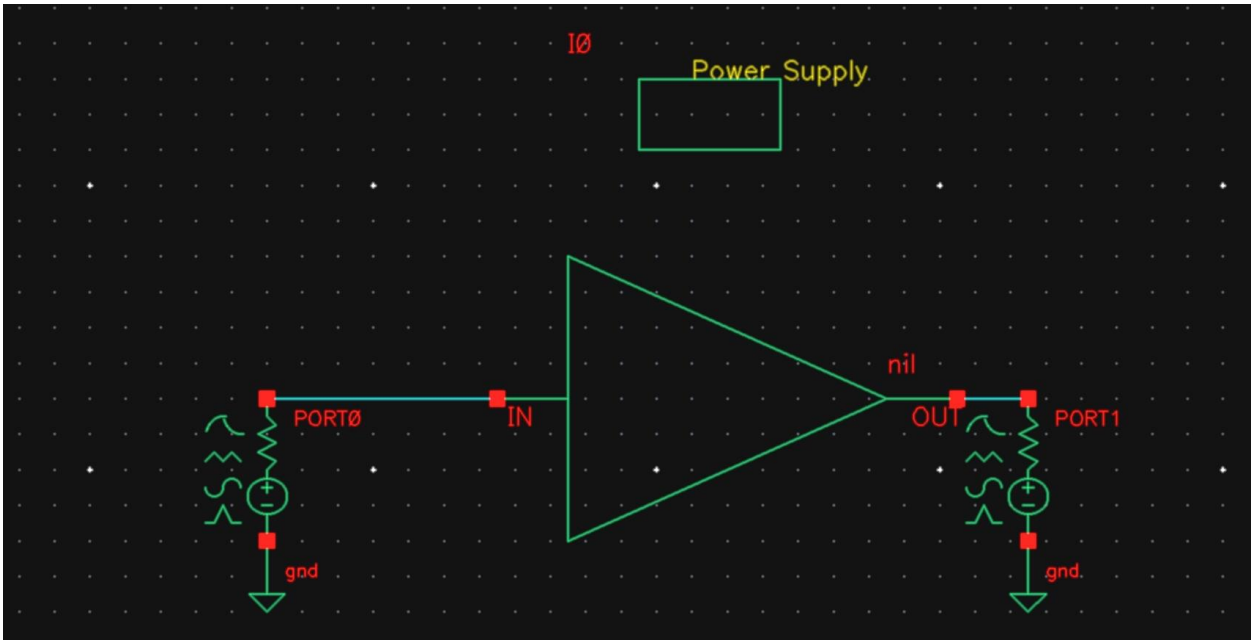

Figure 9. LNA Test Circuit

Utilization of ports instead of voltage or current sources to drive the input node allows the use of 'sp analysis' (s-parameter analysis) in Cadence. 'sp analysis' allows the user to perform a frequency sweep for a two port network and extract the s-parameters for the network. In addition, it has an added feature of carrying out noise analysis between the input and output ports.

4.2. Design Optimization

In order to optimize the LNA design, various design variables were adjusted while monitoring the current drawn, gain, and noise figure.

4.2.1. Bias Network (R_{REF})

Adjusting R_{REF} changes the bias current for M_1 and M_2. During the initial design process, a 5mA was chosen as the reference current through R_{REF}, but the gain was lower than expected.

Decreasing the resistance of R_{REF} increases the current drawn, which in turn increases the gain and lowers the NF. Therefore, an R_{REF} value was chosen after performing a DC analysis by sweeping the resistance of R_{REF} while monitoring the current drawn by M_1 as shown in Figure 10. Although, lowering the resistance improves the performance, the power constraint limits the choice of R_{REF}; hence, R_{REF} was chosen to be 3.9kΩ which meant that around 5.9mA of current would be drawn by M_1.

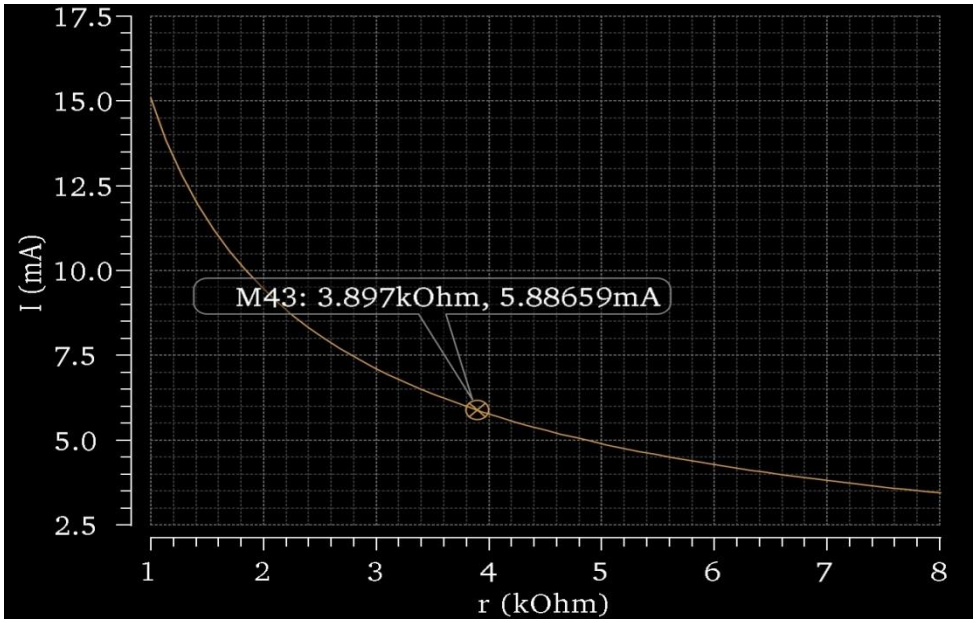

Figure 10. Current drawn by M_1 as a function of R_{REF}

4.2.2. Varying the Number of Fingers of M_1 and M_2

Another variable that played a significant role in the performance of the amplifier was the number of fingers (nf) for M_1 and M_2 transistors. The plots for the gain and NF as functions of the number of fingers are shown in Figure 11 and Figure 12 respectively. The gain and NF both suffer severely at lower values of nf, which is most likely due to the high gate resistance.

However, there was also an upper limit to nf where the noise figure started increasing. Hence, the optimum value of nf was chosen to be 115 for both M_1 and M_2.

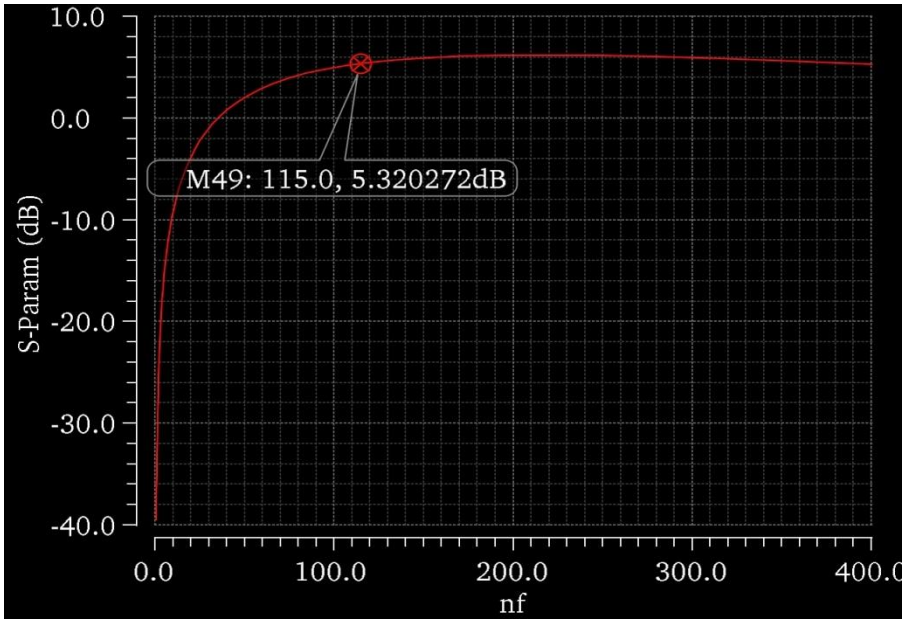

Figure 11. Gain versus Number of Fingers of M_1

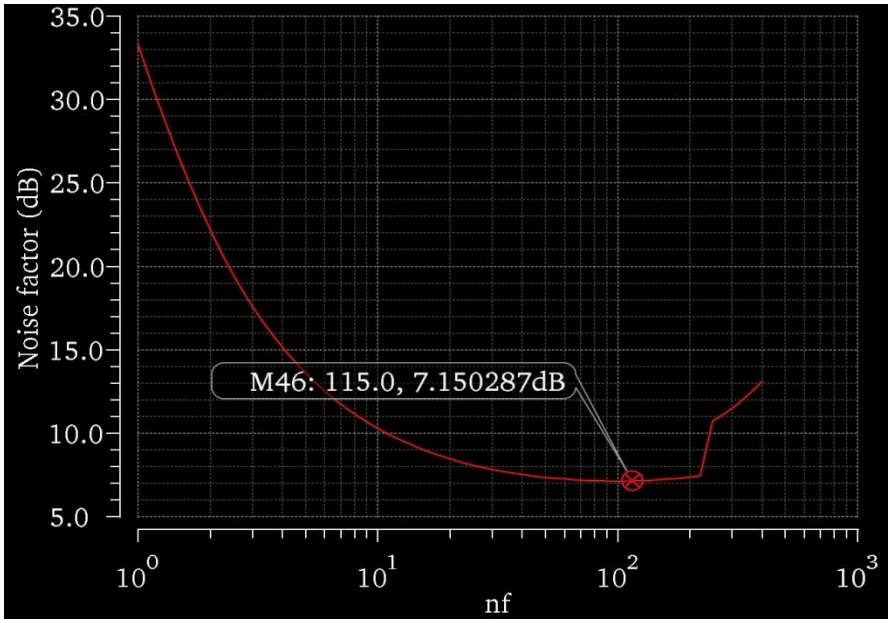

Figure 12. NF versus Number of Fingers of M_1

4.2.3. Varying C_B

Ideally C_B is set to a value such that its effective reactance at the operating frequency is negligible i.e. as large as possible. However, in order to optimize the design, noise and gain analysis were conducted for different values of C_B as shown in Figure 13. As can be seen from the plot, for lower capacitance values, the gain drops and the NF is higher. However, there is a direct correlation between the capacitance value and capacitor size. Therefore, C_B = 68pF was chosen as a compromise between capacitor size and capacitance value.

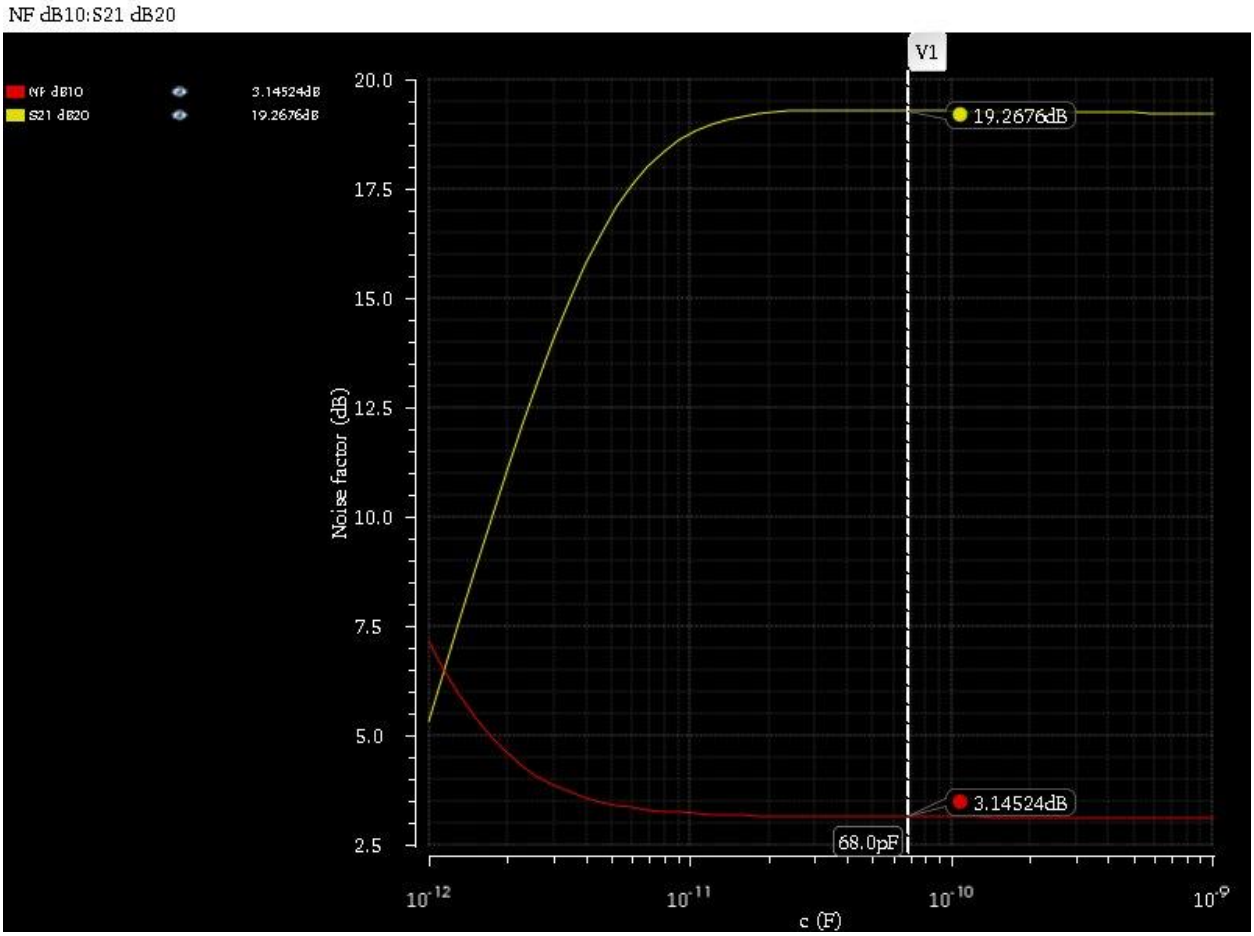

Figure 13. NF versus C_B

4.2.4. *Adding Frequency Tuning*

Frequency tuning capability was implemented in Cadence by using an instantiation of DIFFHAVAR from CMRF7SF library which consists of two hyperabrupt (HA) junction varactor diodes with their cathodes tied together. The two anodes of the DIFFHAVAR were connected to the gate and source terminals of M_1 and a control (Ctrl) voltage was fed at the cathode to vary the capacitance between the gate and source terminals of M_1 as shown in Figure 14.

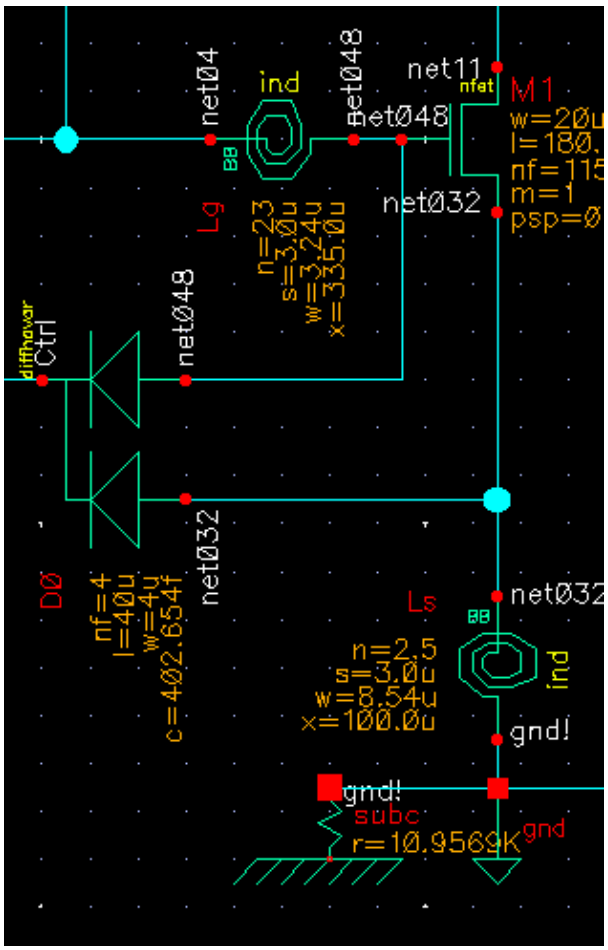

Figure 14. Implementation of Frequency Tuning using DIFFHAVAR

The capacitance range of the HA varactor diodes is determined by the size of the device (W x L x #Anodes) i.e. the width (W), length, (L) and the number of anodes (#Anodes). The

control voltage applied to the cathode terminal can range between 0V and 6V. Table 4 shows the relationship between the range of capacitance obtainable using the HA varactor diode of a particular size.

Table 4. HA varactor diode size and capacitance range relation

Device Size W x L x #Anodes	Minimum Capacitance	Maximum Capacitance
0.8µm x 10µm x 10	0.06pF	0.26pF
2.0µm x 20µm x 20	0.04pF	2.4pF
4.0µm x 40µm x 4	0.03pF	2pF
40µm x 40µm x 2	1.5pF	10pF

After simulating the design with ideal voltage variable capacitors, it was determined that the DIFFHAVAR with two HA varactor diodes 4.0µm x 40µm x 4 provided the widest frequency range in the region of interest (300MHz to 350MHz). Figure 15 shows how the capacitance varies with the applied voltage for the 4.0µm x 40µm x 4 HA varactor diode.

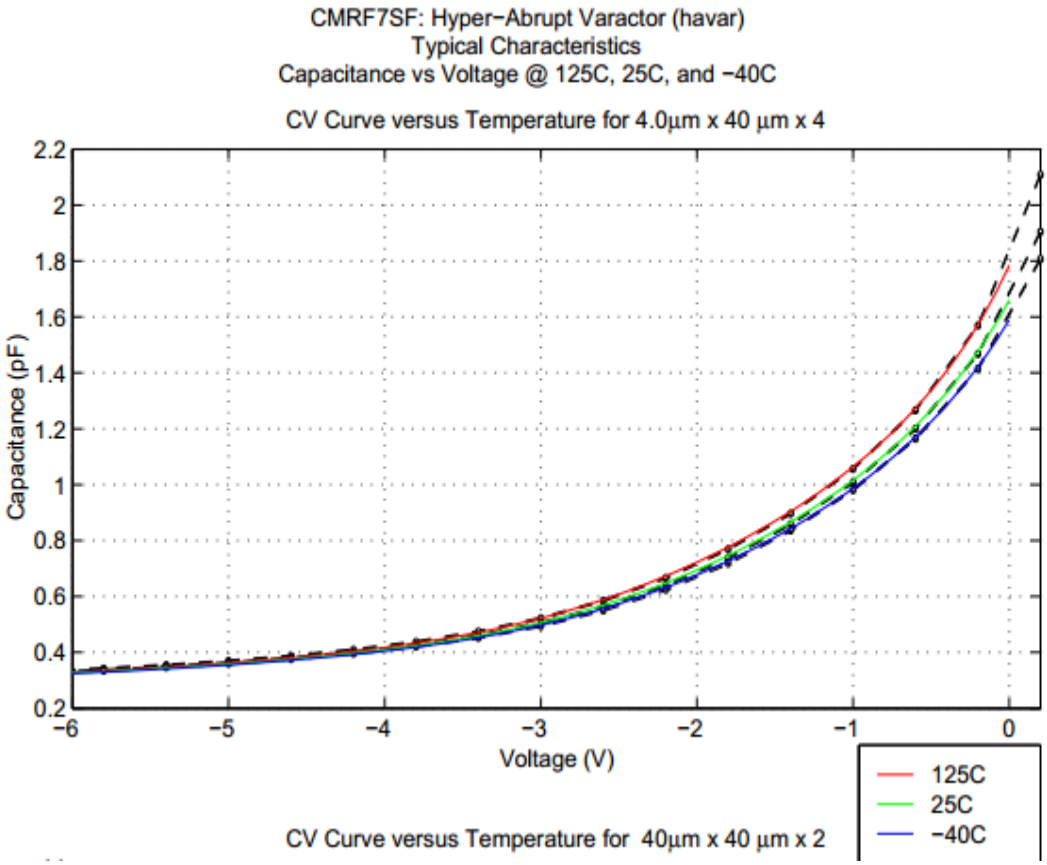

Figure 15. 4.0µm x 40µm x 4 HA varactor voltage versus capacitance (for different temperatures)

5.Layout

Upon the completion of the schematic verification and simulation, the layout for the design was initiated. The major goals for the circuit layout were making the layout compact, reducing parasitics by making short traces and using higher level metals whenever possible.

5.1. LNA without Pins

Figure 16 shows the layout of the proposed LNA without the ring and ESD devices. The overall dimension for this portion was 648um by 552um. The design passed DRC, ESD DRC, floating gate, and LVS checks. It was also simulated with bond pad parasitics and operated as expected.

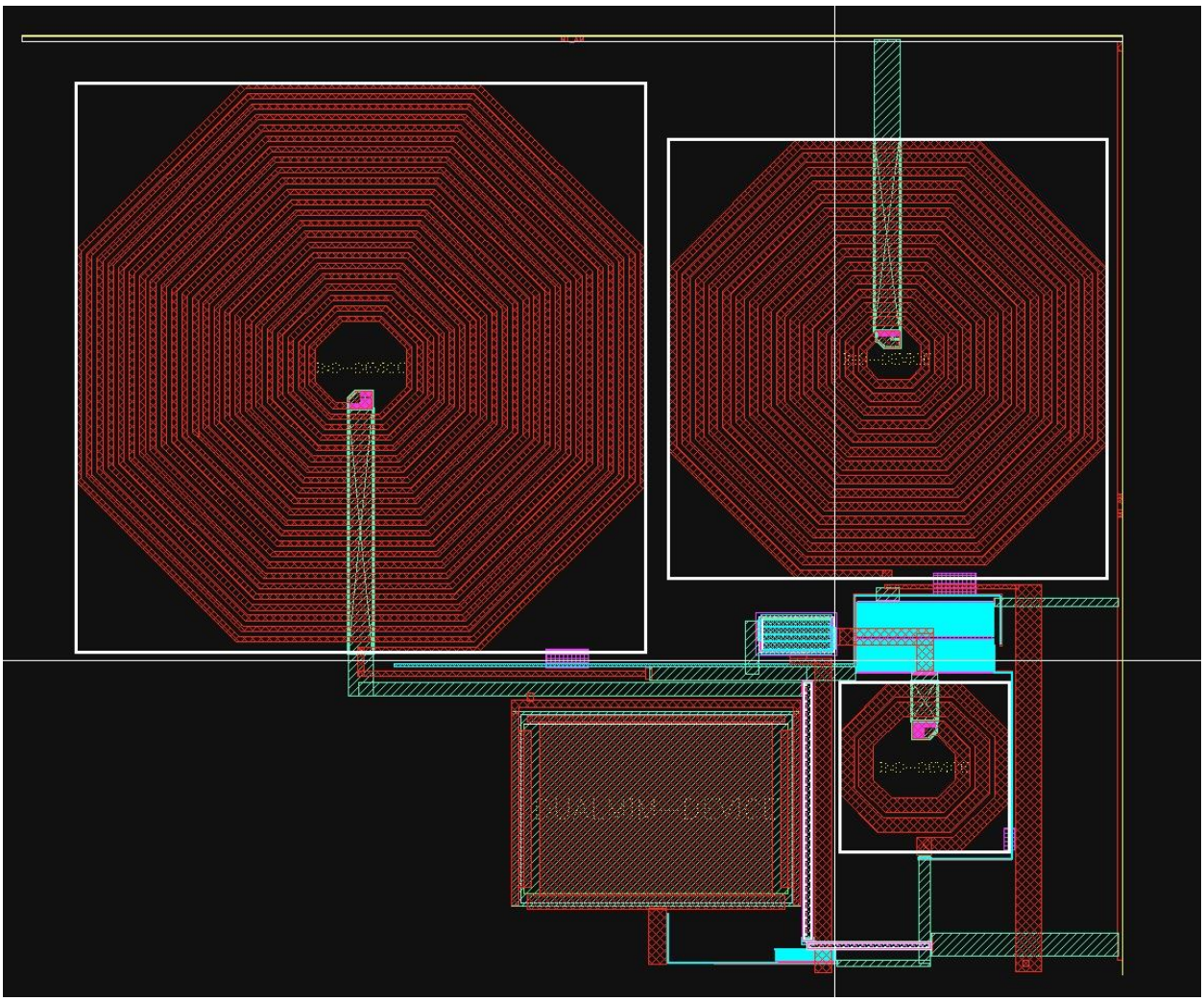

Figure 16. Layout of the proposed LNA (Without Pins and the ring)

5.2. Final Layout

The final layout including the pins and ESD devices is shown in Figure 17. The design occupies 847um by 675um on the ring. The pins with the lowest parasitics were chosen for the input and output signal. The pin assignment is provided in Table 6 in the Appendix. The final design passed DRC, ESD DRC, floating gate, and LVS checks. The simulation for the overall design is discussed in Section 6.

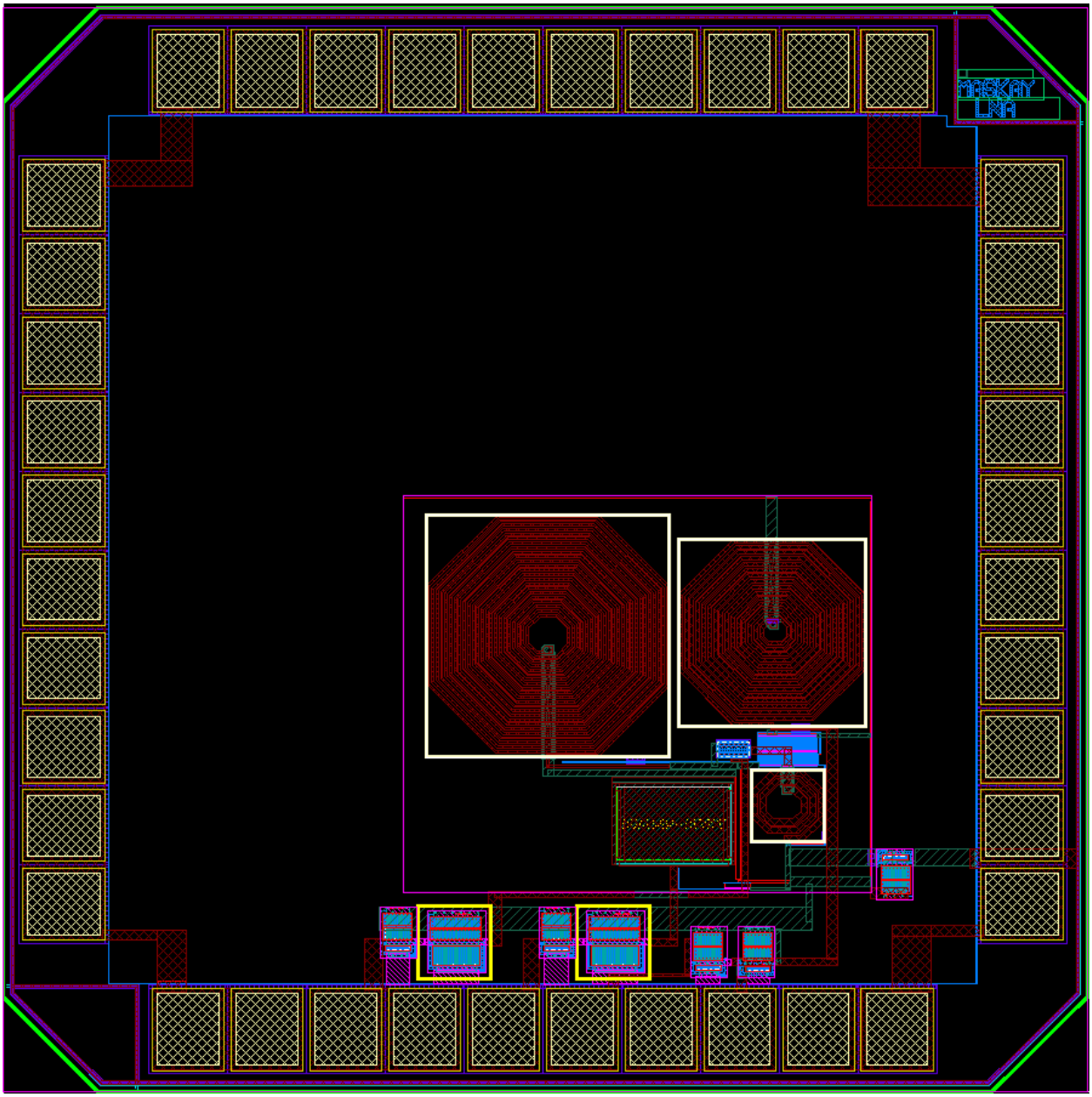

Figure 17. Final Layout

6.Simulation

The final simulation was carried out using the test circuit shown in Figure 18. The LNA has two inputs: (1) the control voltage to tune the amplifier and (2) the input voltage to be amplified. As

mentioned in Section 4.1, Port 1 has an impedance of 50ohms and Port 2 has a reactance of 48.2ohms (10pF C_L).

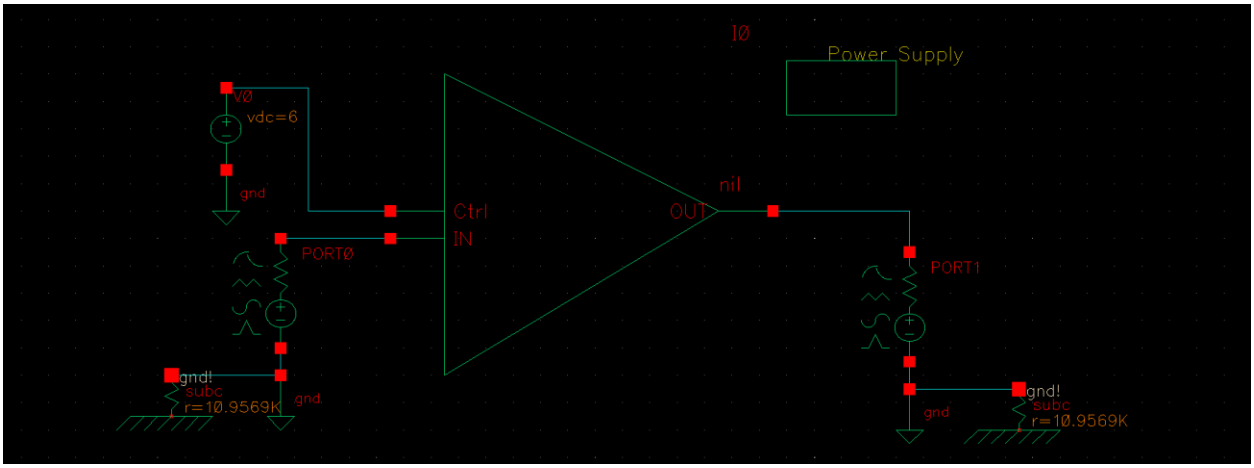

Figure 18. Final Simulation Circuit

The control voltage (Ctrl) was varied from 0V to 6V and a SP frequency sweep was carried out along with noise analysis to observe S_{11}, S_{21}, and NF. As the voltage was varied from 0V to 6V, the operating frequency varied from 356MHz to 303MHz. The gain, S_{11}, and NF increase with increasing frequency. Table 5 shows the simulation results for control voltages of 0V, 1.5V, and 6V.

Table 5. Simulation Results

Control Voltage (V)	Operating Frequency (MHz)	S_{11} (dB)	S_{21} (dB)	NF (dB)
0	356	-24.2	17.1	3.74
6	303	-31.0	11.5	3.57
1.5	330	-28.4	12.8	3.65

Figure 19 shows the S-parameter and noise simulation results for a control voltage of 6V. S_{11} (Yellow), S_{21} (Green), and NF (Red) are plotted. As can be seen from the figure, at the operating

frequency of 303MHz, the input port return loss is very good at -31dB, the noise figure is around 3.6dB; however, the gain is quite low at 11.5dB.

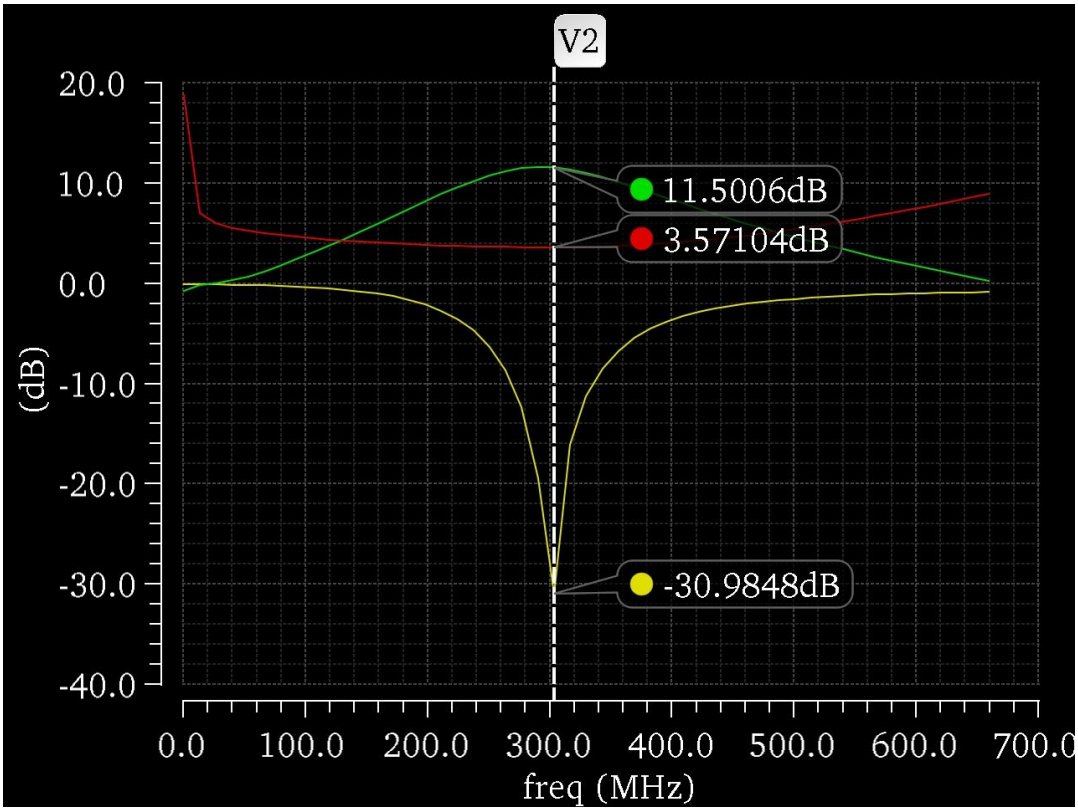

Figure 19. Two Port Simulation Results for a control voltage of 6V

Figure 20 shows the simulation results for the upper frequency limit (356MHz) which occurs when the control voltage is set to 0V. The gain, return loss, and NF are 17.1dB, -24.2dB and 3.74dB respectively. Compared to an operating frequency of 303MHz, the gain improved, but the return loss and NF declined.

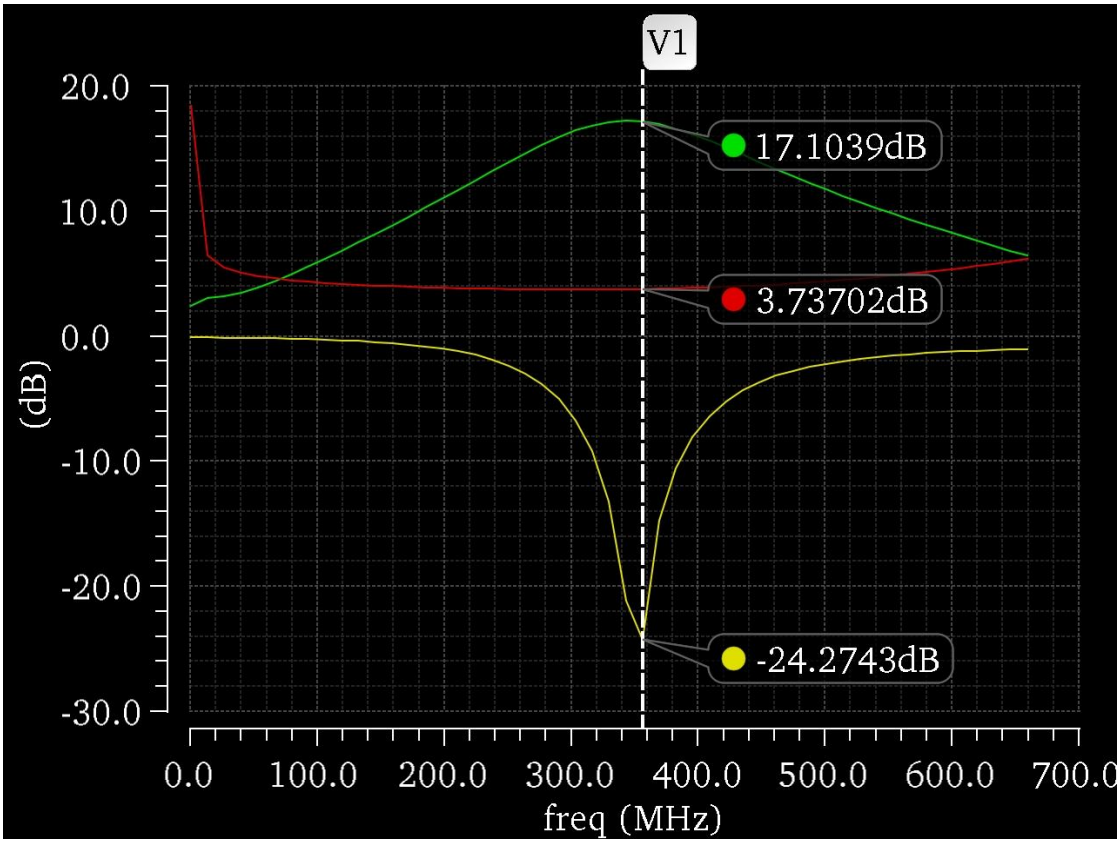

Figure 20.Two Port Simulation Results for a control voltage of 0V

Figure 21 shows the simulation result for a control voltage of 1.5V which translates to an operating frequency of 330MHz. Since, most of the UMaine SAW sensors have a nominal frequency of 330MHz, this result is presented here. The gain, return loss, and NF are 12.8dB, -28.4dB and 3.65dB respectively.

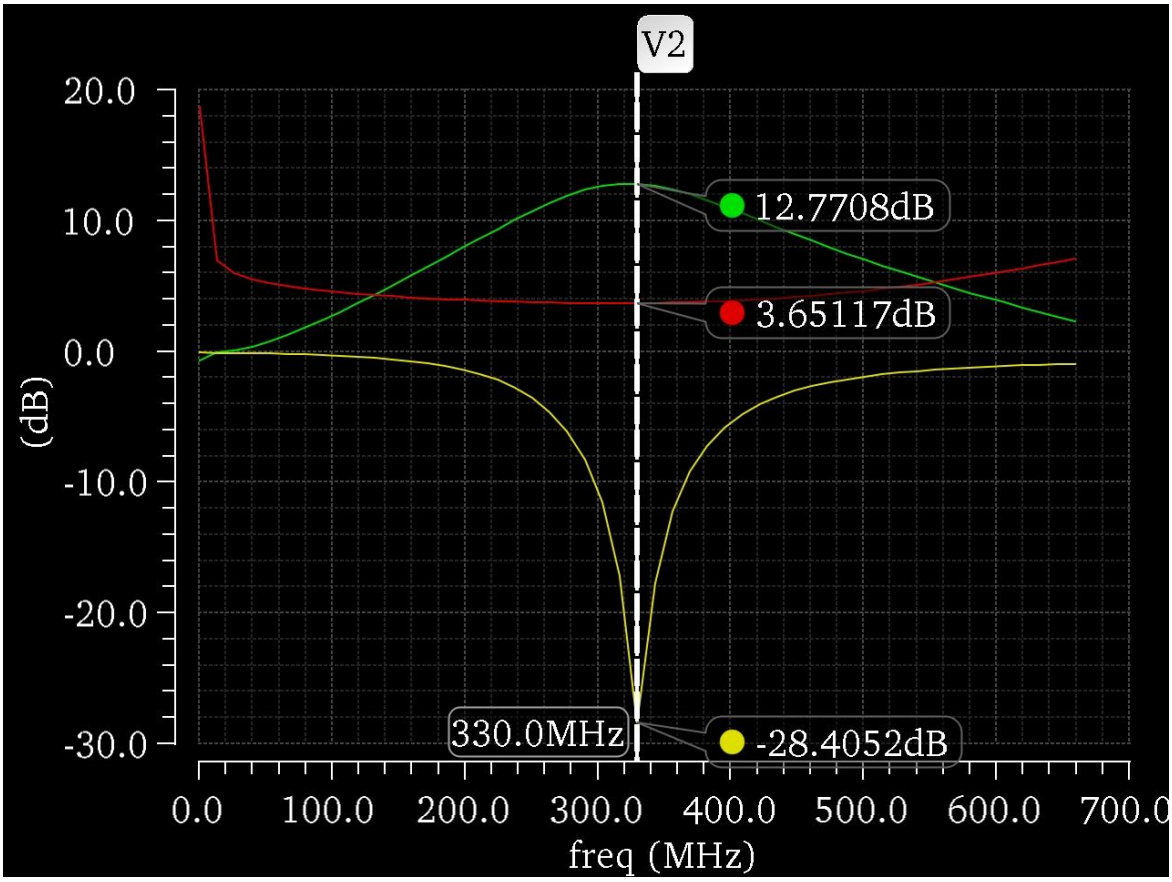

Figure 21.Two Port Simulation Results for a control voltage of 1.5V

The simulation results show that the designed LNA operates between 303MHz and 356MHz with a highest NF of 3.74dB and a lowest gain of 11.5dB.

7.Plan for Testing

The design was completed in Cadence and the simulation verified the performance of the LNA. The design has been sent to MOSIS for verification and fabrication. However, testing wasn't carried out this semester. Below are the instructions to carry out testing:

1. Connect Pin 30 to an input sinusoidal signal at 330MHz.
2. Connect a 1.8V (VDD) DC source to Pin 32, 33.

3. Connect GND to Pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 34, 35, 36, 37, 38, 39, 40.
4. Connect Pin 28, 29 to a DC supply generating a control voltage that can be varied between 0V and 6V.
5. Connect Pin 32 to a Spectrum Analyzer or a High Frequency Oscilloscope to verify the output.

8.Possible Improvements

A number of added features and improvements could be pursued in future work, which are discussed in this section.

8.1. Increase Gain

The gain of the LNA can be increased by adding a second amplifying stage. Since, the noise in the circuit is dominated by the first stage, the noise figure shouldn't change significantly by adding a second stage.

Decreasing the noise figure could be a challenge since it is heavily dependent on component parameters and the current LNA design was optimized as much as possible. However, if the component parameters can be adjusted without changing the performance significantly, the noise figure can be improved.

8.2. Wider Dynamic Range for Tuning

Currently the range of frequencies that the LNA operates is between 303MHz and 356MHz. However, UMaine SAW sensors operating frequencies range from 285MHz to 345MHz. Therefore, the design can optimized to operate in the correct range by shifting the operating

range towards lower frequencies. In addition, a wider range can be obtained if the DIFFHAVAR capacitance range can be increased.

8.3. Adaptive Tuning instead of Manual Tuning

At present, the control voltage to the LNA is varied manually. However, the resonant frequency of the SAW sensor shifts with temperature which is how it can be used as a sensor. Hence, an adaptive frequency tuning would be ideal where the LNA can be notified of the operating frequency of the SAW at that instant to automate the control voltage.

9.Conclusion

During the spring semester of 2014, a tunable low noise amplifier for wireless interrogation of a one port SAW resonator based sensor was design using 0.18μm technology using Cadence. The amplifier was based on an inductive degeneration configuration and operated between 303MHz and 356MHz. The simulation of LNA was performed using Two-port analysis to verify that it had a relatively decent gain, low noise figure and narrowband frequency tuning capability. At 330MHz the LNA has a gain of 12.8dB and Noise Figure (NF) of 3.65dB while drawing 6mA of current. The lowest gain for the design is 11.5dB at 303MHz and the highest noise figure is 3.74dB at 356MHz.

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Appendix

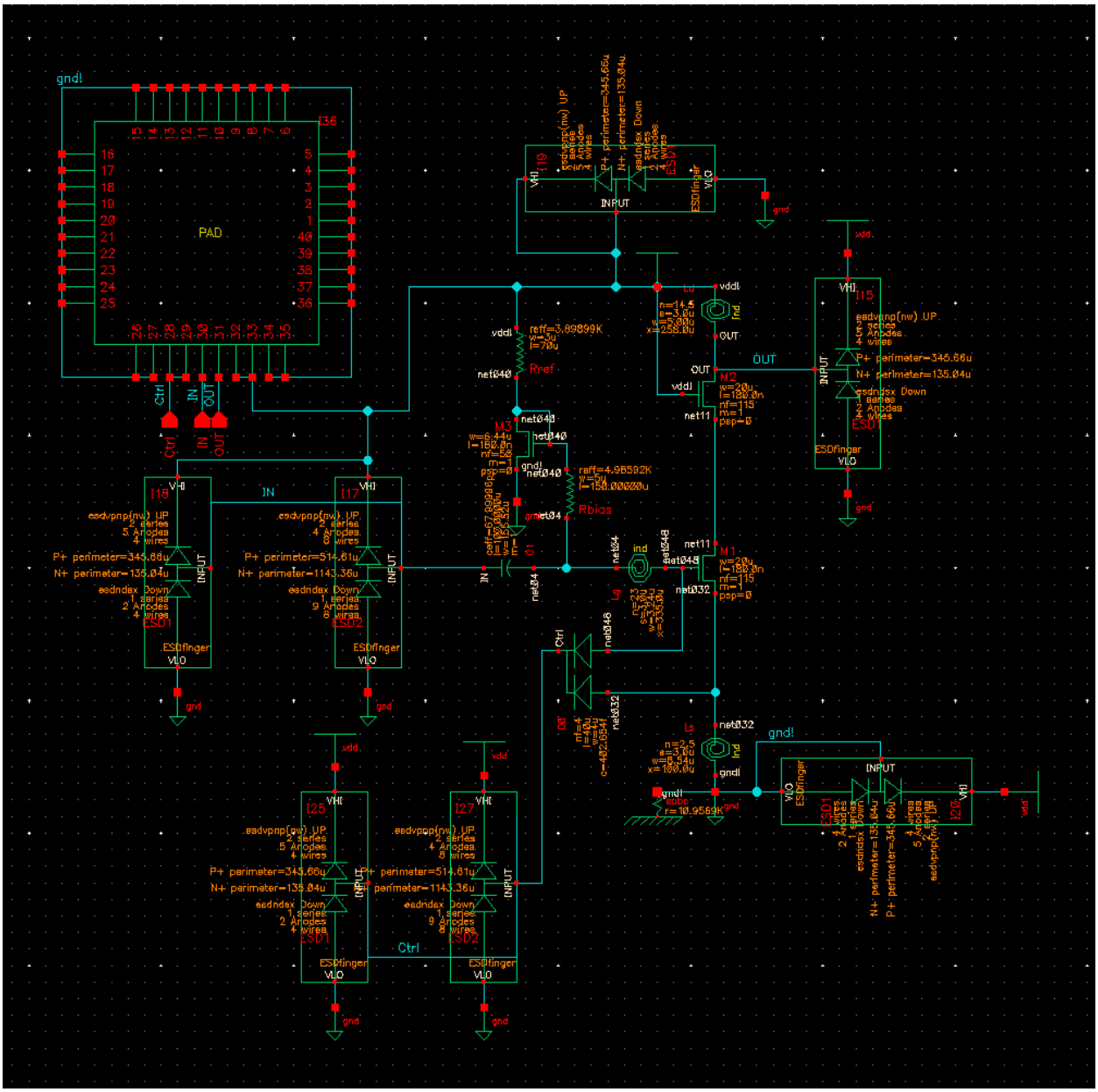

Figure 22.Final Schematic With Pins

Table 6. Final Pin Assignment

Pins	**Assignment**
30	IN
31	OUT
28,29	CTRL
32,33	VDD
1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19, 20,21,22,23,24,25,26,27,34,35,36,37,38,39,40	GND