Digital Phase Locked Loop

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1 Abstract

DPLLs are used widely in communications systems. As a study of these devices, two DPLLs are designed and layed out in a 0.5um CMOS process. One is has a 30MHz starved inverter VCO, a programmable divider and a phase frequency detector. The second consists of a 400MHz differential inverter VCO, a fixed divider and an XOR phase detector. Both devices are layed out together on a 1.5x1.5mm die.

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2 Introduction

2.1 Phase Locked Loops (PLL)

A phase locked loop is a device which generates a clock and sychronizes it with an input signal. The input signal can be data or another clock. The best known application of PLLs is *clock recovery* in communication. When an signal of a known frequency is being recieved often a synchronized clock is required to time circuitry which is processing the incoming signal. Another very common application is *frequency synthesis*. In frequency synthesis PLLs are used to generate a clock which is based on a clock already existing. Often the newly generated clock will be at a multiple of the original frequency.

2.2 Digital PLLs (DPLL)

Digital PLLs are a type of PLL used to sychronize digital signals. While DPLLs input and outputs are typically all digital, they do have internal functions which are dependent on analog signals. There are four basic components of a DPLL.

- Phase Detector
- Loop Filter
- Voltage Controlled Oscillator (VCO)
- Divider

The signal flow through these components is shown in Figure 1.

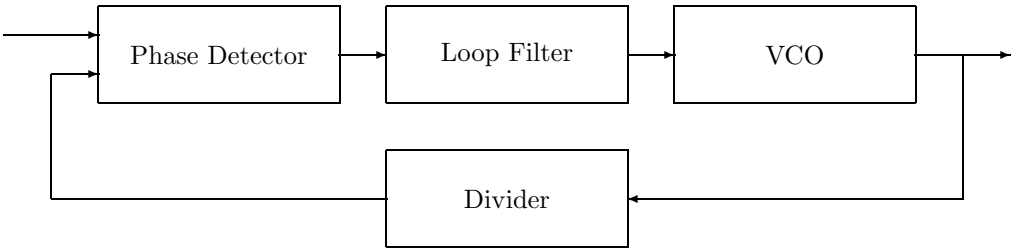

Figure 1: DPLL Block Diagram

2.2.1 Voltage Controlled Oscillator

Generates a digital clock. The frequency of the clock generated is controlled by one or more voltage inputs.

2.2.2 Divider

The divider performs frequency division on the output signal to generate a signal which has the frequency of the input but the phase of the output. This component is not present on DPLLs which are designed to have an input frequency equal to the output frequency.

2.2.3 Phase Detector

The phase detector measures differences in phase between the input and the divided output signal. This measurement is used to correct the phase difference.

2.2.4 Loop Filter

Loop filters translate between the phase detector's measurement signal and the VCO's control voltage(s). If the output lags the input, speed up the VCO. If the input lags the output, slow the VCO down.

2.3 DPLLs Presented

This paper will present two DPLLs.

1. A DPLL operating around 30MHz which has a phase detector known as a phase frequency detector (PFD) which will be called "PFD DPLL"
2. A DPLL operating around 400MHz using a quadrature output VCO which will be called "Quad DPLL"

3 Circuit Design

3.1 Basic Logic Circuits

These basic logic circuits form the building blocks for the digital portions of the PLLs.

3.1.1 Inverter

Figure 2 shows a common CMOS inverter, to obtain approximately matched current handling in the two devices, PMOS well width is double NMOS well width. The NMOS device here is the minimum size device in this process and the inverter is therefore the smallest matched inverter possible. This 2:1 well width ratio is employed in all logic circuits.

3.1.2 2 Input NAND

Figure 3 shows a common 2 input CMOS *nand* gate. A 2:1 overall well width ratio (see *Inverter*) was employed.

3.1.3 3 Input NAND

Figure 4 shows a common 3 input CMOS *nand* gate. A 2:1 overall well width ratio (see *Inverter*) was employed.

3.1.4 8 Input NAND

Figure 5 shows a common 8 input CMOS *nand* gate. A 2:1 overall well width ratio (see *Inverter*) was employed.

3.1.5 XOR

Figure 6 shows a common 2 input CMOS *xor* gate. A 2:1 overall well width ratio (see *Inverter*) was employed.

3.1.6 XNOR

Figure 7 shows a common 2 input CMOS *xnor* gate. A 2:1 overall well width ratio (see *Inverter*) was employed.

3.1.7 D Latch

Figure 8 shows a D latch built from 2 and 3 input nands.

3.1.8 T Latch

Figure 9 shows a D latch built from 2 input nands an inverter and a D latch.

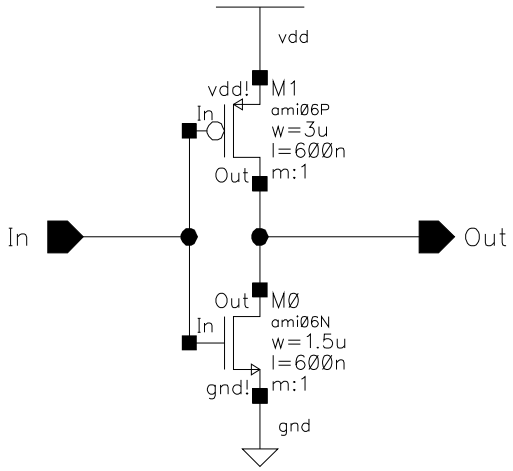

Figure 2: Minimum sized CMOS inverter

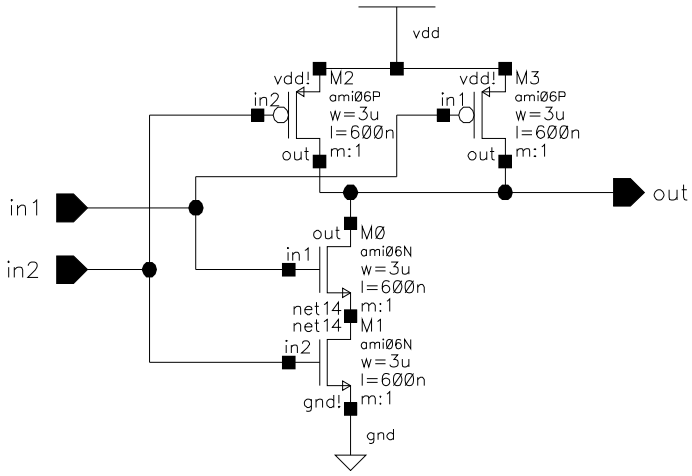

Figure 3: 2 input CMOS nand

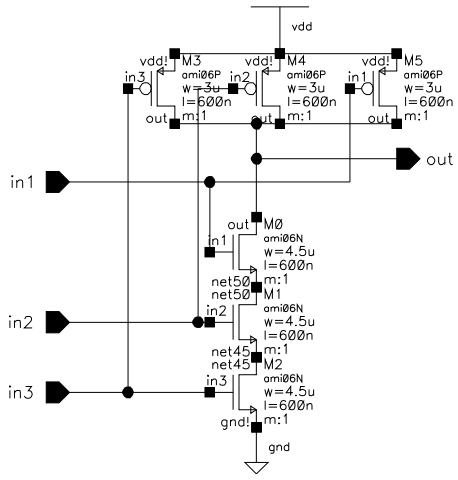

Figure 4: 3 input CMOS nand

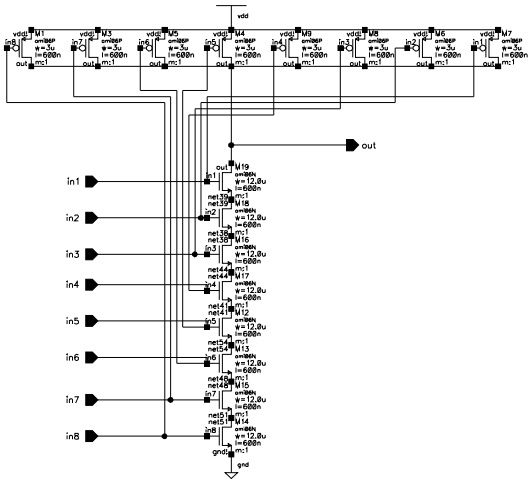

Figure 5: 8 input CMOS nand

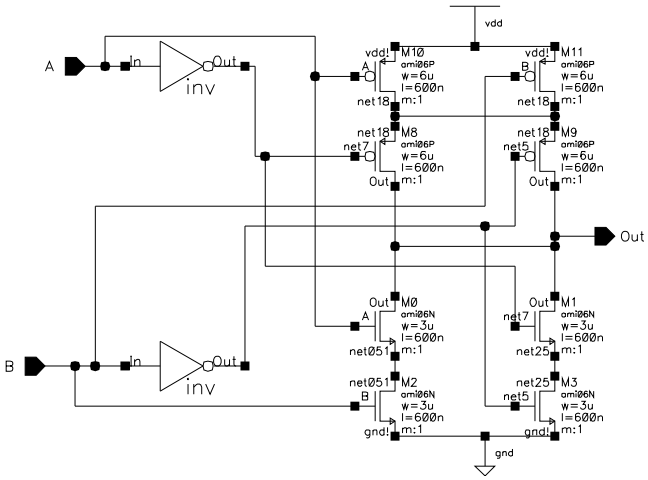

Figure 6: CMOS xor

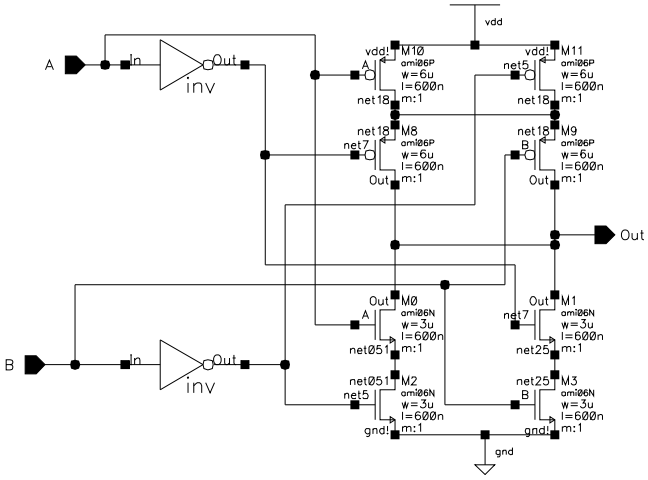

Figure 7: CMOS xnor

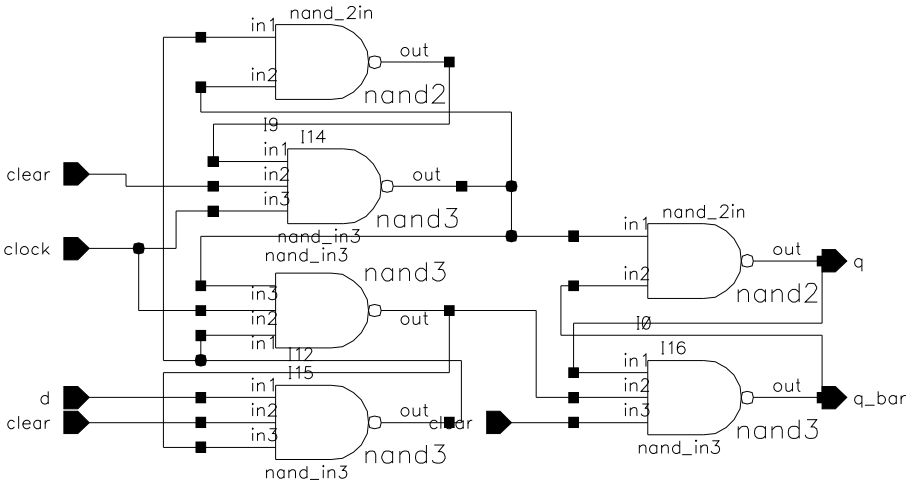

Figure 8: D Latch

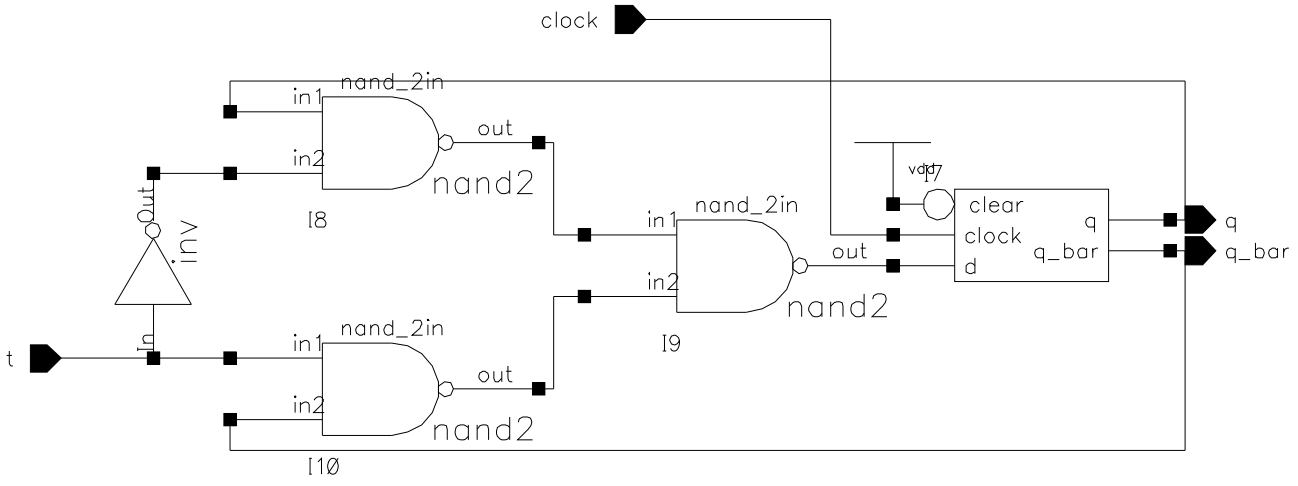

Figure 9: T Latch

3.2 Phase Frequency Detector Digital Phase-Lock Loop (PFD DPLL)

As the name suggests this DPLL has a phase frequency detector to compare the phases of divided clock signal and input signal.As shown in the schematic of the PFD DPLL in Figure 10 and mentioned in the earlier section, this DPLL has four parts and they are as follows.

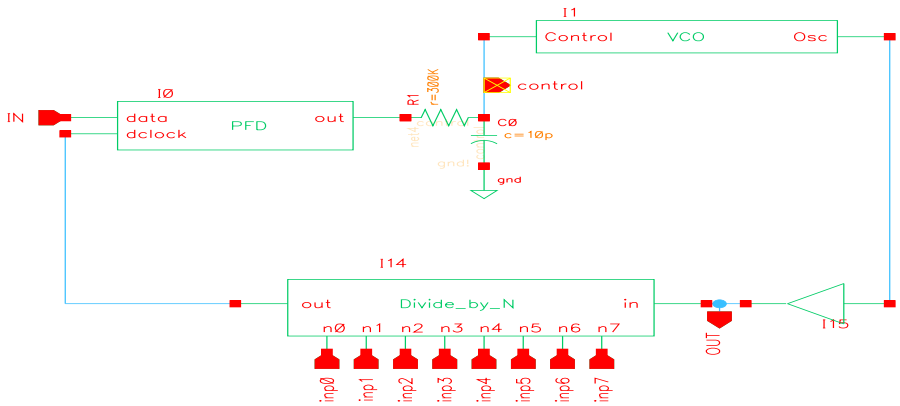

Figure 10: PFD DPLL

3.3 Phase Frequency Detector

The Phase Frequency Detector (PFD) is made out of two D-Latches, a nand gate, and a tristate gate that drives the voltage controlled oscillator (VCO). As shown in Figure 11, two data inputs of D-Latches are always connected high. The clock inputs are fed with data signal and dclock (divided clock) signal from frequency divider. The output from the D-Latch which is fed with data is called 'up' and the output of the other D-Latch, which is fed with d-clock, is called 'down'. The PFD always checks the rising edge of the signals. When the data is leading the dclock signal 'up' goes high till PFD sees the rising edge of the dclock. Similarly, when the dclock is leading the data 'down' goes high utill the rising edge of the data is seen. The inverted 'up' and the 'down' are fed to the tristate gate pmos and nmos, respectively. When the data signal is leading, the capacitor in the loop filter is charged by vdd because the PMOS of the tristate gate is on and the NMOS is off. The increase in control voltage will increase the frequency of voltage controlled oscillator. When dclock signal is leading, the NMOS of the tristate gate is on and pulls down the voltage of capacitor in loop filter. The decrease in control voltage will decrease the frequency of the voltage controlled oscillator. The details of each parts in the PFD are given below.

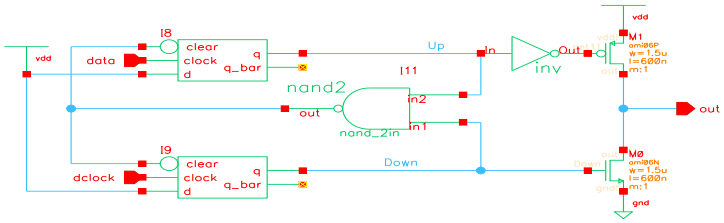

Figure 11: Phase Frequency Detector

3.3.1 D-latch

There are two D-latches used in PFD. Like any other regular D-latches they have a clock input, a data input, an inverted clear input and two opposite outputs, q and q bar. Each D-latch is made out of 4 three input nand gates and 2 two input nand gate. These nand gates are sized to give same delay as basic inverter. An NMOS of a basic inverter has a channel length (l) of 600 nm and a channel width of w_n 1.5 um, so PMOS of the basic inverter has channel width of w_p 4.5 um. The details on D-latch can be seen in Figure(XXX)in Appendix(XXX).

3.3.2 Two-input nand gate

The two-input nand gate takes two inputs from the two q outputs of D-latches and feeds back to inverted clear input of D-latches. The nand gates are sized up to give same delay as a basic inverter. The schematic of Two-input nand gate can be seen in Figure (XXX).

3.3.3 Tristate gate

The tristate gate we have designed in our schematic has a minimum-sized PMOS and a minimum-sized NMOS. The NMOS takes input from the output 'down' of the D-latch, whose input clock signal is dclock. The PMOS takes input from the inverted output 'up' of the other D-latch, whose input clock signal is data signal. The schematic of the Tristate gate can be seen in Figure 11

3.4 Loop Filter

The filter used here is a simple low pass filter. It is comprised of a capacitor and a resistor. The resistor value is 300 k ohm and capacitor is 10 pico farad. The control voltage for the VCO is taken parallel to the capacitor. The values of the component here are taken iteratively. Basically these values allows control voltage to be stable so that small changes or interferences do not effect the locked stage.

$$V_{inVCO} = \frac{1}{1 + jwRC}$$

The schematic of the loop filter is shown in Figure 12.

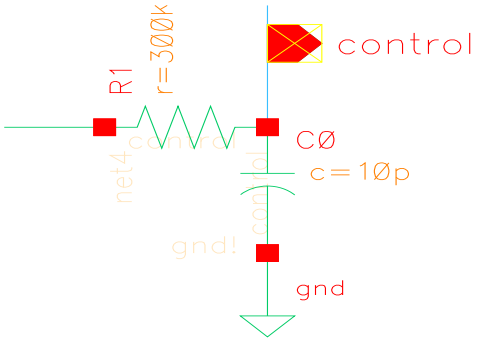

Figure 12: Loop Filter

3.5 Voltage Controlled Oscillator (VCO)

The current starved VCO is the VCO used in PFD DPLL. It has two parts- a current mirror circuit and current-starved inverter configurations. The schematic of current-starved inverter is shown in Figure 13. The current mirror circuit takes the control voltage and mirrors the current in the current-starved inverter ring oscillator. This can be seen in the Figure 14. The oscillator is very similar to a ring oscillator but the current flowing through the inverters are controlled by a PMOS and NMOS- current sources.The oscillator part of the VCO is ring oscillator which is made out of five inverters. Both the PMOS and NMOS in the inverter has channel lengh of 4.5 um. This is done to slow down the oscillator so that we can achieve the desired center frequency of 30 MHz. The channel width of NMOS is 1.5 um and to match the current the PMOS has a 3 um channel width. The PMOS and NMOS in the current source at the vdd end and gnd end that control the current through inverter, are sized to that of basic inverter. The current mirror circuit has the minimum sized PMOS and NMOS. The current in the MOSes of the mirror circuit is replicated in each current-starved inverter configuration.

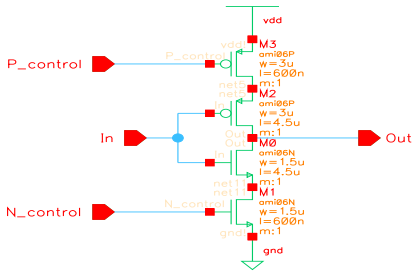

Figure 13: Current-starved inverter

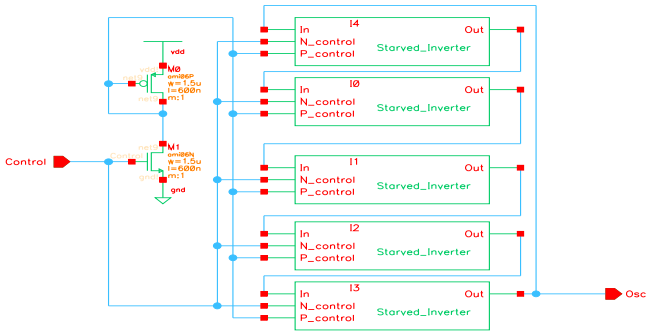

Figure 14: Current-starved VCO

3.6 Frequency Divider

Frequency Divider divides the output frequency before feeding it to PFD. It takes input from VCO and divides the frequency, which is the dclock signal. The Frequency Divider designed for the PFD DPLL is programmable. It takes 8 bit input to divide the frequency so the frequency can be divided by 1 to 255 times. The Frequency Divider has three basic parts - a 8-bit synchronous counter,an array of 2input XNOR gates to take input bits and a 8 input Nand gate. The schematic of the Frequency Divider is shown in the Figure 15.

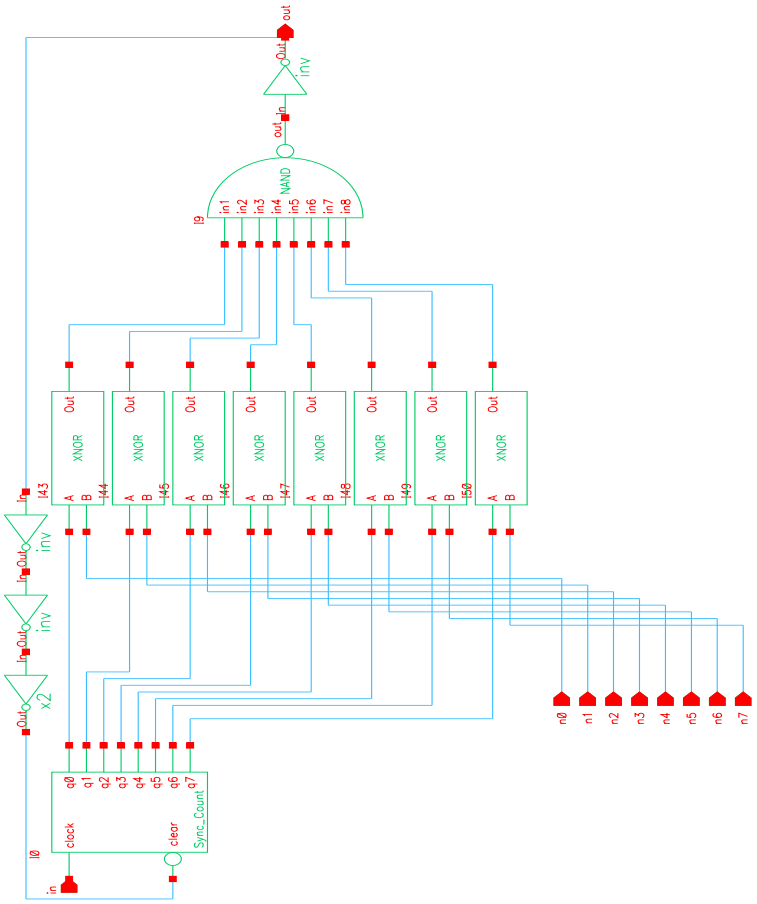

Figure 15: Frequency Divider

3.6.1 8-bit counter

The counter designed for the Frequency Divider is made from combination of D-latches, XOR gates and AND gates. The D-latch is the same D-latch that we used in PFD. The schematic of D-latch can be seen in Figure(XXX)in Appendix (XXX). XOR gate designed is sized to match the basic inverter. The PMOSes have channel width of 6 um, NMOSes have channel width of 3 um. The inverters used in XOR gate are matched minimum sized inverters.The AND gate is basically a nand gate with inverter and are sized to match the basic inverter. The schematic in the Frequency Divider is shown in the Figure 16.

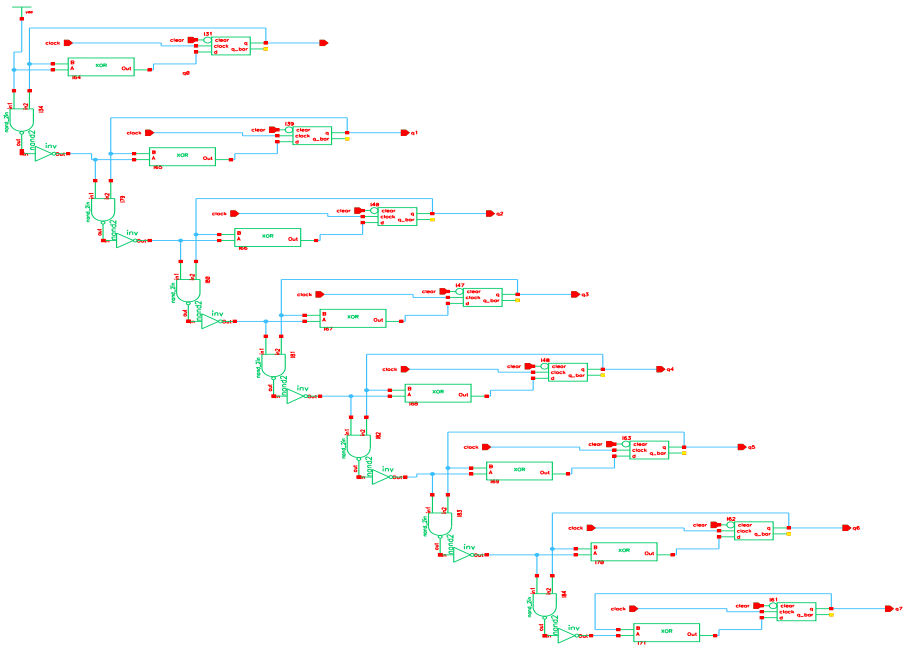

Figure 16: 8-bit synchronous counter

3.6.2 XNOR gate

The array of 8 2-input XNOR gates are used to make the counter programmable. The each output bit from the counter is fed to 2-input XNOR gate with the input bit we want to program. The schematic in the Figure (XXX) in Appendix (XXX) describes it better.

3.6.3 8-input NAND gate

The 8-input NAND gate takes input from the array of 8 2-input XNOR gates, which are used for programing. This NAND gate gives logic low when counter matches with the programmed bit and resets the counter after few delays provided by 4 inverters so that it stays high for time enough to reset the counter.

The schematic of Frequency Divider can be seen in the Figure(XXX) in Appendix (XXX).

3.7 Digital Output Buffer

The VCO itself is not capable of driving a big load capacitor.The digital buffer is designed to drive the output up to 40 pF load. The digital buffer for PFD DPLL has 6 inverter stages.The size of the inverter increases by the factor of 4. The largest inverter is 3.072mm wide and the smallest inverter is the minimum sized inverter. The schematic of the buffer is in the Figure 17.

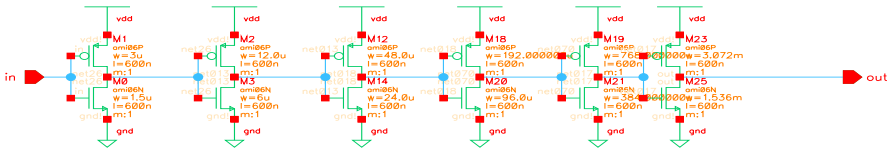

Figure 17: Digital Buffer

3.8 Quad DPLL

This DPLL is a 400MHz loop with a fixed frequency divider of 64. It uses an XOR phase detector and can only lock on to signals operating very near its center frequency. A simple low pass RC loop filter is used.

3.8.1 Quadrature Output Differential VCO

This VCO is an implementation of previous work on differential oscillators[1]. This is a four stage oscillator in which each node between stages has two signals which are 180 degrees out of phase. Each stage consists of two differential inverters, one which drives the output nodes and a second which is forward fed from other stages. The second forward fed inverter can pull the output node low, but do not drive it high. In addition, the stages are timed such that each pair of out of phase signals is 45 degrees different in phase than the next most similar signal. In this way, all eight possible 45 degree different signals (0,45,90,135,180,225,270,315) are present at any given time in the oscillator loop. These signals are used to drive the forward fed differential inverters.

This oscillator can operate at unusually high speeds because the feed forward paths allow nodes to begin switching before the signal from the main loop reaches the node. Also, because it is a differential mode logic it does not switch over the full range of supply voltage, meaning there is less charge to move each switch. A schematic is provided in Figure 18 and Figure 19, however more descriptive graphics are available[1].

3.8.2 High Speed Frequency Divider

At frequencies under 300MHz, T latches are used for simple frequency division by 2, however the propagation delay of these cells is too high for the 400MHz signal produced in this DPLL. To divide the high speed clock an inverter based divider was constructed[2]. This divider shown in Figure 20 uses a pair of cross coupled inverter as a memory cell to hold the previous state. When a high voltage period of clock arrives it closes the switch provided by the two inline transistors. This allows the next state to propagate into the inverter memory cell.

The string of inverters after the memory cell must be sized to prevent the next state from propogating around the loop before the transistors turn off. At the same time the inverter stages must be fast enough to propagate the next state before the next clock. For this reason, a divider of this style must be designed for the frequency at which it will operate.

3.8.3 XOR Phase Detector

The most basic phase detection device, the XOR phase detector is used here for speed. When the two input clocks are 90 degrees out of phase, the signals are different from each other as much time as they are the same and the XOR output is a 50% duty cycle signal. This 50% duty cycle output is considered the locked case. When the DPLL generated clock is too slow or lagging the input, the XOR output has a duty cycle proportionally greater than 50%. In the other case, the generated clock is too fast or leading the input and the output duty cycle is less than 50%.

3.8.4 RC Loop Filter

Figure 21 shows the well known RC low pass filter. Large values have been chosen for resistance and capacitance to make this an averaging filter that is insensitive to minor input errors. The effect of this filter is to average the XOR output. This output is used to control the VCO. When the XOR output is 50%, the average voltage is 2.5v. In this case the DPLL is considered locked on the input and the VCO is oscillating at its center frequency. If the XOR output is not locked, the filter output voltage is:

$$V_{FilterOut} = XOR_{DutyCycle} * (VDD - VSS) \tag{1}$$

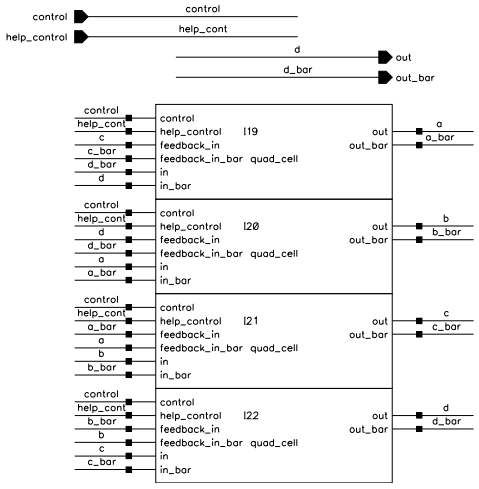

Figure 18: Quadrature Output VCO

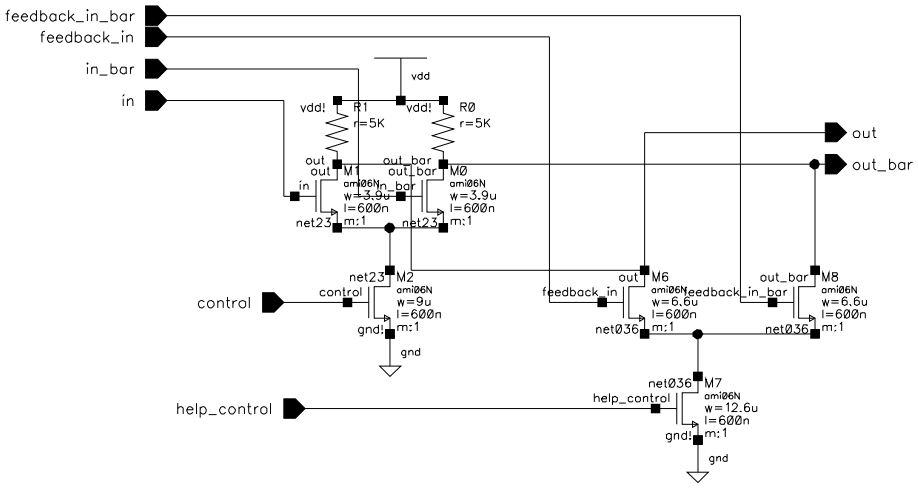

Figure 19: Quadrature Output VCO Cell

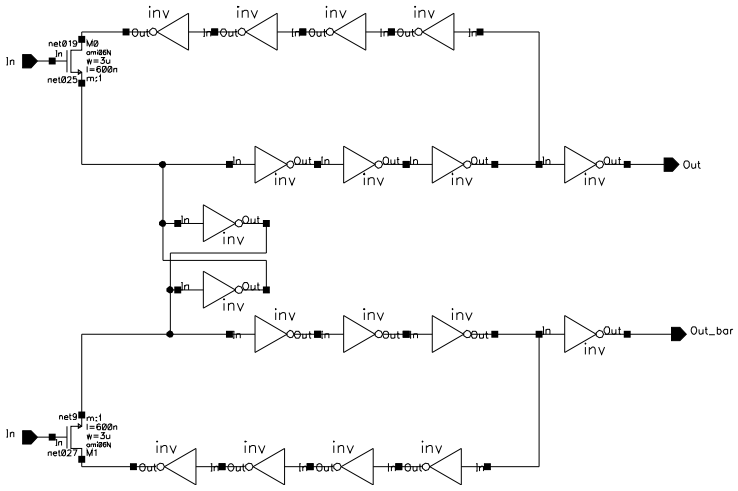

Figure 20: 400 MHz Frequency Divider

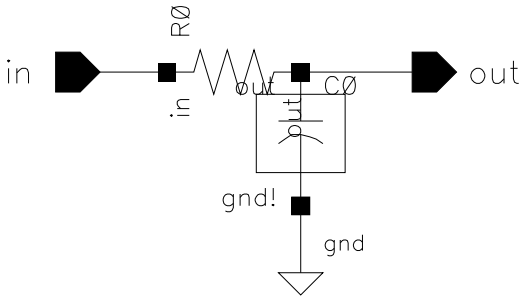

Figure 21: RC Low Pass Filter

This produces a control voltage which keeps the VCO in phase with the input. For example, if the VCO signal lags the input this causes a rise in the control voltage to increase the VCO's speed.

3.8.5 Digital Output Buffer

Because the oscillator output has niether the current driveing capability nor the voltage swing to drive an output pin and the frequency divider, a digital buffer is connected to the output of the oscillator. This buffer, whose schematic is Figure 22, is a 12 stage buffer of inverters which increase in size by a factor of 2 each stage. The first stage is a minimum sized inverter *(see Basic Logic Circuits)* while the biggest transistor in the last stage is 6.144mm wide. This slow rate of stage to stage size growth and large final transistor size allows this stage to drive outputs at the frequencies required.

3.9 Test Oscillator

To aid in verification of this design a second version of the differential oscillator is was constructed. This oscillator runs alone and it's control voltage is accessable by a pin. It's output is driven by the same output buffer used in the PFD DPLL, and will be available for measurement only via a probe pad. The schematic of this oscillator is the same as Figure 18. Its transistors have been resized from above and it oscillates around 1GHz. The faster VCO cell is shown in Figure 23. This output frequency is then divided by a high speed divider similar to that used in the Quad DPLL. Because it must respond faster, it has less inverters in the feedback loop. Figure 24 is the overall schematic of this test circuit.

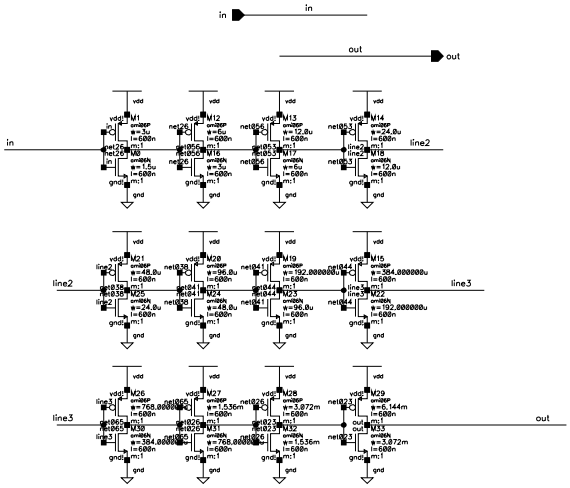

Figure 22: Digital Buffer

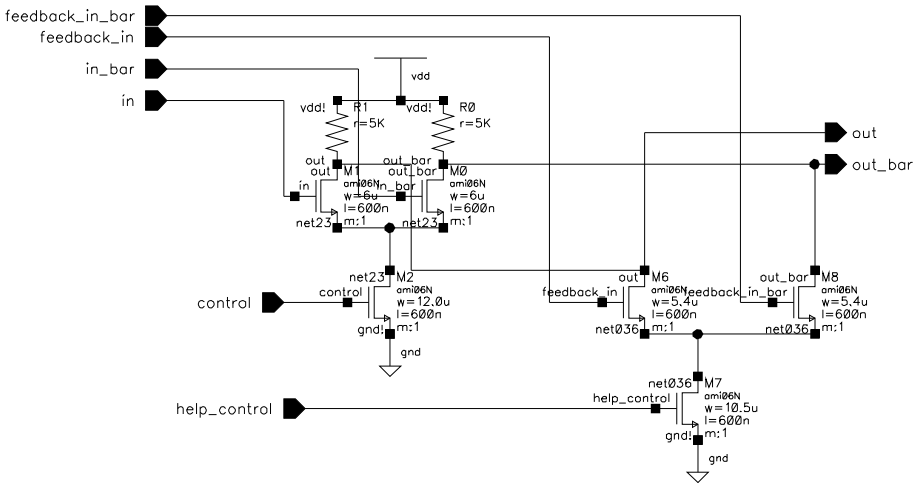

Figure 23: 1GHz VCO Cell

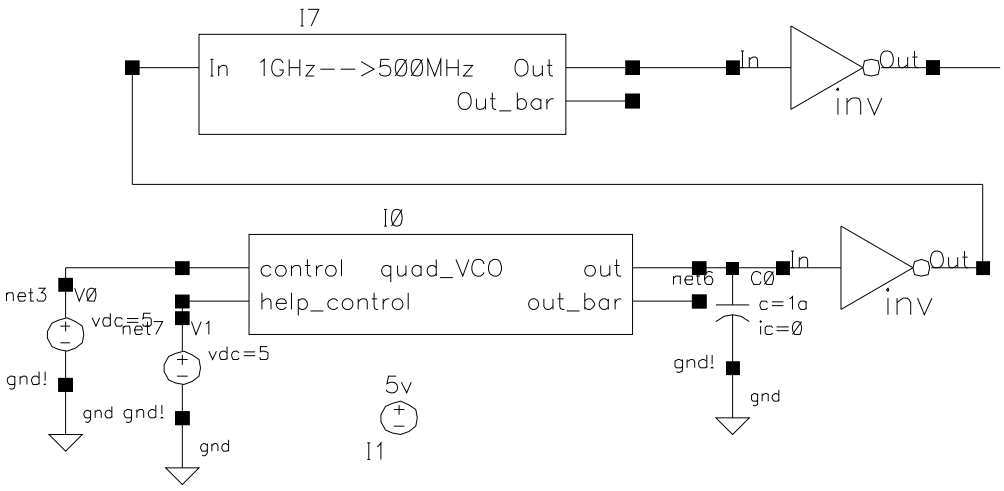

Figure 24: 1GHz Test Oscillator Schematic

4 Simulation Results

Schematic simulations were performed on all circuits to verify functionality. Simulations with parasitic capacitors extracted from the layout were performed on circuits whose performance was expected to be highly layout dependant. As a final verification, extracted simulations were performed on top level layout. This section presents the simulation results.

4.1 Circuit Simulations

4.2 Simulation Results

The simulated outputs of three different parts of PFD DPLL and output of PFD DPLL are shown in this section.

4.2.1 Phase Frequency Detector

The simulated output of the Phase Frequency Detector (PFD)*(see the Figure 11)* is shown in the figure 25. The simulation shows the output of tri-state goes high if the data signal leads the d-clock signal, this duration is equal to the phase difference of the data signal and d-clock signal.

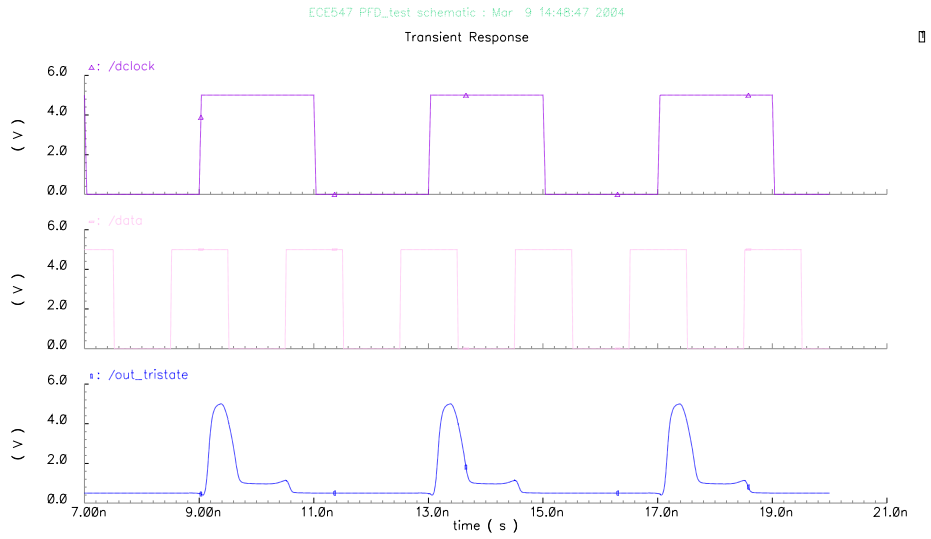

Figure 25: Output of PFD

4.2.2 Voltage Control Oscillator

The simulation of current-starved Voltage Controlled Oscillator (VCO) at two different control voltages are done. Figure 26 shows the output of the VCO at control voltage of 5 volts. The oscillation frequency at this control voltage is about 34 MHz.

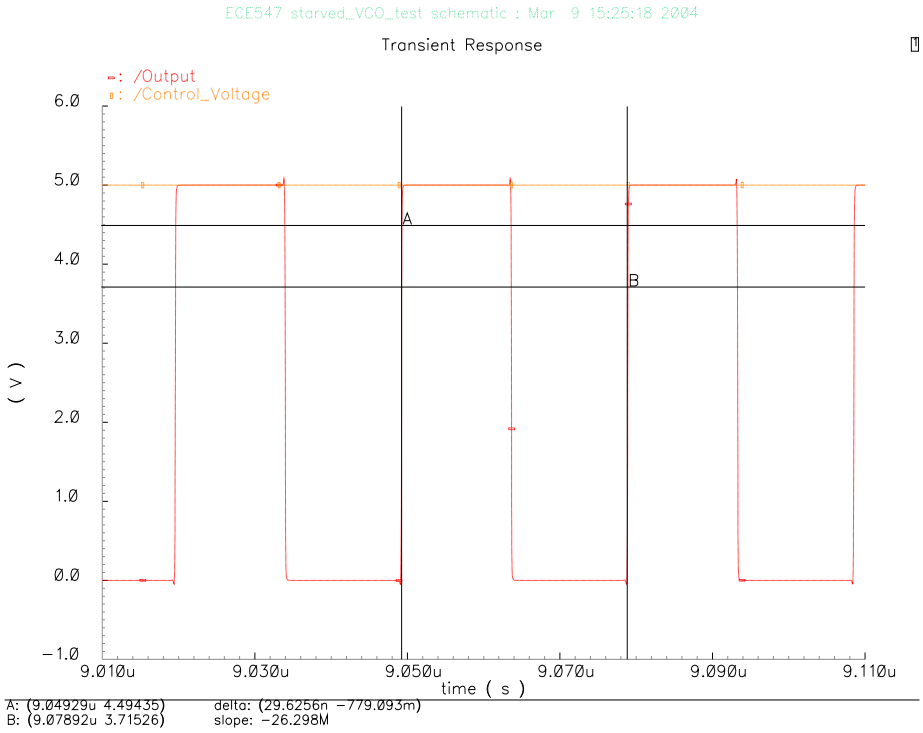

Figure 26: Output of VCO at Control Voltage of 5V

The frequency of the VCO does not fall much when the control voltage is 2.5 V howerever, frequency starts falling pretty quickly at lower control voltages. Figure 27 shows the output of the VCO at control voltage of 2.5 volts.The oscillation frequency at this voltage is about 32 MHz.

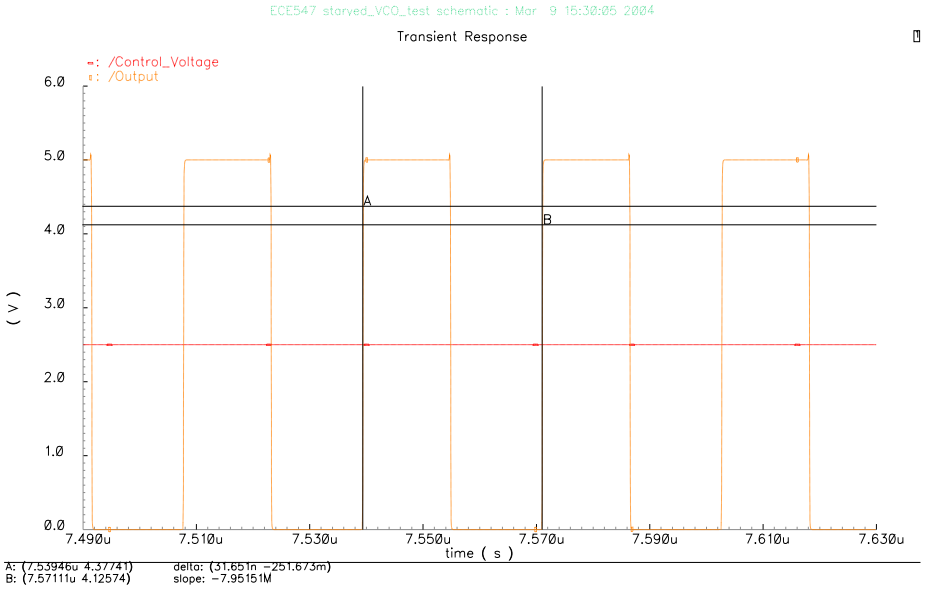

Figure 27: Output of VCO at Control Voltage of 2.5V

4.2.3 Frequency Divider

The programmable Frequency Divider is programmed at two different divider values, or frequency is divided by two values. In the figure 28 it is cleary shown that frequency is divided by 3 and in the figure 29 frequency is divided by 5.The duty cycle of the divided signal is not 50 percent as four inverters *(see the Figure 15)*in the frequency divider does not provide enough delay before it resets the counter.

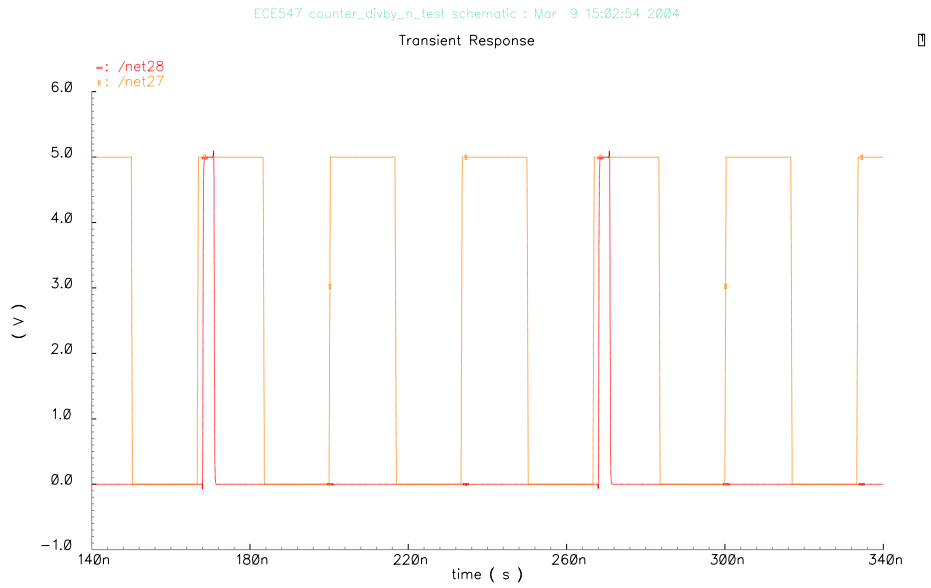

Figure 28: Output of Frequency Divider Divided by 3

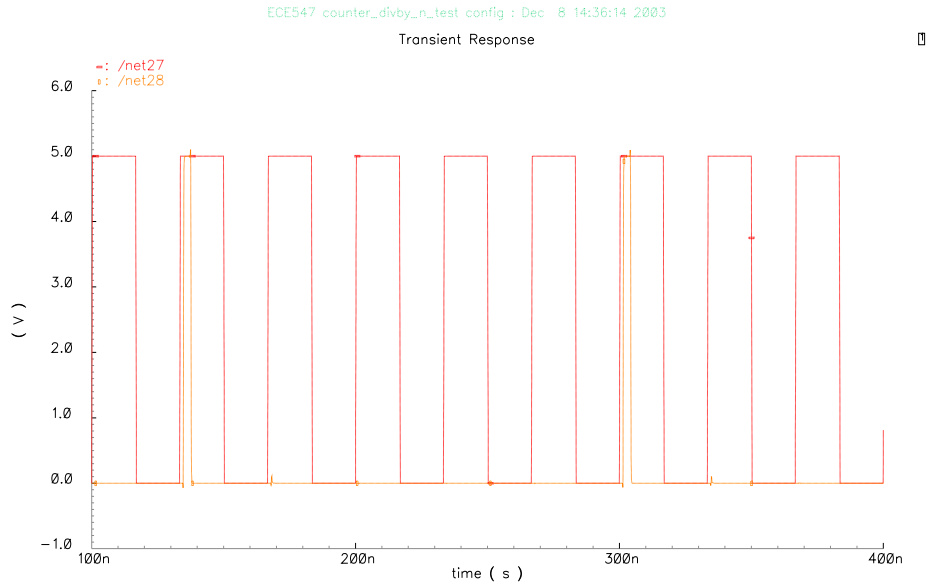

Figure 29: Output of Frequency Divider Divided by 5

4.2.4 PFD DPLL

In the figure 30 the output simulation of top level PFD DPLL is shown, the frequency divider was programmed with divider as 2. The output frequency of the DPLL is twice that of data signal. XXXXXXXXXXXXX In the figure XXXXXX the control voltage of the VCO is shown which kind of lock down at XXXXXXXXXx.Add figure over here.

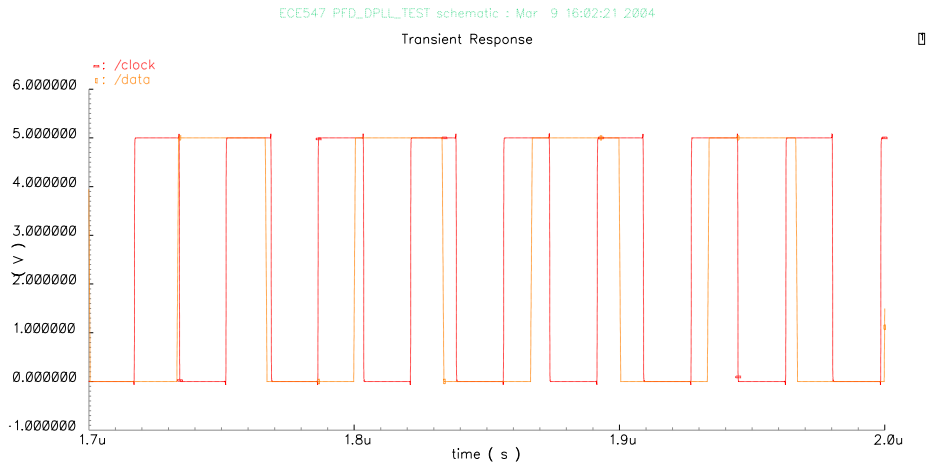

Figure 30: Output of PFD DPLL with Frequency Divider Divided by 2

4.3 400MHz DPLL

4.3.1 T Latch Frequency Divider

Frequencies below 500MHz are divided by the T latch. Figure 31 shows the output of a t latch with its input tied high and its clock line driven at 500MHz by a test source.

4.3.2 Programmable Frequency Divider

With an input of ten 100MHz pulses, the counter was set at several different divide values. Figure 32 shows counter output at different division values. These outputs are do not have 50

4.3.3 300MHz Digital Buffer

Large currents are required to drive the capacitive load of the package pins at the 300MHz output by the faster PLL. To verify the output buffer for this device can drive loads of that magnitude, simulation was performed with that buffer driving 40pF at full operating frequency. The results of this simulation, shown in Figure 33 verify this capability of the buffer.

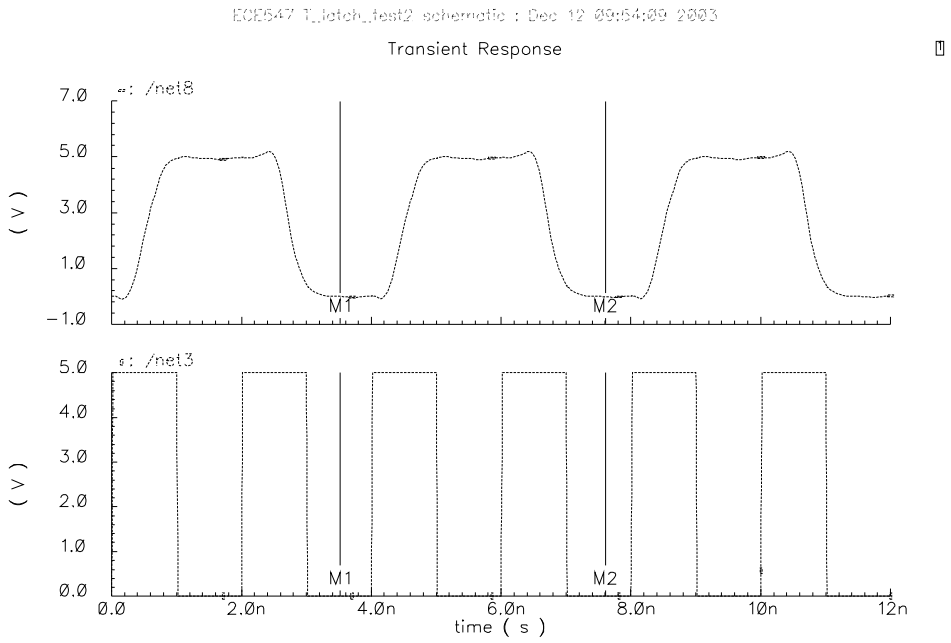

Figure 31: T Latch 500MHz Simulation

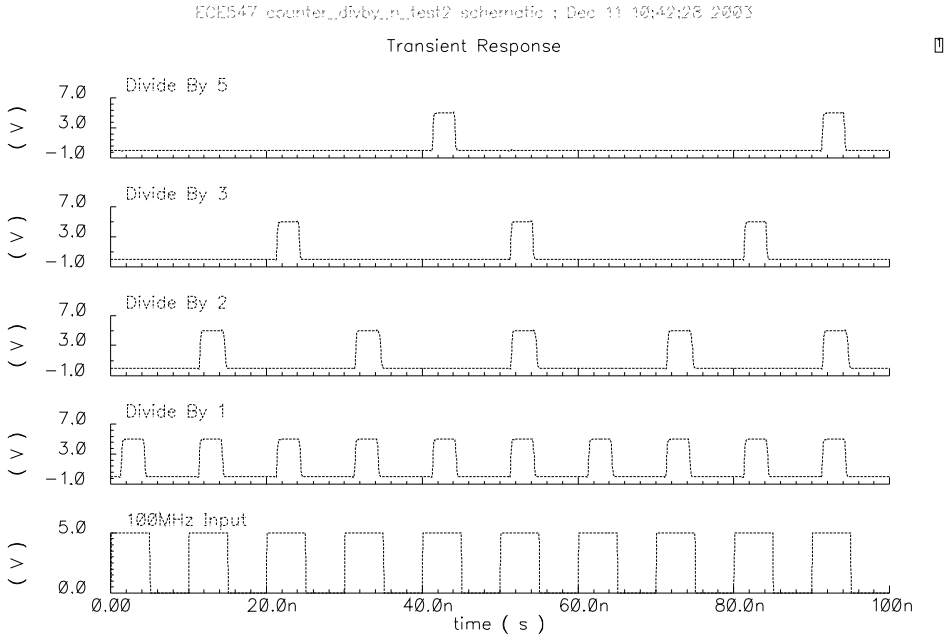

Figure 32: Programmable Counter Divide Simulation

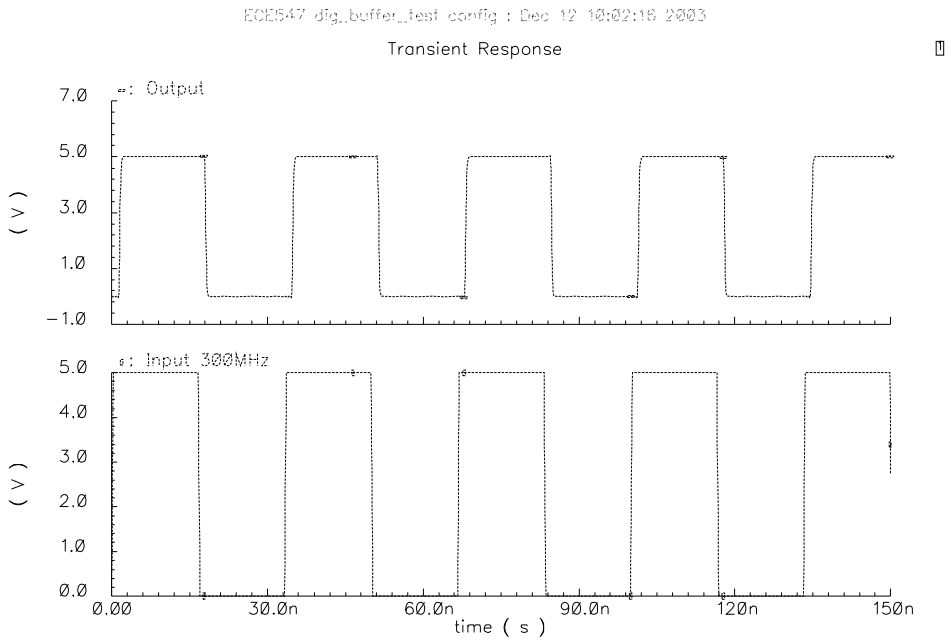

Figure 33: 300MHz Buffer Driving 40pF Load

4.3.4 High Speed Quadrature VCO

This high speed VCO has outputs shown in the simulation Figure 34 which range in frequency from 521MHz with the control voltage at 5 volts to 268MHz when the control voltage is at 2 volts.

4.3.5 High Speed Frequency Divider

In Figure 35 A 500MHz test signal is driving the dynamic frequency divider which is tuned to divide the VCO's output. The input and output signals are shown together and clearly show proper division.

4.3.6 Maximum Oscillation Frequencies

Figure 36 is a simulation of the maximum speed the three oscillators on chip can operate. To perform this simulation, the initial condition on the three VCO control lines was set at 5 volts. The faster DPLL has a maximum output frequency of 525MHz, the slower DPLL has a maximum output frequency of 28MHz and the test VCO runs up to 529MHz.

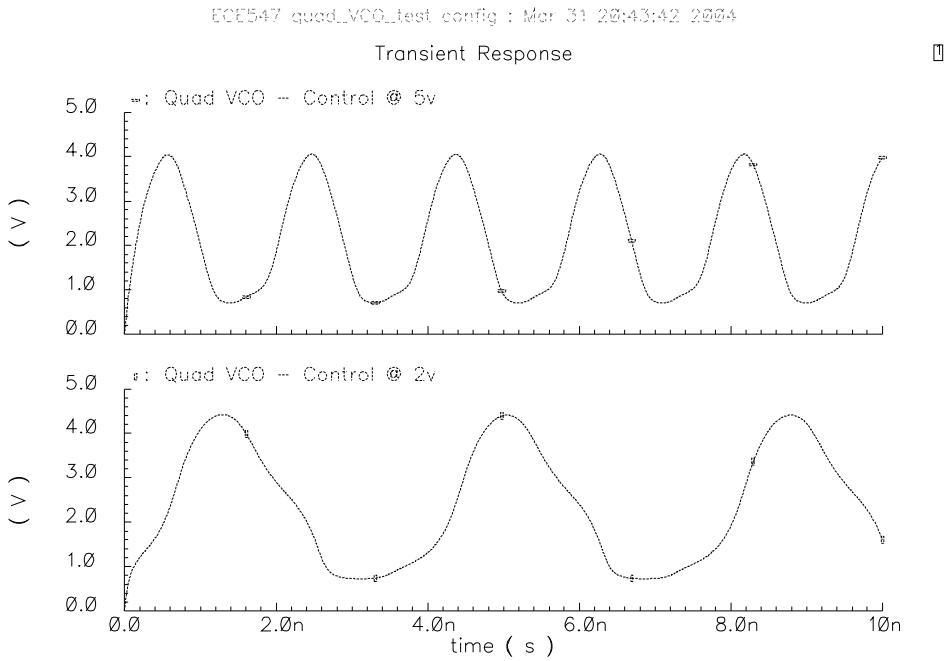

Figure 34: Quad VCO Oscillations at Control Voltage Extremes

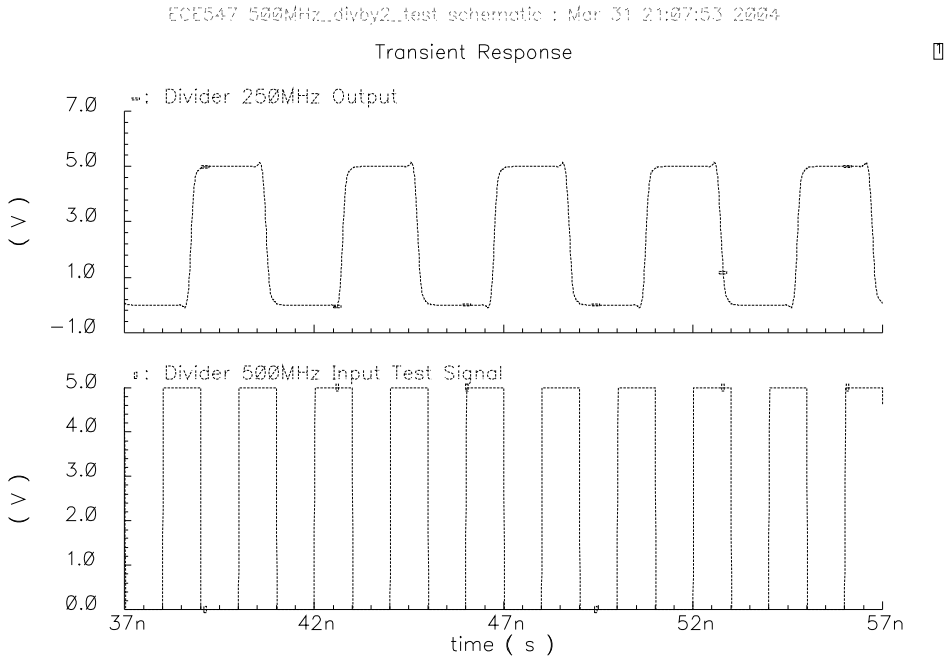

Figure 35: 500MHz Frequency Divder

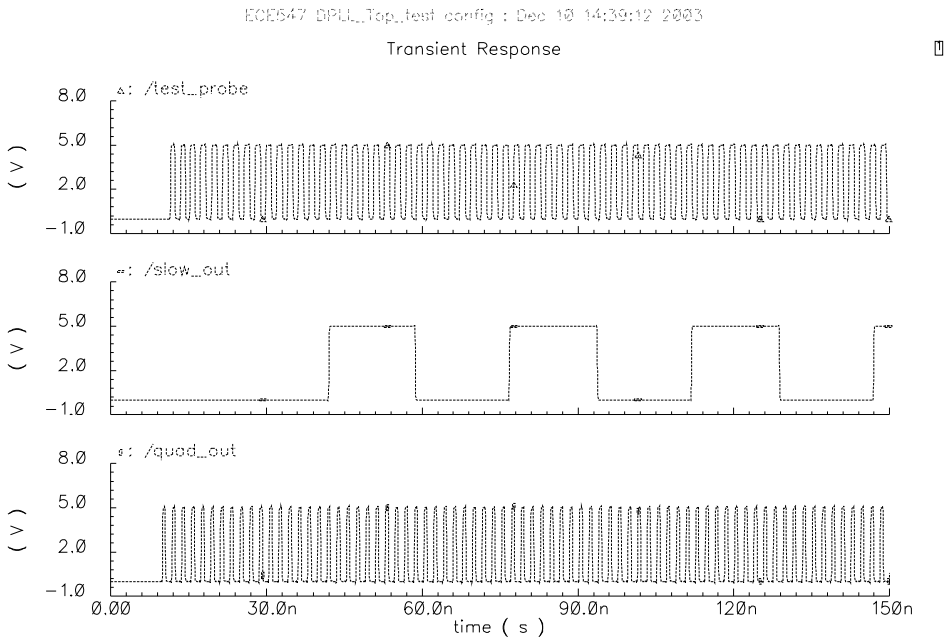

Figure 36: Maximum Frequency Simulation

5 Testing and Verification

5.1 High Speed Quadrature Output Oscillators

Figure 37 is the measured output of the test oscillator with the control voltage set at 3v. Under this condition, the ouput oscillates at 361MHz. This is 15difference was expected. This oscillator does not perform well at other control voltages. High control voltages lead to distorted output, while lower voltages stop oscillation entirely.

Due to the poor performance of this type of oscillator, the high speed PLL testing is limited. While the output of the high speed PLL does oscillate at frequencies in the expected range, it does so only intermittantly when a real input is applied. Since the output of the test oscillator verifies the functionality of the high speed frequency divider, the VCO in the high speed PLL is likely the issue.

5.2 30MHz DPLL

This circuit performs as simulated with the exception of the frequency divider. Some frequency divider settings did not perform predictably. Figure 38 shows a waveform as measured from the output of this PLL. This output was quite noisy, so a filtered version of the waveform is also plotted. An interesting result seen most easily in the filtered plot is a varying oscillation amplitude. Since the design of this oscillator is a loop of inverters, it is not clear why the amplitude varies significantly. The overall output amplitude is greater than expected and parasitic reactive elements in the packaging are the believed cause. To test the frequency aquisition capabilities the output frequency of the PLL was monitored while the input frequency was varied. For this test, the frequency divider was set to divide by 2. Figure 39 shows filtered transforms of the PLL outputs. As the expected output frequency lowers, the oscillator reaches it's lowest oscillation frequency, and the oscillations become less stable. The less stable signal has poor accuracy compared to the higher frequency signals. In this figure, a direct relationship between frequency and stability of oscillation is shown by the width of the response generated at different frequencies.

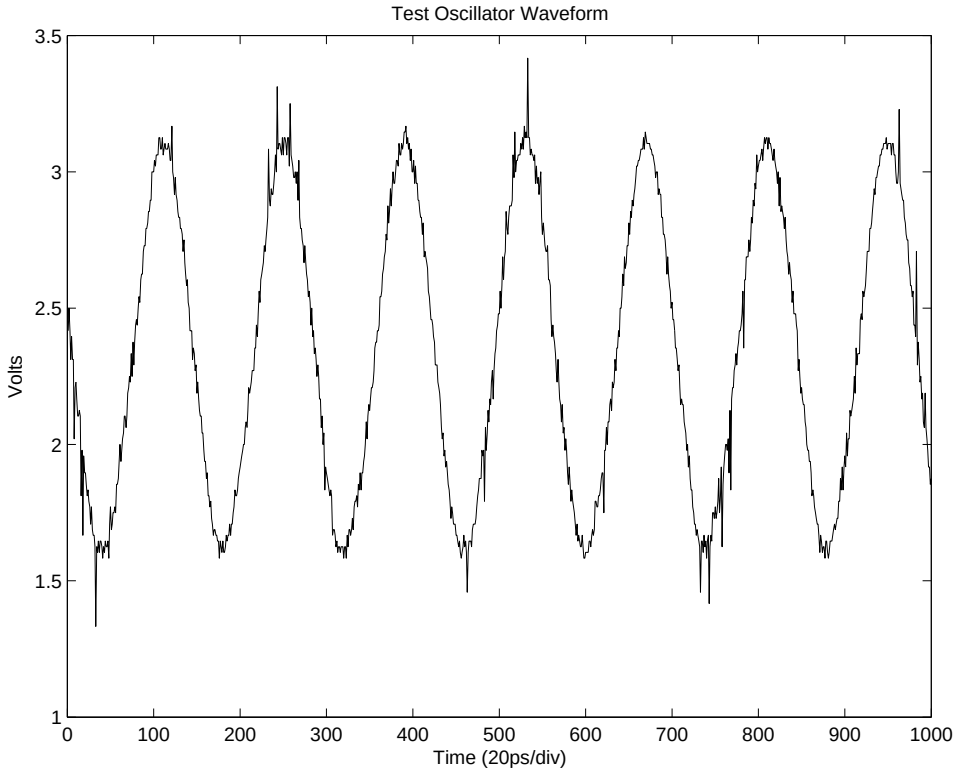

Figure 37: Test VCO Output when Control is 3v

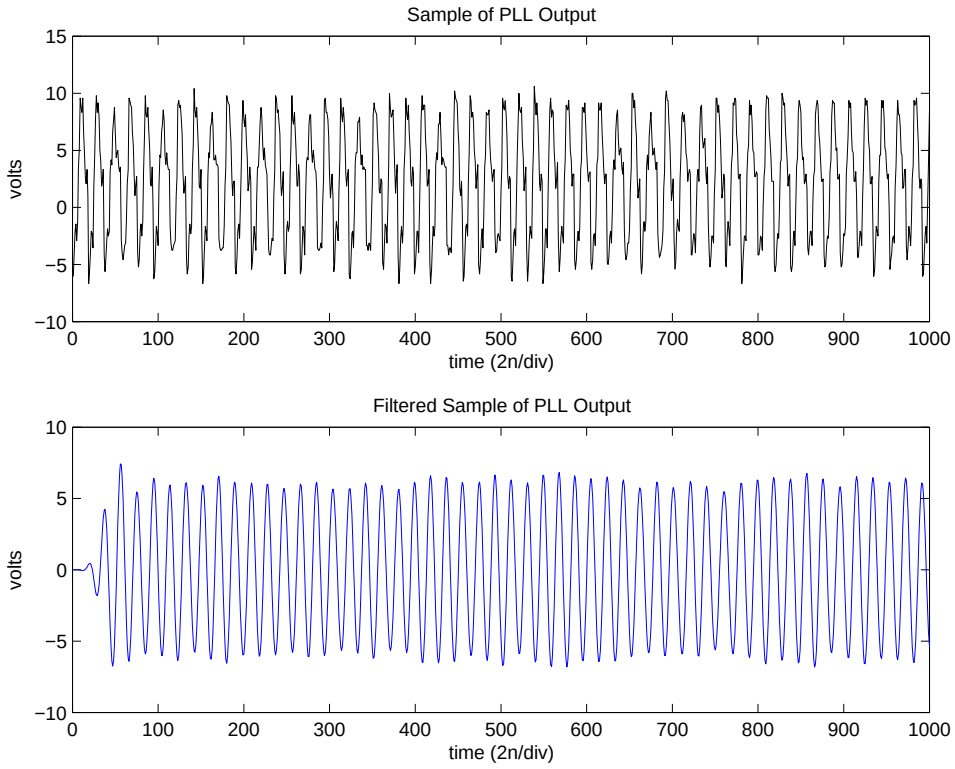

Figure 38: Output Waveform from 30MHz DPLL

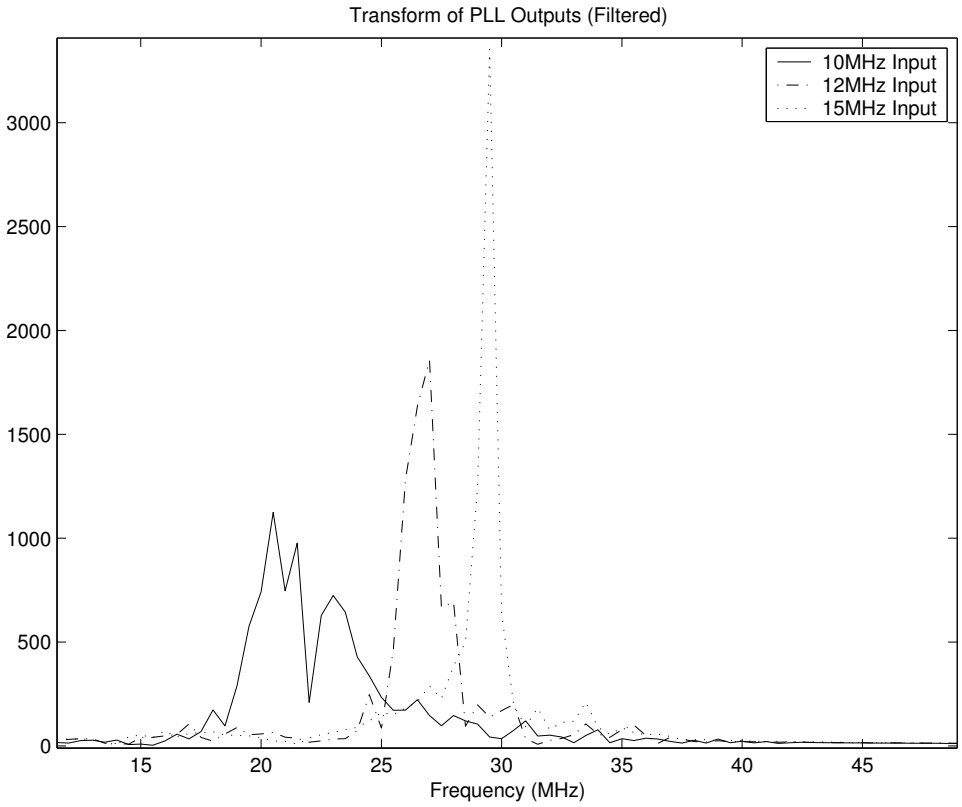

Figure 39: Frequency Response of PLL to Inputs

6 Layout Design

1056 Transistors, 80k ccs, 73.4k vias, and 27k via2s are laid out on a 1.5um x 1.5um die. Digital buffers are placed in the outer regions to minimize the distance power must travel to them from the padset and signal must travel from them to the pads. Lower power digital circuitry is placed closer to the center of the design. Guard rings of grounded metal1 to substrate contacts are used extensively to isolate logic componenets. Supply decoupling capacitors are built in any space not occupied by circuitry.

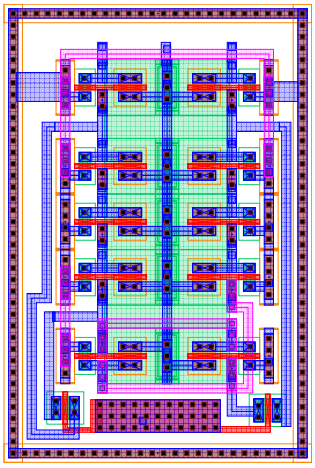

Figure 40: 1GHz Frequency Divide By 2

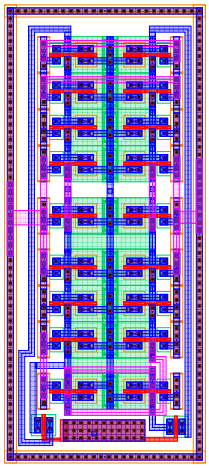

Figure 41: 500MHz Frequency Divide By 2

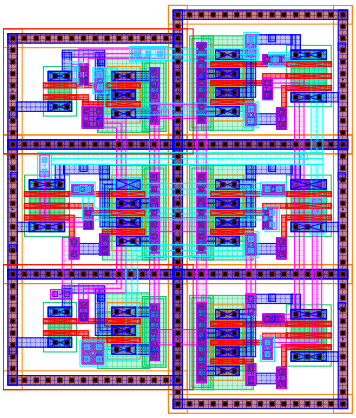

Figure 42: D Latch

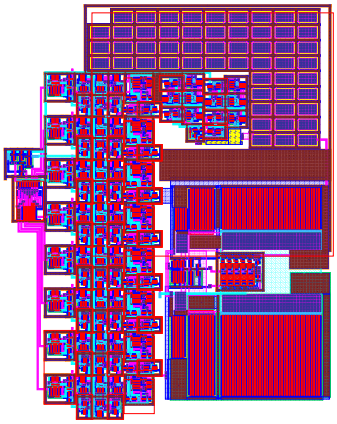

Figure 43: PFD DPLL

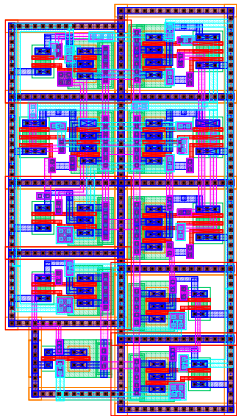

Figure 44: T Latch

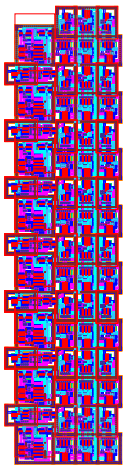

Figure 45: 8 Bit Counter

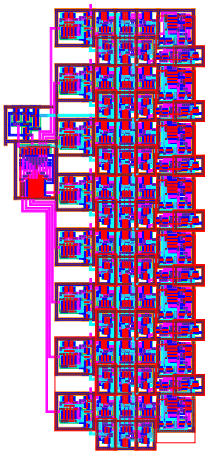

Figure 46: Divide By N Counter

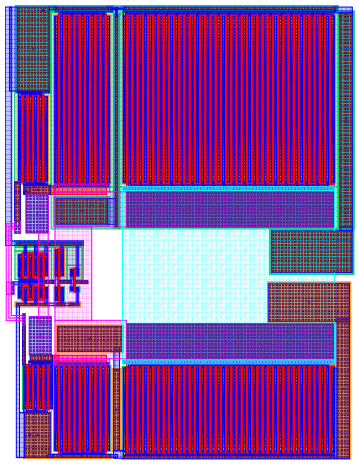

Figure 47: Digital Buffer

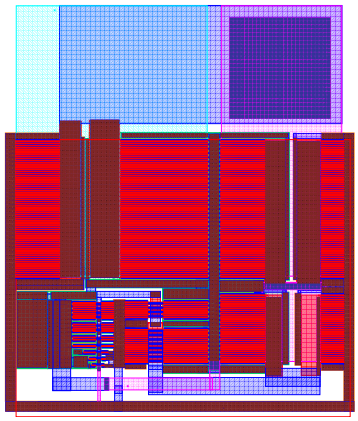

Figure 48: Fast Buffer

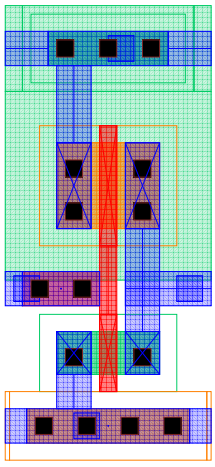

Figure 49: Basic Inverter

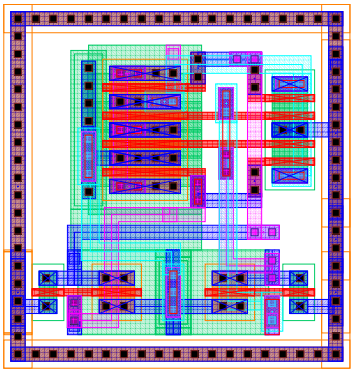

Figure 50: CMOS xnor

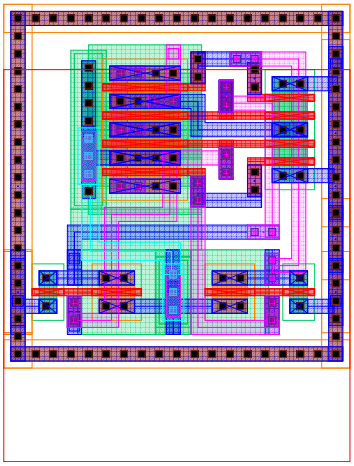

Figure 51: CMOS xor

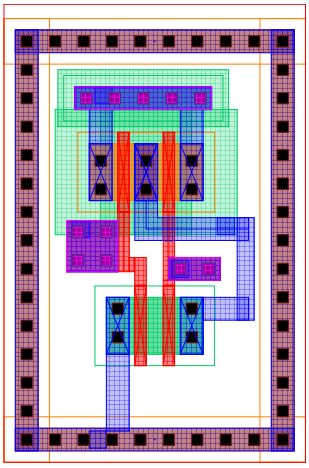

Figure 52: CMOS 2 Input nand

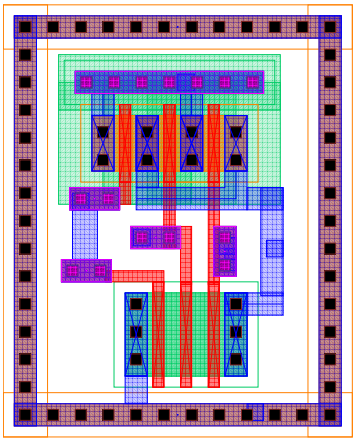

Figure 53: CMOS 3 Input nand

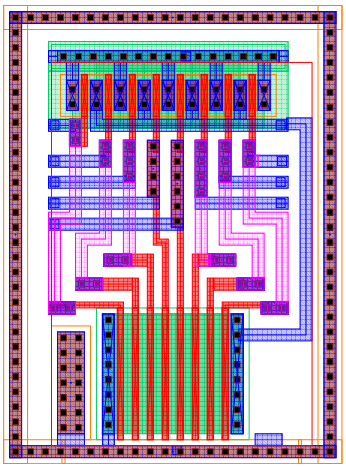

Figure 54: CMOS 8 Input nand

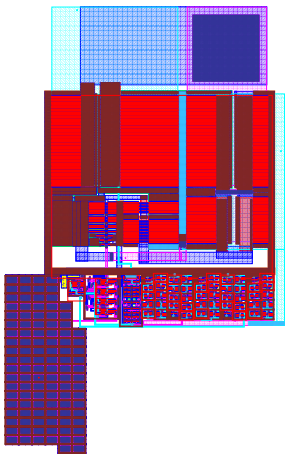

Figure 55: 400MHz DPLL

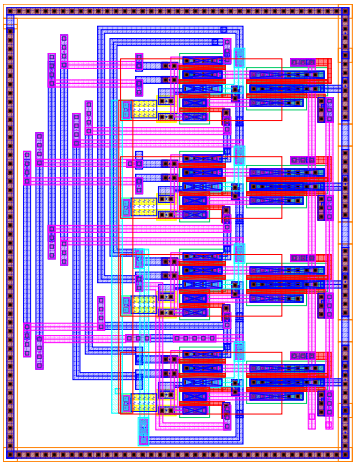

Figure 56: 400MHz VCO

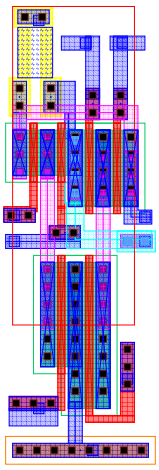

Figure 57: 400MHz VCO Cell

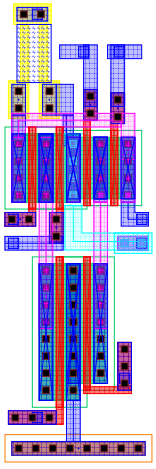

Figure 58: 1GHz VCO Cell

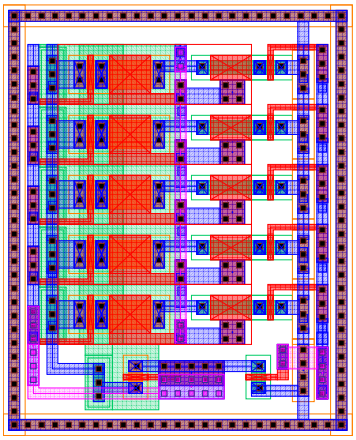

Figure 59: 30MHz VCO

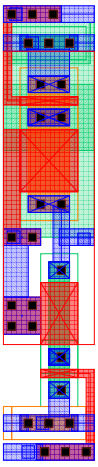

Figure 60: 30MHz VCO Cell

7 Conclusion

With a 1.5um x 1.5um die, two DPLLs were constructed. Simulations with extracted parasitic capacitances indicate these devices function properly. Testing of the fabricated devices revealed problems with designs operating near the limits of this technology, while the more conservative designs function as predicted. Improvements are needed, but there is potential for a viable design based on this work.

Future work on this project would likely focus on improved loop filters to optimize locking speed and characteristics.

8 Bibliography

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- R.E. Best. *Phase-Locked Loops, 3rd Ed.* McGraw Hill 1997
- S. Brown, Z Vranesic. *Fundamentals of Digital Logic with VHDL Design.* McGraw Hill 2000

9 Biography

9.1 Devon Fernandez

Devon was born in Bangor, Maine and grew up in Maine and in upstate New York. In May 2003 he conpleted a BS in Electrical Engineering and Computer Engineering at the University of Maine. During his college career he has worked in computer networking and as a teaching assistant for Electrical Networks I and II. Devon is a member of Eta Kappa Nu, Tau Beta Pi and the IEEE. He is currently persuing an MS in Electrical Engineering at the University of Maine.

9.2 Sanjeev Manadhar

Sanjeev Manandhar is a Undergraduate student in Computer Engineering. He was born in Kathmandu, Nepal. He attended high school from Nepal and is working towards a bachelor's degree in computer engineering at the University of Maine, Orono. He is member of IEEE chapter. He likes to play soccer, hiking and do sketches. He plans to go to graduate school and learn more about microelectric circuit designing.