1 KB SRAM

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Abstract

The design, simulation, and layout of an Asynchronous 1KB SRAM is presented. The SRAM is constructed from four 256 byte blocks and is built on a 180nm process and uses 3.3V devices. The SRAM is functional at 10 MHz with a 3.3 V supply.

1 Introduction

The Asynchronous Static Random-Access Memory (SRAM) designed in this report consists of five disctint components. The SRAM cell used is a standard 6 transistor CMOS implementation. The memory is organized into 4 blocks each with 256 bytes of storage. The memory is addressed with a row decoder for the first 8 bits of the address, which correspond to the word lines in each of the 4 blocks. The last two bits of the address are sent to a collumn mux to select from the 4 blocks. The output of the collumn mux is then sent to either a sense amplifier for the read operation or a write driver for the write operation. The memory is configured to read or write a word at a time. A block diagram of the SRAM is shown below in Figure 1.

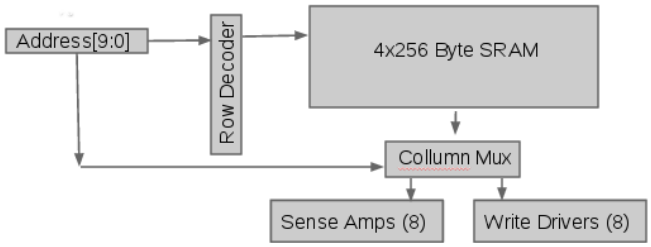

Figure 1: SRAM Block Diagram

The SRAM design and sizing was done in accordance with "Analysis And Design Of Digital Integrated Circuits", *Hodges, David A./ Jackson, Horace/ Saleh, Resve, 0-07-228365-3.*

2 Design and Schematics

The schematic design and layout of the SRAM subcomponents are described in this section. The section will flow from the most basic component, the 6T cell, to the complete SRAM block.

2.1 6T Cell

The schematic for the base 6T cell used in the SRAM is shown below in Figure 2.

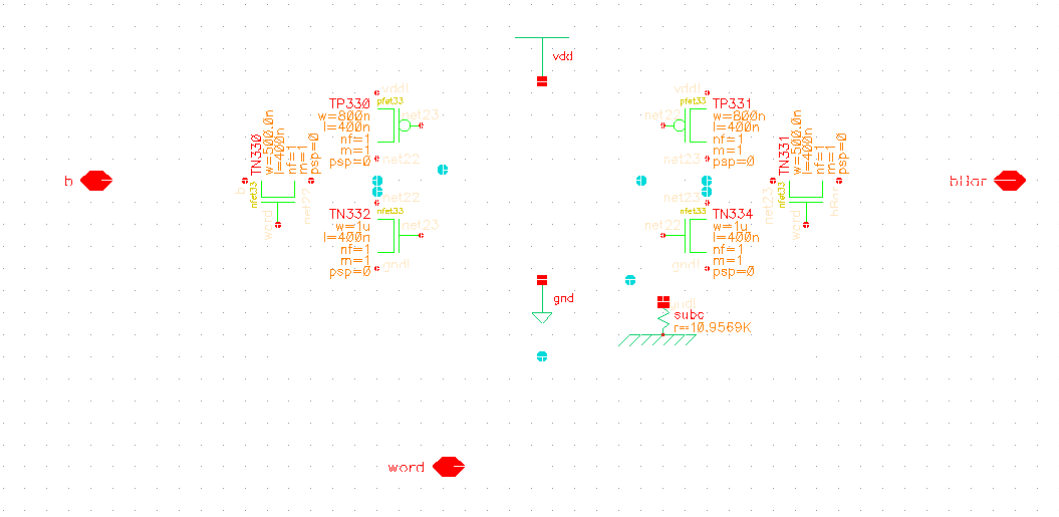

Figure 2: 6T Cell

This 6T cell is the building block used to created the 256 byte blocks shown in the next section.

2.2 256 Byte Block

The 256 byte block consists of 256 rows, each with 8 collumns of 1 bit SRAM cells. During the pre-charge stage, the bit lines are all driven high by the PC signal and the PFET gate between each bitline pair. A small subsection of the 256 byte cell is shown below in Figure 3.

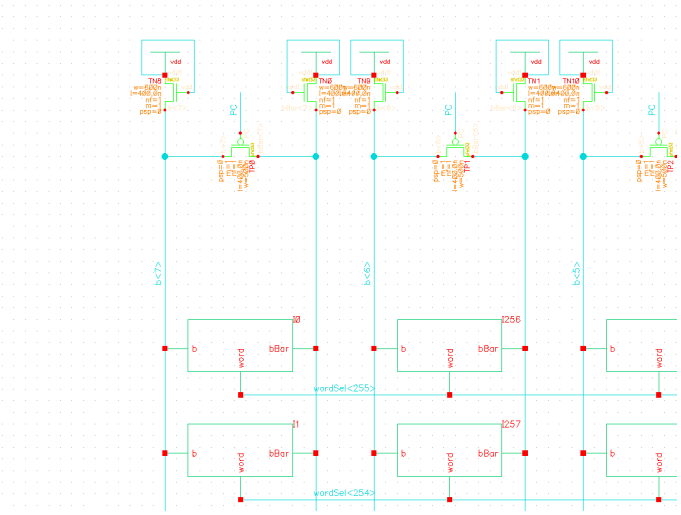

Figure 3: 256 Byte Block Top

2.3 Row Decoder

The row decoder uses a precoder to reduce the fanout and also to make the layout simpler. The precoders are 4 to 16, and the final stage is 32 to 256. A snapshot of the precoder is shown in Figure 4.

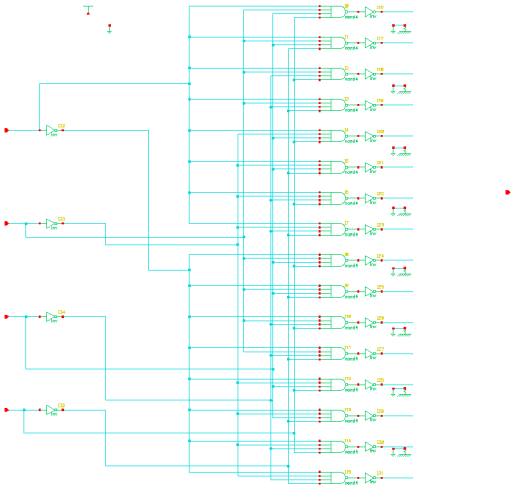

Figure 4: Precoder

Figure 5 shows the schematic view of the row decoder.

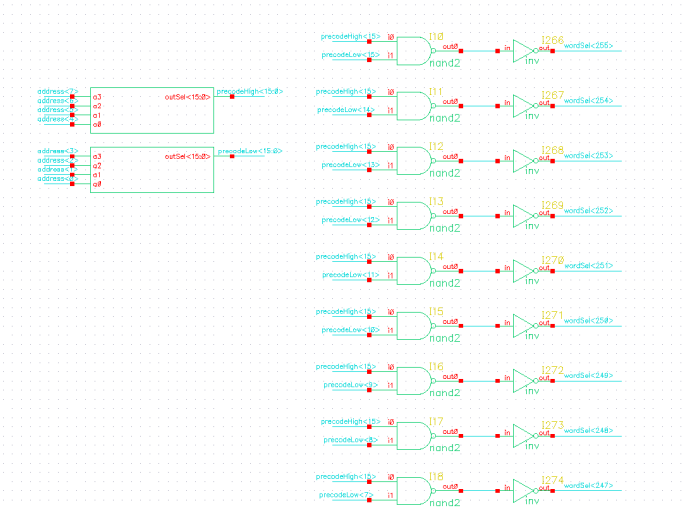

Figure 5: Row Decoder

2.4 Collumn Mux

The collumn mux selects which of the 4 blocks to connect to the write drivers and sense amplifiers based on the lowest two bits of the address. A PFET is used to connect to the sense amplifiers, as they must be driven high by the bitline to read. The write drivers are connected through an nfet gate so that the write driver can drive the bitlines low as required. The overall collumn mux is shown in Figure 6.

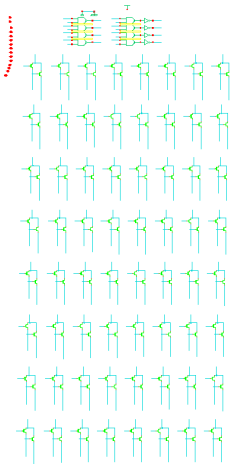

Figure 6: Collumn Mux

2.5 Write Driver and Sense Amplifier

The write driver is a large nfet driven by an and gate. During a write, the transistor pulls the corresponding bitline to zero. This will set the cell to the correct value. The sense amplifier is a differential pair with an output buffer to isolate it from the data line. The buffer is needed to ensure that the write operation is not affected by the unknown output state of the sense amplifier. The sense amplifier configuration is depicted in Figure 7.

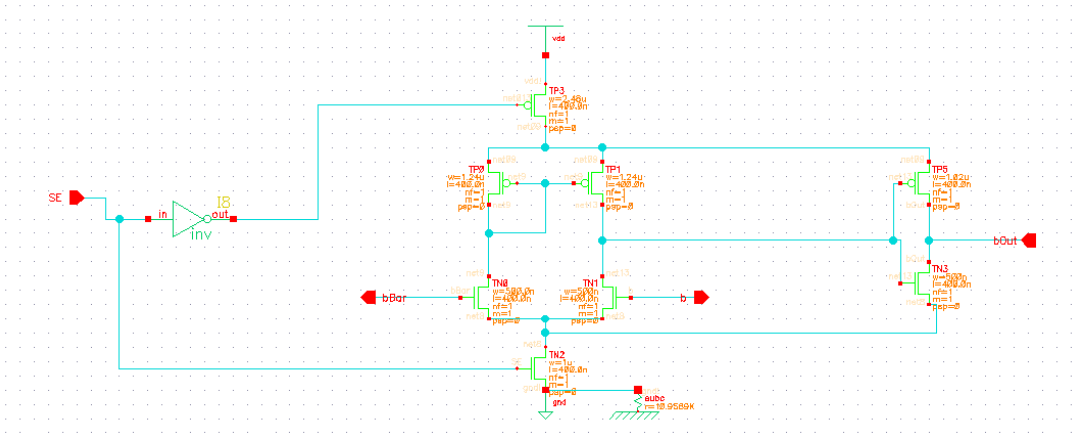

Figure 7: Sense Amplifier

2.6 Complete SRAM Circuit

Figure 8 shows the complete SRAM schematic.

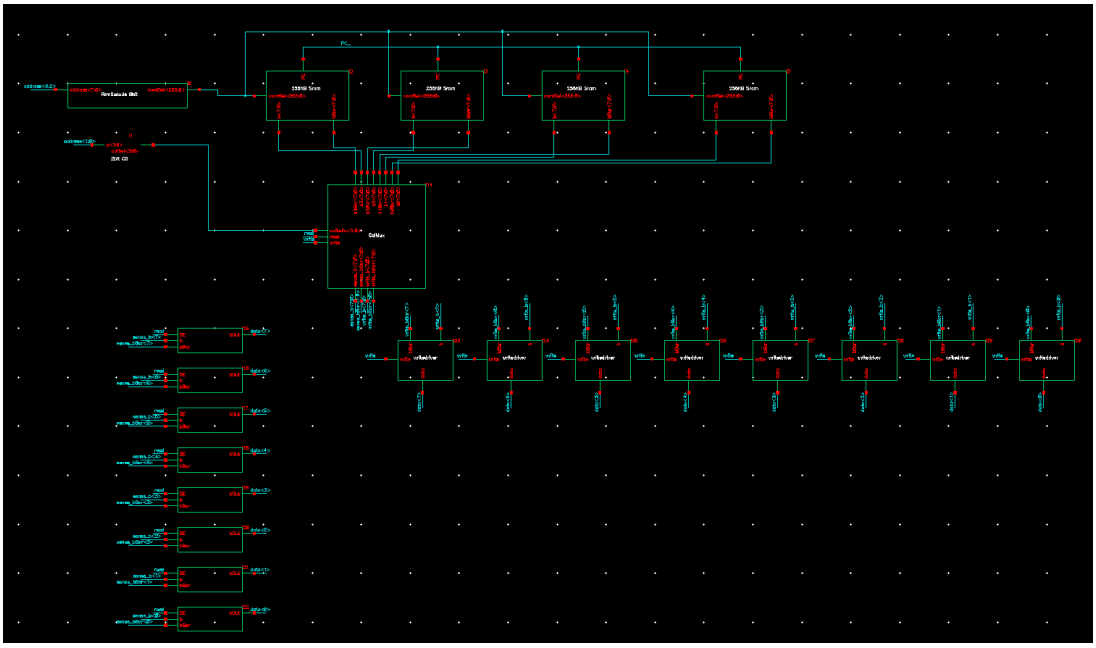

Figure 8: Complete SRAM Circuit

3 Layout and Simulation Results

The layout of the complete chip is shown below in Figure 9. In addition to the SRAM, ESD pads and a bandgap reference are included to complete the chip.

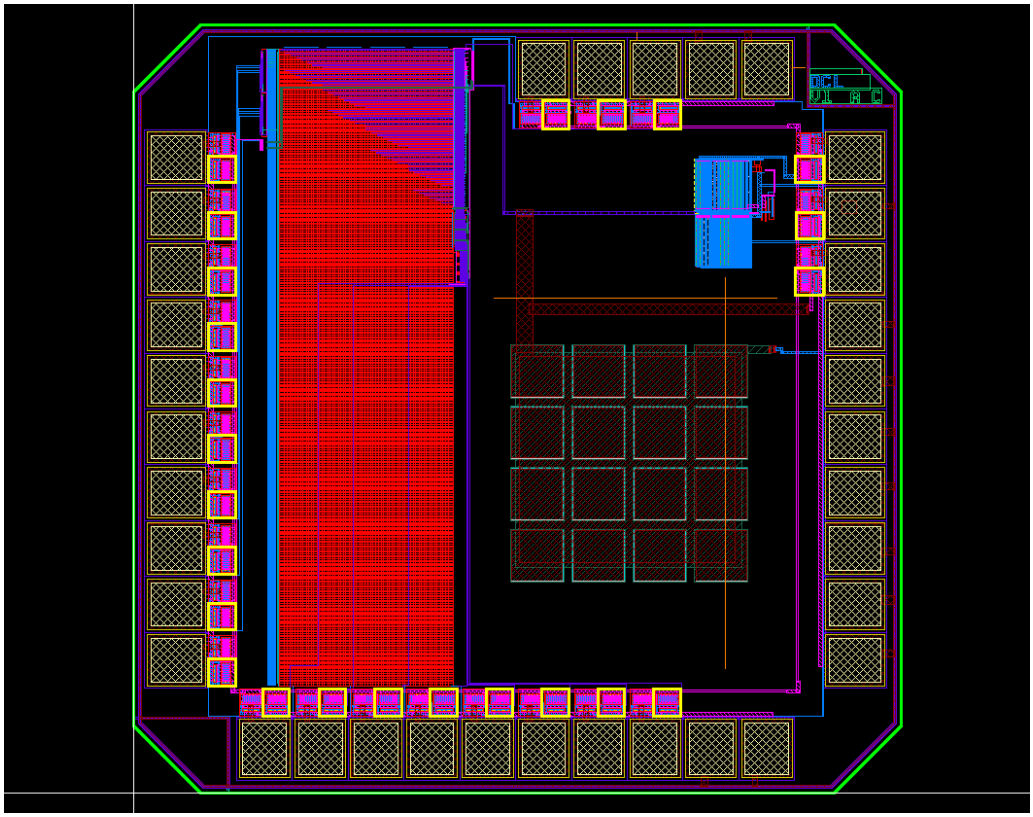

Figure 9: SRAM Layout

Simulation results indicated that a read can take up to 10ns. The write time is approximately 80ns. The reads are non-destructive and the cells operate as intended. The simulation results shown in Figure 10 show a write and then two successive reads on the address 0x3FC of the data 0x0A. Based on the delays and simulation, the SRAM can run at speeds up to 10 MHz.

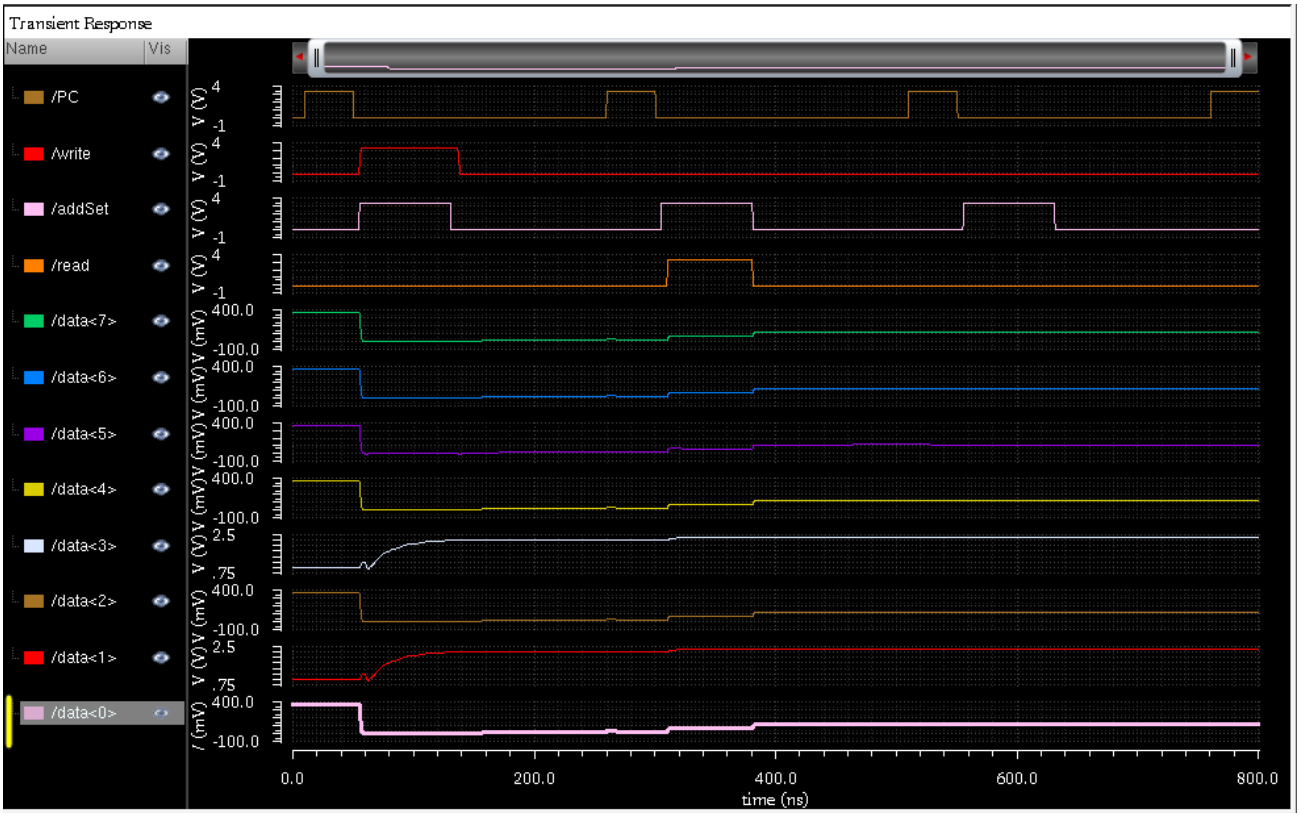

Figure 10: SRAM Layout