Switched Oscillator for LADAR Applications

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Abstract

This project presents the design and simulation of a switched oscillator intended to be the first part of the front end of a Light Detection and Ranging (LADAR) system. A chirped frequency modulated (FM) LADAR system works by driving a laser beam modulated by a chirped FM signal. The chirp is a sinusoidal waveform that begins at a start frequency (f_{start}) and ramps up to an end frequency (f_{stop}), forming sawtooth pattern with respect to the frequency of the sinusoid. By comparing the transmitted signal with the reflected signal, a distance to target may be determined. The goal of this particular integrated circuit (IC) is to form the FM chirp signal necessary to a LADAR system as a whole.

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1 Introduction

Laser Detection and Ranging (LADAR) systems operate on similar principles as their RADAR counterparts, but offer a number of distinct advantages. It is more useful in the detection of sea-skimming cruise missiles, where scattering from the sea surface and ducting in the marine boundary layer present problems for radar due to the small beamwidth of LADAR [1]. This also makes LADAR less detectable by enemy combatants [2]. LADAR also allows for the generation of 3D images that are valuable in target identification and clutter penetration via the use of focal plane resolution [3]. The applications of LADAR systems include collision avoidance systems on commercial vehicles, military target analysis, and even facial recognition and security.

The fundamental operation of LADAR systems consists of sending a laser beam to a target, receiving its reflection, and comparing the reflected signal to the sent signal. In the case of the FM chirp LADAR system, the laser beam is modulated in frequency, linearly increasing from a start frequency (f_{start}) to an end frequency (f_{stop}). The difference between the start and stop frequency is referred to as ΔF, while the difference in frequency and time between the send and receive signals are referred to as f_{if} and τ, respectively. Finally, the period of the chirp is known as T. Figure 1 below depicts the FM chirp setup with the send signal shown solid and the receive signal shown dashed.

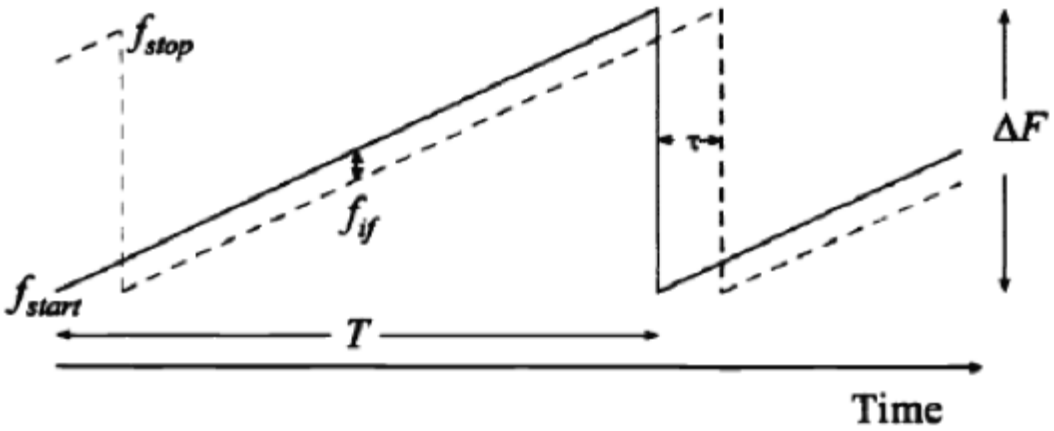

Figure 1: Conceptual Plot of FM Chirp Setup [3]

The reflected signal is mixed with the transmitted signal, which results in four distinct components. These components correspond to the transmitted signal, the reflected signal, the sum of the two signals, and the difference in the two signals.

In the frequency domain, the difference component appears as a series of peaks. These peaks occur at multiples of the chirp period, and the largest peak is then used to determine the range to the target. The following relationships express how to determine both the range resolution and the distance to target:

$$\Delta R = \frac{c}{2\Delta F} \quad \text{(Eq. 1)}$$

$$d = n\Delta R \quad \text{(Eq. 2)}$$

Where ΔR is the range resolution, c is the speed of light, and d is the distance to target. The range resolution defines the minimum distance interval at which targets can be distinguished. For example, a system with a range resolution of 1 meter would not be able to tell the difference between an object 1.7 meters away from an object 1.8 meters away. For this task, a range resolution of 0.1 meters would be required. Simple inspection of Equation 1 shows that the critical variable in determining range resolution is the frequency range of the chirp, ΔF. Equation 2 states that the distance to target is defined by the highest peak found in the frequency domain, that occurs at n peaks away spaced out by intervals of ΔR.

The mixing, amplification, and signal processing required to implement a complete LADAR system is beyond the scope of this project. Instead, the FM chirp signal is desired from a single integrated circuit (IC). The following section will cover the design work required to meet this objective.

2 Design

The goal of this design is to come up with an adjustable sinusoidal output that varies from the high MHz to low GHz range that can deliver up to 20mA to a 50Ω load. This adjustable sinusoid is intended to serve as the FM chirp signal described in the previous section. The IBM CMR7SF 3.3V CMOS 180nm process was used in this design as implemented in the Cadence design software suite.

A cross-coupled double ended MOS setup was chosen. The basic layout of this oscillator is shown below in Figure 2.

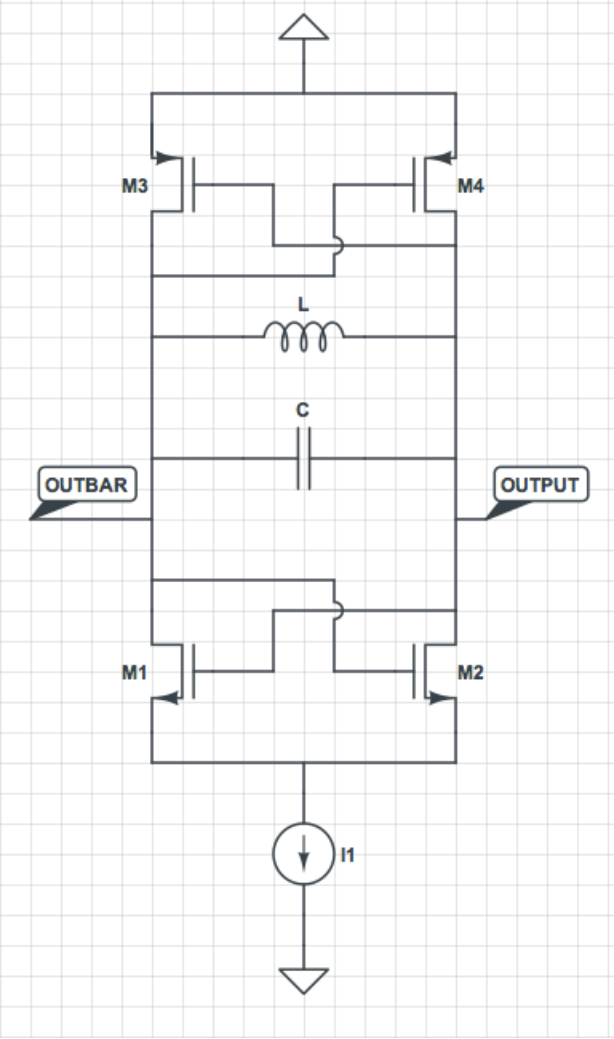

Figure 2: The Cross-Coupled Oscillator

Of the two outputs, labeled in Figure 2 as OUTPUT and OUTBAR, one is always high while the other low, and they are constantly switching. The cross-coupled gates of both the NMOS and PMOS transistor pairs ensure that only one transistor in each pair is on at any given time. This forces two distinct current paths from V_{DD} to ground, with the inductor and capacitor acting as energy storage elements between the two paths. These storage elements cause each output to oscillate between a high and low voltage in a sinusoidal manner at the frequency described in Equation 3.

$$f(Hz) = \frac{1}{2\pi\sqrt{LC}} \qquad \text{(Eq. 3)}$$

Inspection of Equation 3 shows that altering the inductance and/or the capacitance will change the frequency of oscillation. This is the foundation of many voltage controlled oscillator (VCO) designs, where some or all of the desired capacitance is replaced by a varactor used to act as a frequency tuner. For the purposes of the FM chirp application, this is not a viable option as the control voltage used to bias the varactor would be in itself a sinusoidal signal. While the recursive nature of requiring a VCO to operate a VCO may be comically ironic, it was overlooked for this application. Instead, a switched capacitor bank option was explored, where capacitance could be added and removed by switching in either additional or fewer parallel capacitors. However, this route was also abandoned, as the capacitors in the cap bank were on the order of 10^{-15}(fF), and the parasitics involved with switching those in and out proved to be too significant to generate a proper FM chirp.

Instead of a switched capacitor bank, a switched *oscillator* bank was developed. By switching on and off the current mirrors used to generate the bias current that drives each oscillator, the parasitics of switching on a different oscillator for each desired frequency are avoided entirely. Sixteen different oscillators were implemented, each with different inductances and capacitances to generate a different frequency signal. All 16 oscillators are switched on and off with their own control bit, which is just a digital high or low signal, and each output is tied to a single final output. There are a couple of additional wrinkles included in each oscillator that are not included in the conceptual schematic shown in Figure 2. To overcome the initial condition requirements to ensure reliable startup, one output is tied to ground while the other output is tied to the positive supply rail. These connections are in place only when the oscillator is in the ‘OFF’ state, and is therefore controlled by the same digital control bit as the oscillator as a whole. Additionally, each oscillator’s output is fed into a common drain amplifier, which provides the necessary current drive for a 50Ω load.

Figure 3 below shows an example of what a single oscillator looks like with the described modifications.

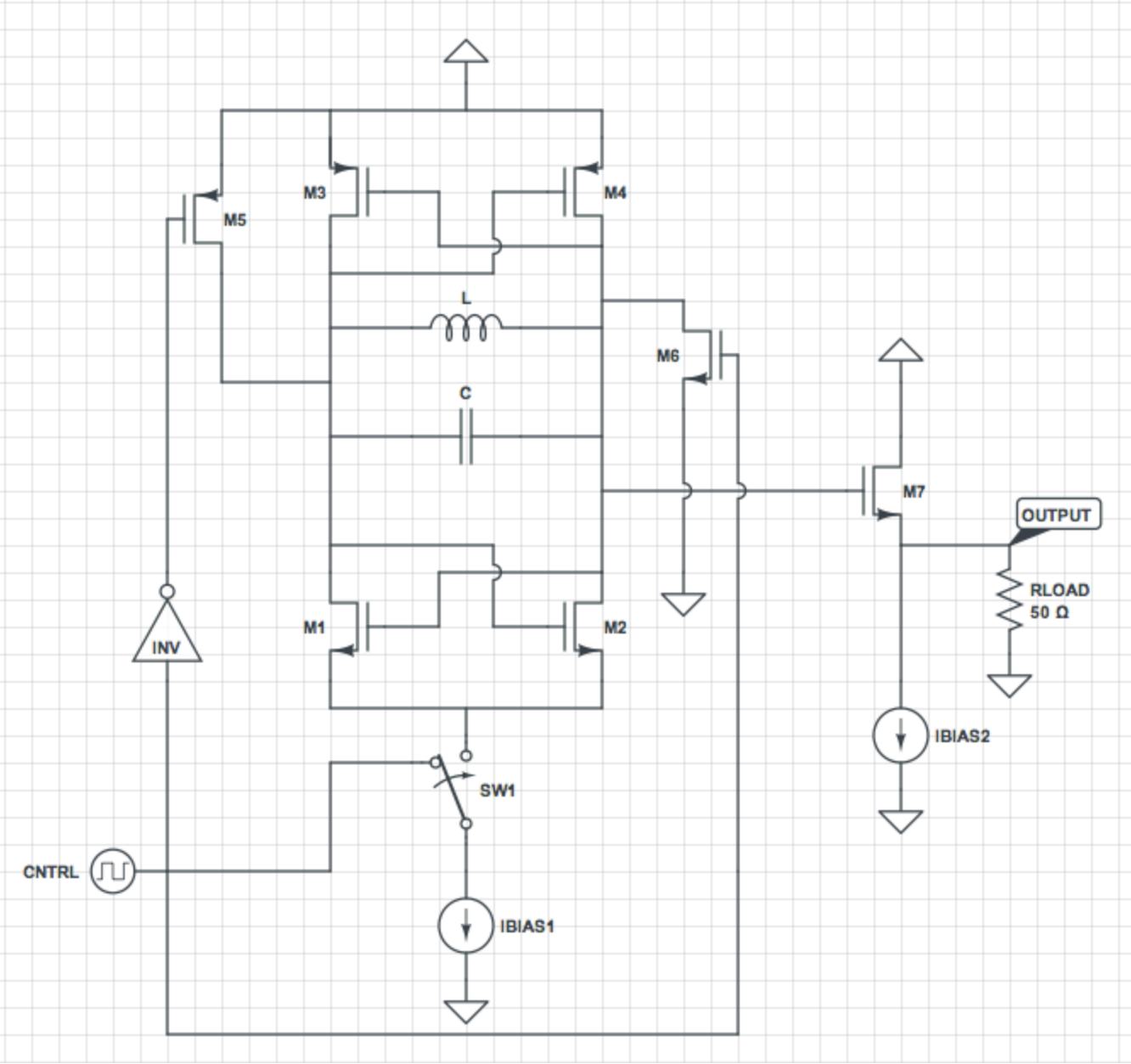

Figure 3: A Single Switched Oscillator Component

Note that M7 above is the common drain amplifier stage, while M5 and M6 are used to set the initial conditions necessary to ensure reliable startup.

In the Cadence design environment, 16 oscillators were created, intended to range in frequency from 600 MHz to 2.1GHz. This translates to a ΔF value of 1.5 GHz, which results in a range resolution of 10 centimeters as shown previously in Equation 1.

In addition to 16 oscillators, inverter and transmission gate schematics were also required to implement the entire switched oscillator system. The relevant schematics from Cadence are reproduced in the following figures.

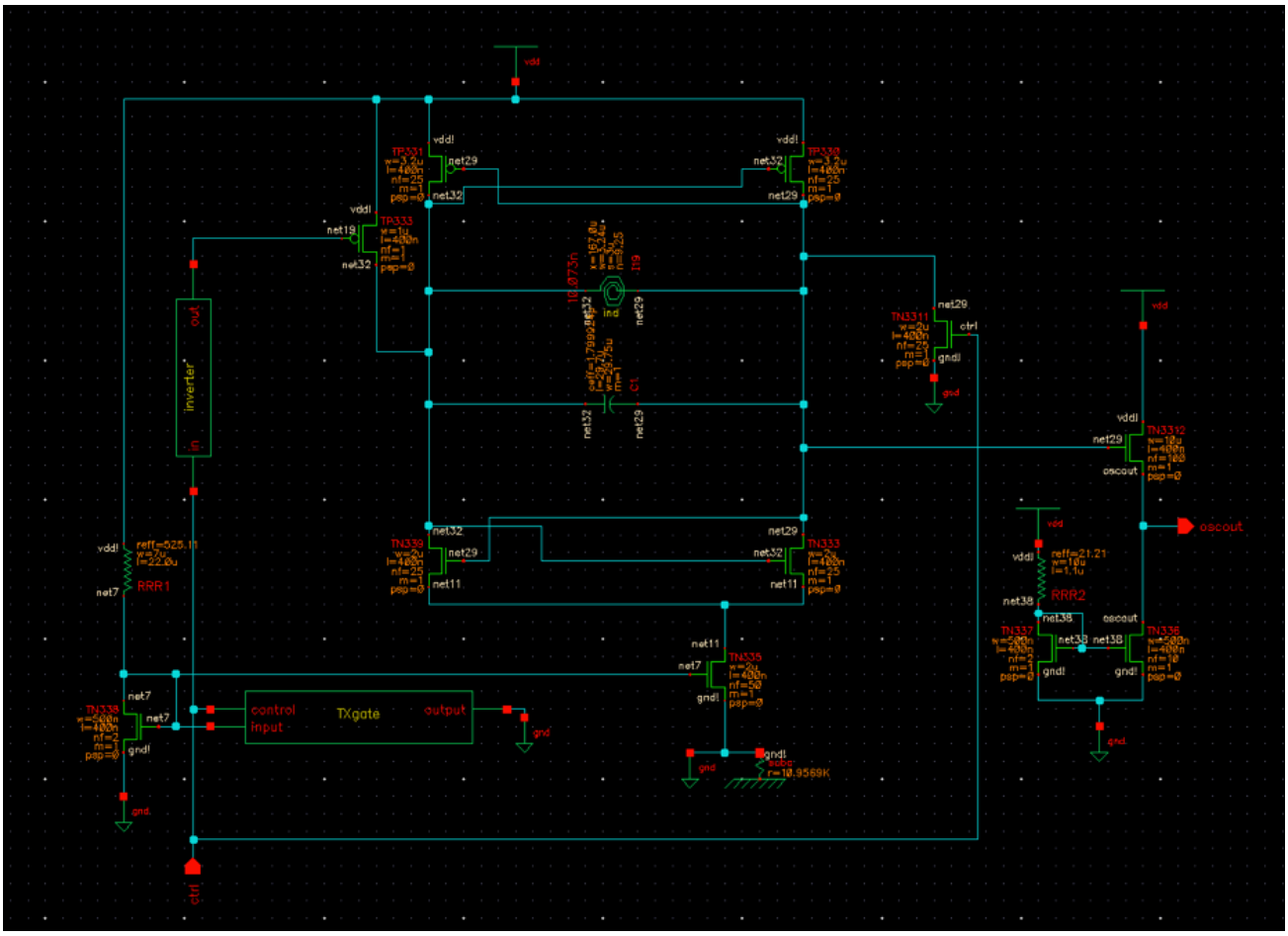

Figure 4: Oscillator Schematic

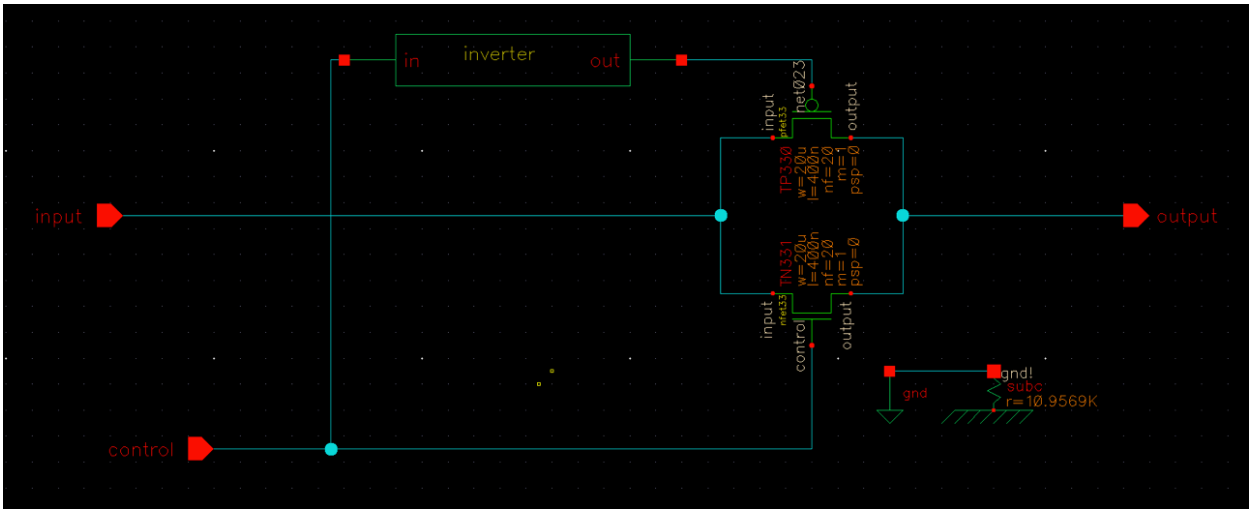

Figure 5: Transmission Gate Schematic

3 Layout

The layout view of a single oscillator is presented below in Figure 6.

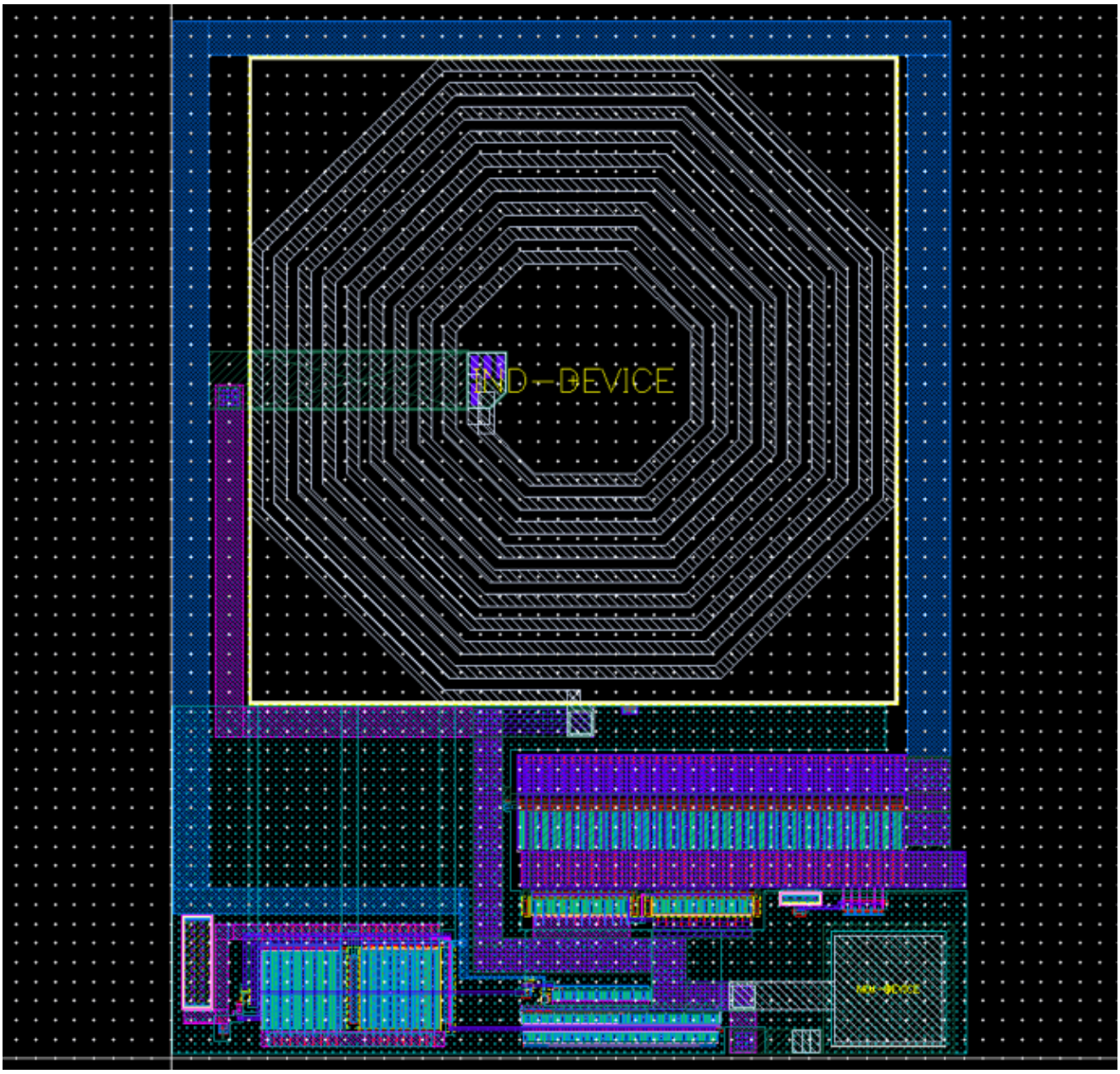

Figure 6: Oscillator Layout

The layout view of the transmission gate is presented below in Figure 7.

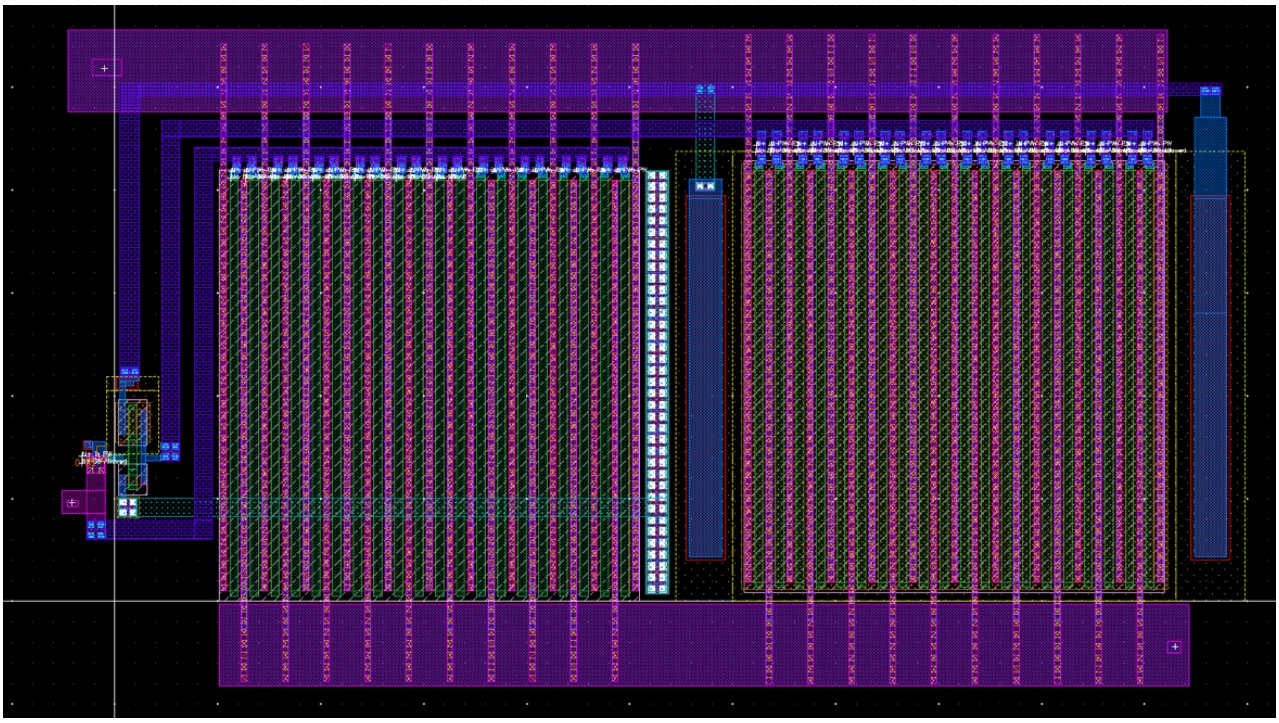

Figure 7: Transmission Gate Layout

Finally, the layout view of the entire switched oscillator is presented below in Figure 8.

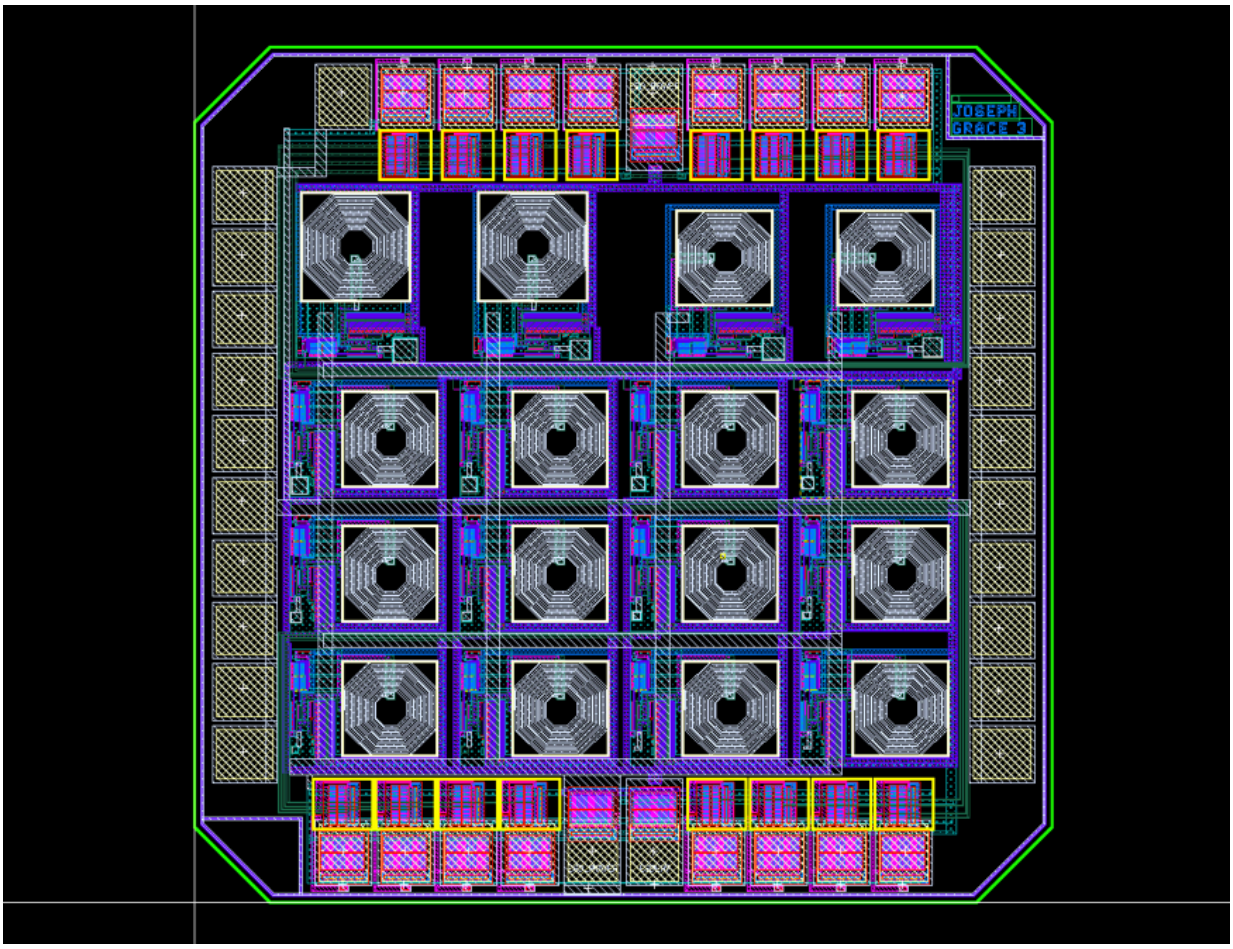

Figure 8: Full Switched Oscillator Layout

Note that this view includes all 16 oscillators and both CDM and HBM ESD devices.

4 Simulation

All simulations were performed with the package resistance, inductance, and capacitance included as described in the following pinout table:

Table 1: Oscillator Pinout

PINOUT				
pin name	**pin number**	**R (Ohms)**	**L (nH)**	**C (pF)**
output	31	0.0247	3.15	0.66
ctrl1	6	0.0661	4.37	1.43
ctrl2	7	0.0646	4.54	1.48
ctrl3	8	0.0498	3.69	1.05
ctrl4	9	0.0378	3.54	0.863
ctrl5	11	0.0247	3.15	0.66
ctrl6	12	0.0378	3.54	0.863
ctrl7	13	0.0498	3.69	1.05
ctrl8	14	0.0646	4.54	1.48
ctrl9	35	0.0661	4.37	1.43
ctrl10	34	0.0646	4.54	1.48
ctrl11	33	0.0498	3.69	1.05
ctrl12	32	0.0378	3.54	0.863
ctrl13	29	0.0378	3.54	0.863
ctrl14	28	0.0498	3.69	1.05
ctrl15	27	0.0646	4.54	1.48
ctrl16	26	0.0661	4.37	1.43
vdd	10	0.0247	3.15	0.66
ground	30	0.0247	3.15	0.66

While all sixteen oscillators were tested, the output of two oscillators is shown below in Figure 9:

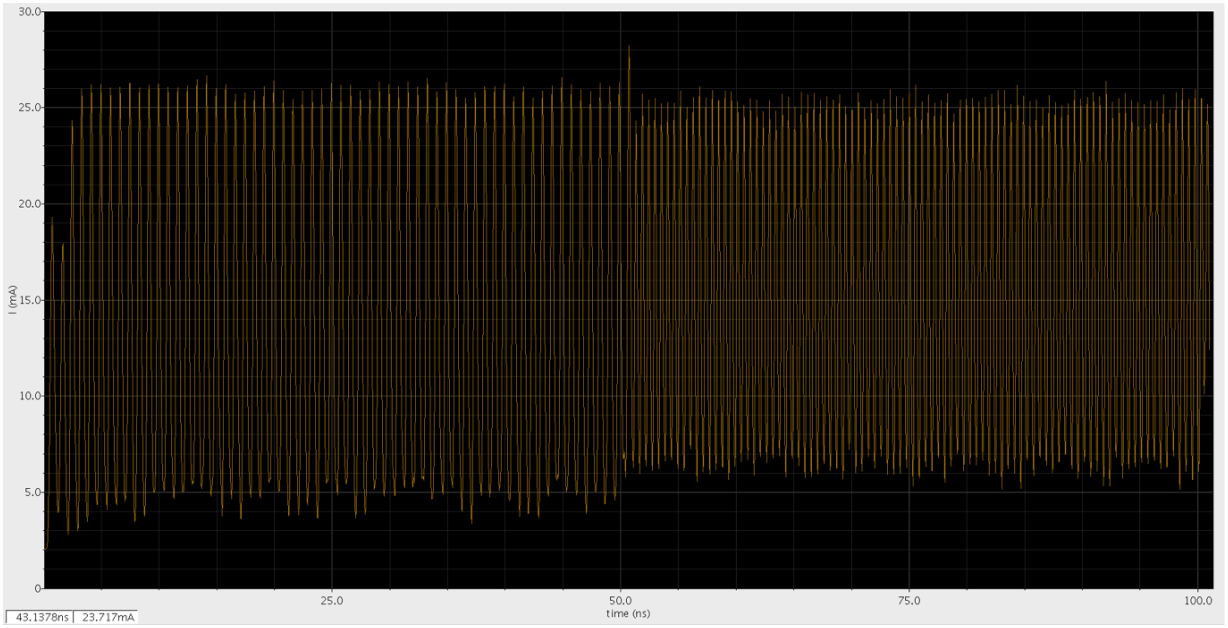

Figure 9: Oscillator Plot

The first 50ns of the plot shows the oscillator operating at 1 GHz and at 50ns the oscillator switches to 1.8 GHz. Figure 10 is the same plot but zoomed in to take a closer look at the transition at the 50ns mark.

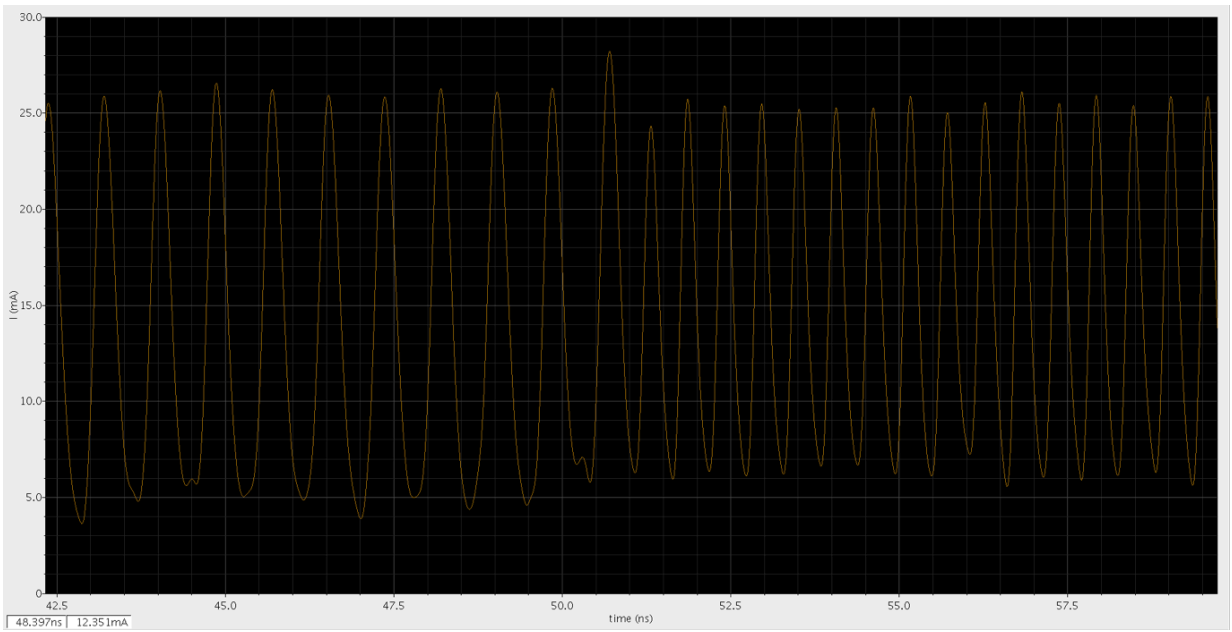

Figure 10: Oscillator Plot (Zoomed)

A complete table of simulation results is presented below in Table 2.

Table 2: Simulation Results

Oscillator Name	Desired Frequency	L (F)	C (H)	Time Span	Observed Frequency (Hz)
oscillator600meg	600 MHz	1.50E-08	3.65E-12	1.65E-09	6.06E+08
oscillator700meg	700 MHz	1.50E-08	2.45E-12	1.42E-09	7.04E+08
oscillator800meg	800 MHz	1.01E-08	3.10E-12	1.24E-09	8.06E+08
oscillator900meg	900 MHz	1.01E-08	2.28E-12	1.10E-09	9.09E+08
oscillator1000meg	1.0 GHz	1.01E-08	1.80E-12	9.88E-10	1.01E+09
oscillator1100meg	1.1 GHz	1.01E-08	1.41E-12	9.02E-10	1.11E+09
oscillator1200meg	1.2 GHz	1.01E-08	1.16E-12	8.32E-10	1.20E+09
oscillator1300meg	1.3 GHz	1.01E-08	8.90E-13	7.64E-10	1.31E+09
oscillator1400meg	1.4 GHz	1.01E-08	7.20E-13	7.09E-10	1.41E+09
oscillator1500meg	1.5 GHz	1.01E-08	5.50E-13	6.62E-10	1.51E+09
oscillator1600meg	1.6 GHz	1.01E-08	4.32E-13	6.15E-10	1.63E+09
oscillator1700meg	1.7 GHz	1.01E-08	3.32E-13	5.77E-10	1.73E+09
oscillator1800meg	1.8 GHz	1.01E-08	2.40E-13	5.51E-10	1.81E+09
oscillator1900meg	1.9 GHz	1.01E-08	1.58E-13	5.15E-10	1.94E+09
oscillator2000meg	2.0 GHz	1.01E-08	7.50E-14	4.80E-10	2.08E+09
oscillator2100meg	2.1 GHz	1.01E-08	5.00E-14	4.71E-10	2.12E+09

5 Analysis

Table 2 shows that all sixteen oscillators are performing at or near their intended frequencies of oscillation. It is important to note that these simulations were all performed with extracted parasitics included, as well as the package characteristics. Also worthy of note is the switching time presented in Figure 10. While in a real environment, each oscillator will be on for a time period on the order of tens to hundreds of microseconds, the switching time associated with each frequency change is on the order of 5 nanoseconds.

6 Verification

All schematics and layouts were tested in the Cadence design environment and underwent Assura DRC, ESD DRC, LVS, floating gate, and pattern density checking. Furthermore, QRC testing was included to simulate the chip's performance with all of the relevant extracted parasitic components.

7 Conclusion

A frequency modulated (FM) chirp signal was successfully implemented through a switched oscillator design. This design is intended to make up the first part of a LADAR IC system.

8 References

[1]

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[2]

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[5]

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