10-bit, 50MHz Pipeline A/D Converter

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Chapter 1

Introduction

1.1 Project Overview

There are two types of Analog to Digital Converters (ADCs): high speed and high resolution. Converters with a speed (or sampling rate) greater than 10MHz are considered high speed ADCs. They are used in applications such as imaging, ultrasound, digital cameras, communications, baseband digitization, etc. One of the issues of the high speed ADCs is their moderate resolution, in other words low dynamic range. In applications such as ultrasound, high speed and high resolution ADCs are needed. Currently, variable-gain amplifiers (VGAs) are implemented together with ADCs as a front-end component of the ultrasound system in order to compensate for the low dynamic range of the ADCs [1]. A 10-bit, 50MHz, pipeline architecture, analog to digital converter was designed as part of a thesis work that will investigate the dynamic range of a high speed converters. The converter was implemented with a 9 stage pipeline architecture, with 1.5 bits per stage. Outputs of the converter are the intermediate bits from the 9 stages. This allows access to the internal behavior of the pipeline architecture.

1.2 Objective

The objective of the project was to design a high speed, analog to digital converter which will operate from a 5V power supply and provide the intermediate stage outputs off chip. The converter should accept -1 to 1 volt (2.5V common mode offset) fully differential input.

1.3 Pipeline Architecture

In a pipeline architecture, several stages with a low resolution per stage are cascaded to obtain a high overall analog to digital converter resolution. They are typically used in moderate resolution, high-speed applications. The main concept and design of this A/D converter was adapted from [2, 3, 4]. A generic pipeline converter is shown in Figure 1.1. Each 'stage' of the ADC includes a low resolution quantizer. The i^{th} stage provides two outputs. The first output, q_i, is a coarse resolution digital representation of its input voltage. q_i is an integer value that can range from 0 to $2^{B_i} - 1$, where B_i is the bit resolution of the i^{th} stage. The second output is a residual voltage, r_i, obtained by measuring the difference between the input and it's digital representation q_i. The residual voltage is passed onto the next stage in the pipeline and q_i is sent to the digital error correction logic. All the q_i's are collected and using digital error correction a final high resolution ADC is produced. In the case of 1.5bits/stage architecture, digital error correction used is referred to as redundant signed digit (RSD) correction [5].

All stages are referenced to the same clock. Once stage 1 produced r_1 and q_1, stage 2 begins quantizing r_1 while Stage 1 is processing the next input sample. This continuous processing of samples is the concept of *pipelining*. There is one complete conversion per clock cycle, allowing high speed conversion. Theoretically, the resolution of the pipelined ADC is governed by the number of stages implemented. Increasing the number of stages will increase the ADC resolution. In reality, the result does not improve after some point as a consequence of the component mismatch and noise [5]. Also, adding more stages puts a requirement on more real-estate on a chip. One disadvantage of a pipeline architecture is introduction of latency. In the case of a 10-bit ADC, 6 initial clock cycles are required before the first digital output becomes valid. The 6 clock cycle latency is due to the input sample propagating through the 9 stages to obtain a 10-bit converter resolution. All stages of pipelined ADC rely on a two phase non-overlapping clock for operation. More on this in Chapter 2.

Figure 1.2 shows a block diagram of a stage. A sample and hold (S/H) is on the input of each stage block since conversion must take place while the previous stage is processing the next sample. Each stage has a B_i-bit sub-ADC to provide the digital output for that stage. A sub-DAC with similar resolution is used to convert this digital output to an analog voltage. This voltage is subtracted from the initial input sample giving the error voltage, e_i. The resulting residual error, e_i, is scaled by a gain factor and sent to the following stage as r_i. The gain depends on a stage resolution and typically has a value of 2^{B_i-1}. The scale factor is used to scale

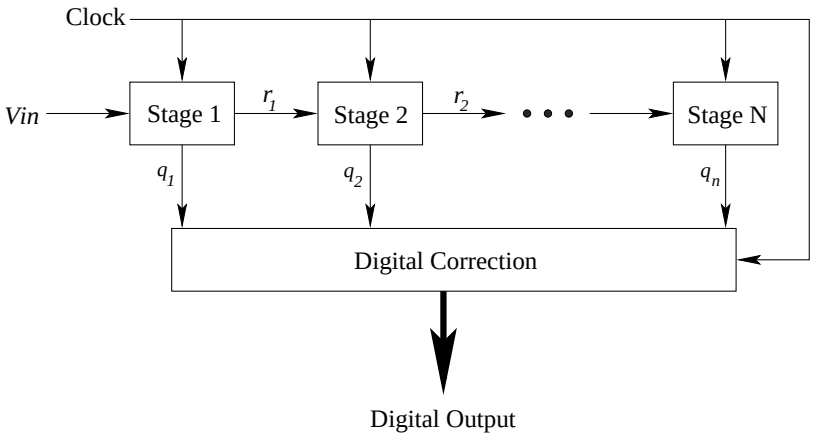

Figure 1.1: Generic Pipeline ADC block diagram.

the residual to the full operating range of the next stage. Design described in this report implements 9 stage pipelined architecture with 1.5 bits per stage. Two bits are required to obtain 1.5 bits and therefore 18 bits of raw output are available for digital error correction. The final resolution is 10 bits. The ADC designed here does not implement the digital error correction logic. The 18 bits from nine stages are instead sent to a shift register until the last stage completes its conversion and the outputs are then routed off-chip.

1.4 Specifications

Table 1.1 gives simulated performance specifications of a pipeline ADC. These specifications are based on operation at the room temperature ($27°C$) with the following input conditions:

- Fs = 51.2MHz
- Fin = 24.8MHz
- Ain = 450mV

Where, Fs, Fin and Ain correspond to sampling frequency, input frequency and input voltage, respectively.

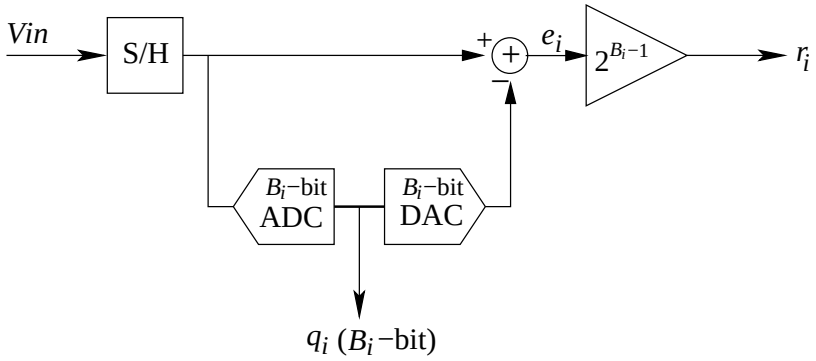

Figure 1.2: Generic stage block diagram.

Specification	Value	Units
Sample rate	50	MHz
Effective number of bits (ENOB)	8.97	bits
Supply	5	V
Input range	-1 to 1	V
Vcm	2.5	V
Vcm_{OTA}	1	V
$Vref^{+}$	3	V
$Vref^{-}$	2	V
Power consumption	192	mW
Current consumption	40	mA

Table 1.1: Table of Simulated Specifications.

Macro number	Name
1	Gain Stage
2	Sub-ADC
3	Sub-DAC
4	Clock
5	Shift Register
6	Even Stage
7	Odd Stage
8	Last Stage

Table 1.2: Table of Macros.

1.5 Macros

Table 1.2 lists the higher level blocks used in the particular design. Function of each block is discussed in details in Chapters 2 and 3.

1.6 Pin-Out Assignment

Table 1.3 gives the assignment of all pins when packaged in a 40 pin DIP. Normal operation requires the following inputs: power, reference voltage, input signal, input clock and two common mode voltages (Vcm and Vcm_{OTA}). The outputs consist of intermediate bits of 9 stages.

1.7 Design Methodology

Kannan Sockalingam and Rick Thibodeau successfully designed and fabricated a 10-bit, 5MHz, pipeline ADC through MOSIS in AMI's C5N process technology [3]. The design of this 10-bit, 50MHz, pipeline ADC was based on their work discussed in [3]. The idea was to look at [3] and improve components that were limiting the speed of the 10-bit converter to 5MHz. Components crucial in determining the speed and therefore in need of improvement were: operational transconductance amplifier (OTA), clock, differential comparators (sub-ADC), sub-DAC and digital output buffers. Each of these components were looked at separately and improved to work at the speed of 100MHz. Once the speed requirement was accomplished, a pipeline stage was assembled and tested. Refer to Figure 1.2 for

Pin Num.	Pin Name	Function
1,20	VCCD	Supply voltage for the output buffers (Typically 5V)
2,3,5,7,15,17,19	GND	Ground connection
4,6,14,16,18	VDD	Supply voltage (Typically 5V)
8	VCM	Common-mode voltage (Typically 2.5V)
9	VREF+	Positive reference voltage (Typically 3V)
10	VIN+	Positive side of the differential input
11	VIN-	Negative side of the differential input
12	VREF-	Negative reference voltage (Typically 2V)
13	VCM(OTA)	Common-mode voltage for the OTA (Typically 1V)
21	PHI2	Reference clock for the outputs
22	MSB8	Digital output from stage 2 (MSB)
23	LSB8	Digital output from stage 2 (LSB)
24	LSB9	Digital output from stage 1 (LSB) - most significant bit
25	MSB9	Digital output from stage 1 (MSB) - most significant bit
26	MSB7	Digital output from stage 3 (MSB)
27	LSB7	Digital output from stage 3 (LSB)
28	LSB6	Digital output from stage 4 (LSB)
29	MSB6	Digital output from stage 4 (MSB)
30	MSB5	Digital output from stage 5 (MSB)
31	LSB5	Digital output from stage 5 (LSB)
32	CLK	External clock
33	LSB4	Digital output from stage 6 (LSB)
34	MSB4	Digital output from stage 6 (MSB)
35	MSB3	Digital output from stage 7 (MSB)
36	LSB3	Digital output from stage 7 (LSB)
37	MSB2	Digital output from stage 8 (MSB)
38	LSB2	Digital output from stage 8 (LSB)
39	MSB1	Digital output from stage 9 (MSB) - least significant bit
40	LSB1	Digital output from stage 9 (LSB) - least significant bit

Table 1.3: Table of Pin-Outs.

the stage components. In the pipelined architecture the final resolution of the converter depends on the resolution accuracy of the first two stages. These correspond to the most significant bits of the converter. For the current design, outputs of a first two stages need to be accurate within 2mV in order to obtain the final 10 bit resolution. The calculation is based on the equation: $1LSB = Vpp/(2^n - 1)$, where Vpp corresponds to the full-scale range of the converter and n is the converter resolution. The equation defines the number of devisions of the full analog range and therefore measures the resolution of the converter. The goal was to design a stage where the output is accurate within 2mV at the speed of at least 50MHz.

A fellow undergraduate student, Eric McCarthy, designed an OTA capable of at least 10 bit resolution at 100MHz [6]. Details of the OTA design can be found in [6]. The remaining components were re-designed based on research and knowledge of analog and digital circuit design and help from Prof. Hummels, Prof. Kotecki and graduate student Steven Turner. Details of a design and simulation results are discussed in Chapter 2.

Chapter 2

Circuit Design

This chapter discusses the concept and design of the individual building blocks of the pipeline A/D converter. The performance of these blocks will determine the performance of each pipeline stage and the ultimate performance of the converter. Blocks discussed in the chapter are:

1. 2-phase non-overlapping clock
2. Sub-ADC
3. Sub-DAC
4. Gain stage
5. Last stage
6. Shift register
7. Output buffers

2.1 2-Phase Non-Overlapping Clock

All stages of pipeline ADC rely on a two phase non-overlapping clock for operation. The design and concept of the two phase non-overlapping clock was adopted from [2, 3]. The two phases, ϕ_1 and ϕ_2, have a 180° phase shift and a delay between the clock transitions. All the odd stages sample during phase ϕ_1 and present a valid residue output to the next stage during phase ϕ_2. Even stages work on the

opposite phases. All the stages operate at the same time making a pipeline architecture a choice for a high speed ADC design. After the initial inherent delay in the pipelined ADC, the digital word becomes available at every clock cycle. As alternate stages are clocked by alternate clock phases, the components in a stage must settle within half the period of the main clock. If the main clock is running at 50MHz, the longest time for any component within the stage to settle would be $\frac{20}{2} = 10$ns.
The bottom plate sample and hold circuit (S/H) is used in a design of this converter. The bottom plate S/H circuit insures for a signal-independent charge injection [2]. To implement the bottom plate S/H circuit the additional clock signals, ϕ_1' and ϕ_2', are introduced. ϕ_1' and ϕ_2' are designed to turn off before ϕ_1 and ϕ_2 respectively, [2]. Figure 2.1 illustrates the four clock waveforms together with the timing requirements used in the design. The non-overlapping period t_{nov} and the lag time, t_{lag}, between ϕ_k and ϕ_k', t_{lag} are the two timing requirements needed to implement the non-overlapping clock and bottom-plate switching respectively. t_{nov} is the time from the falling edge of ϕ_1 to the rising edge of ϕ_2. t_{lag} is the time from the falling edge of ϕ_1' to the falling edge of ϕ_1. The same is true for ϕ_2 and ϕ_2'.

2.1.1 Clock Design

The clock generator design was adapted from [2, 3] and was resized to meet the timing requirements for the current design. The clock was designed to run at 100MHz and Figure 2.2 shows the schematic of the clock generator. There are four different components presented in Figure 2.2: *inv_min*, *2nand*, *delay_1* and *buffer_100fF*. *Inv_min* is the minimum sized inverter. The $\frac{W}{L}$ for the devices are, PMOS= $\frac{3}{0.6}$ and NMOS=$\frac{1.5}{0.6}$. *2nand* is a two input NAND gate. The internal circuit and transistor sizing of a NAND gate can be found in Appendix A. Duration of generated clock phases depends on a propagation delay of the various gates in the clock generator. *Delay_1* consists of four minimum sized inverters cascaded together and it used to adjust the the 'on time' of four clock phases. *Buffer_100fF* is a buffer designed to drive a 100fF load. The internal circuit together with the transistor sizes of the buffer are provided in Appendix A. All clock outputs are buffered to increase the drive capability.

As it was mentioned above, the clock was designed to run at 100MHz. This means each stage is required to settle in 5ns. Due to the short settling time, the timing requirements for the clock, t_{nov} and t_{lag} need to be well preserved when used within

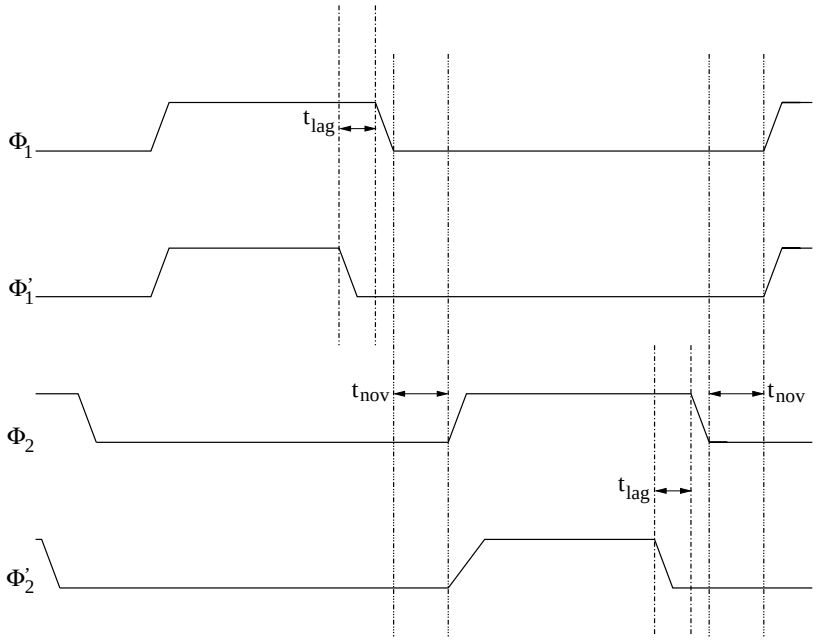

Figure 2.1: Two phase non-overlapping clock timing diagram.

each stage in order to maintain the signal-independent charge injection [2]. The non-overlap period, t_{nov} is used by the sub-ADC to digitize the sample and select the appropriate DAC level. If this time period is too short the capacitors of the gain stage will not have time to settle to their final value to be passed on to the next stage. In order to preserve t_{nov} and t_{lag} times, each of the nine stages contains four 100fF buffers. The buffers ensure the clock is capable of driving each stage with originally designed t_{nov} and t_{lag} times. The advantage of having clock buffers at each stage is discussed in Chapter 4.

2.1.2 Clock Simulation Results

Figures 2.3 and 2.4, show the simulation results for the clock generator. This simulation was done using a 100MHz square wave input with an amplitude of 5V. Test was run using the package model pins. Refer to the Appendix A for the schematics of the power supply. Figure 2.3 shows the t_{lag} period between ϕ_1 and ϕ_1', and it is approximately 0.35ns. Figure 2.4 shows the t_{nov} period between ϕ_1 and ϕ_2, and it is approximately 0.7ns. Therefore, each stage needs to sample and

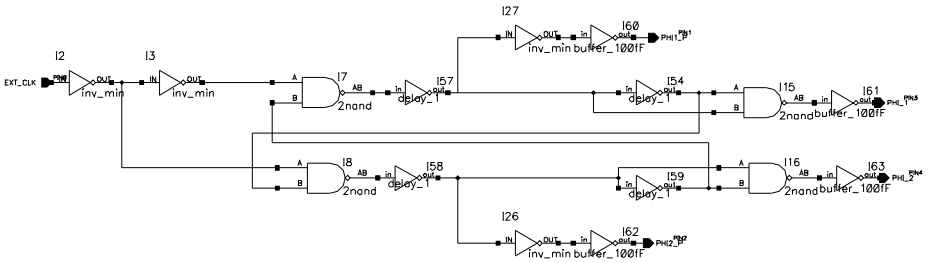

Figure 2.2: Schematics of a two phase non-overlapping clock.

$DifferentialInput$	$\frac{+V_R}{4}$ $comparator$	$\frac{-V_R}{4}$ $comparator$	$Sub-ADCoutput$
$Vin^+ - Vin^-$	$>$	$>$	11
$Vin^+ - Vin^-$	$<$	$>$	01
$Vin^+ - Vin^-$	$<$	$<$	00

Table 2.1: Outputs of a sub-ADC block.

quantize the input, drive the sub-DAC, quantize the residual and latch the output in 4ns. In simulation the output was connected to 100fF load because the clock generator was designed to drive the mentioned load.

2.2 Sub-ADC

Function of the sub-ADC is to quantize the input signal and provide the intermediate bits for each stage. For 1.5 bits per stage architecture sub-ADC can have one of three binary states as an output: 00, 01, 10. The sub-ADC consists of two differential comparators with thresholds set at $\frac{+V_R}{4}$ and $\frac{-V_R}{4}$, where $+V_R$ and $-V_R$ represent the range of the differential input signal. Refer to Figure 2.5 for the locations of sub-ADC thresholds and corresponding digital outputs. Table 2.1 lists the outputs of the two differential comparators which are part of the sub-ADC. These outputs are sent to sub-DAC block. Logic within the sub-DAC block will generate the three allowable binary states for a 1.5 bit per stage architecture. Refer to section 2.3 for more on binary outputs of the stage.

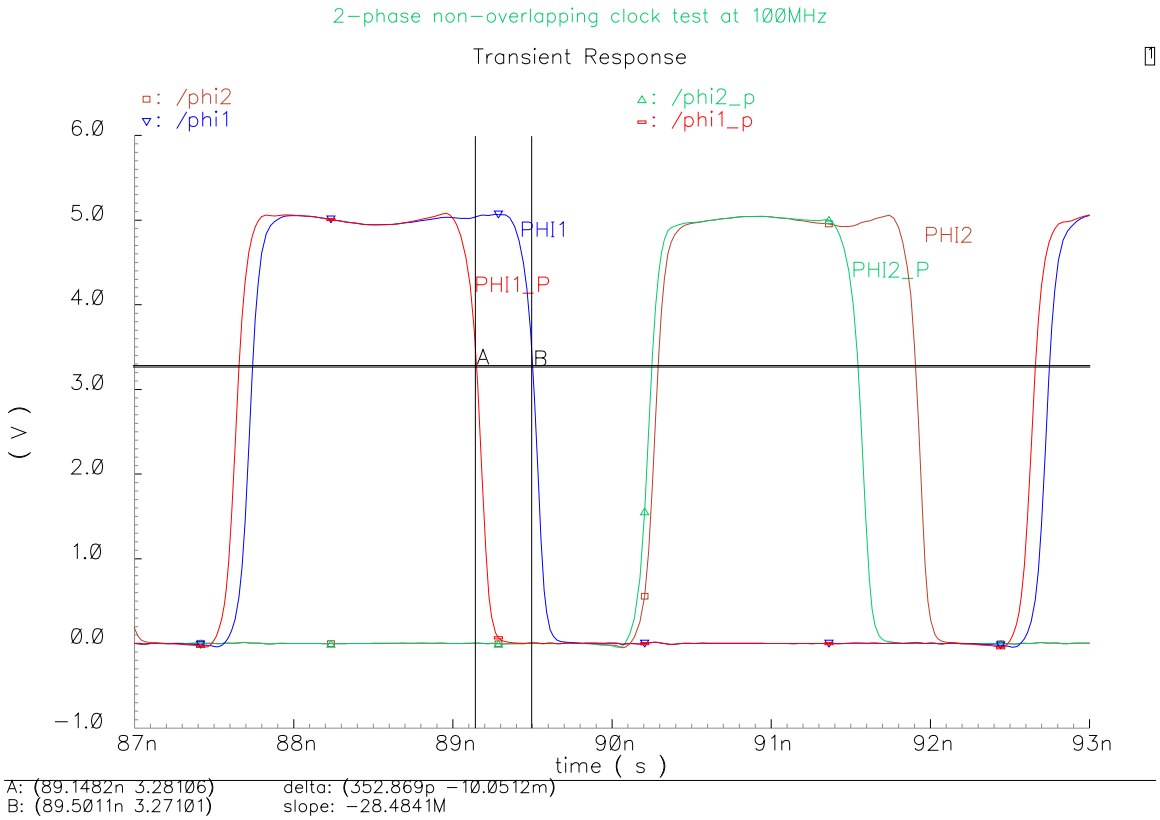

Figure 2.3: Clock simulation at 100MHz - t_{lag}.

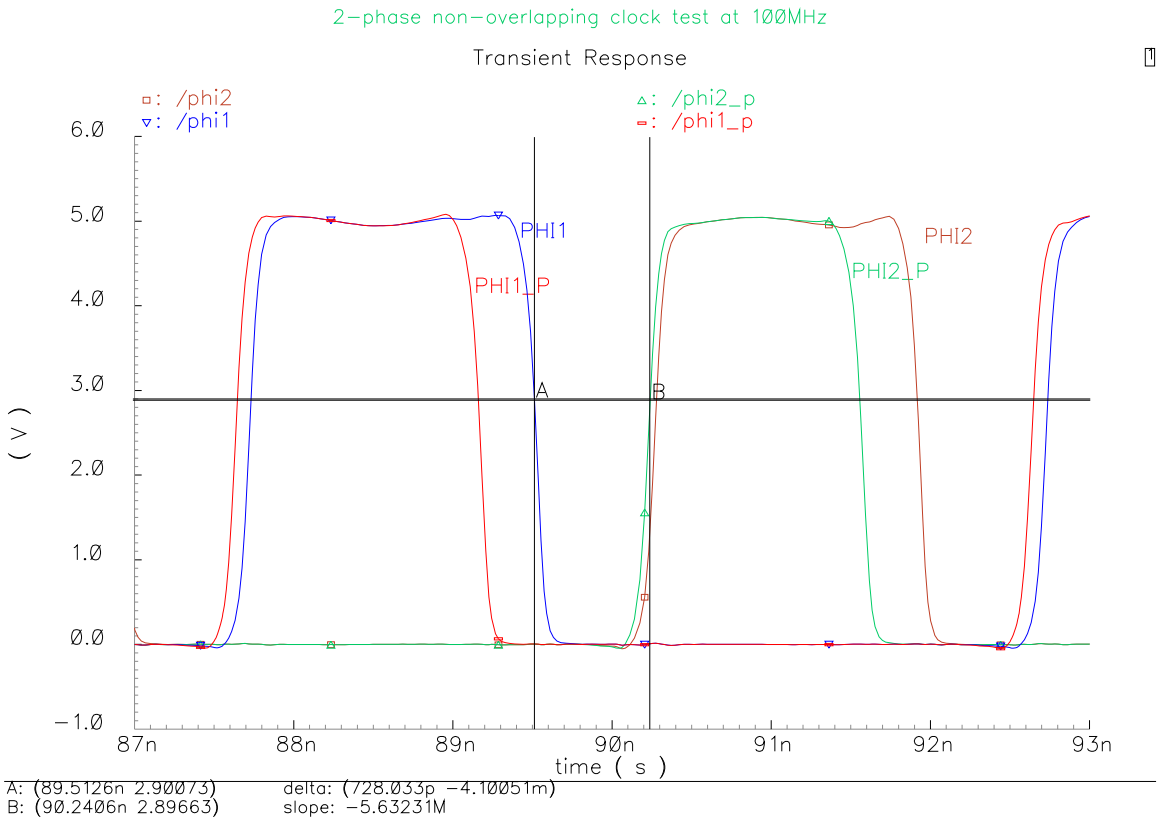

Figure 2.4: Clock simulation at 100MHz - t_{nov}.

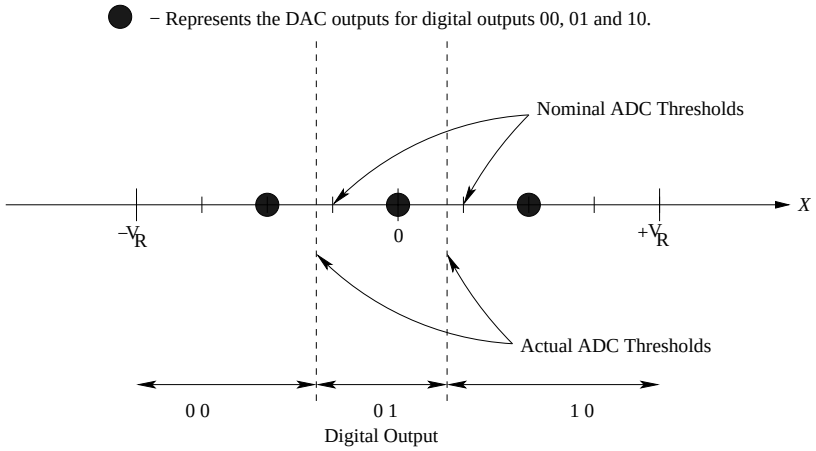

Figure 2.5: Sub-ADC threshold locations and corresponding digital outputs of sub-DAC.

2.2.1 Differential Comparator

The design and concept behind the differential comparator is adopted from [2]. It consists of capacitor network, clocking circuitry and voltage comparator. Figure 2.6 shows the differential comparator schematic. Four capacitors are used to obtain $\frac{+V_R}{4}$ and $\frac{-V_R}{4}$ thresholds for the comparison operation. Capacitor and switch sizes were taken from [3]. They were adequate size in to run at 100MHz. Voltage comparator and bias voltage block were optimized to meet the 100MHz specifications.

Voltage Comparator

In Figure 2.6 the block titled CMP_CLK is a clocked voltage comparator. As mentioned before, each sub-ADC has two differential comparators. One has the threshold set to $\frac{+V_R}{4}$ and other to $\frac{-V_R}{4}$. The $\frac{-V_R}{4}$ threshold is obtained by changing the reference voltage connections, meaning in place of $+V_{REF}$ we connect $-V_{REF}$ and vice versa. V_{REF}s are the reference voltages of the converter. For the current design $V_{REF}+$ is 3V and $V_{REF}-$ is 2V.

When building a high speed voltage comparator, the accuracy of the comparator suffers. importance was placed on building a comparator which will make a definite decision and maintain it. This was a challenge when designing the high

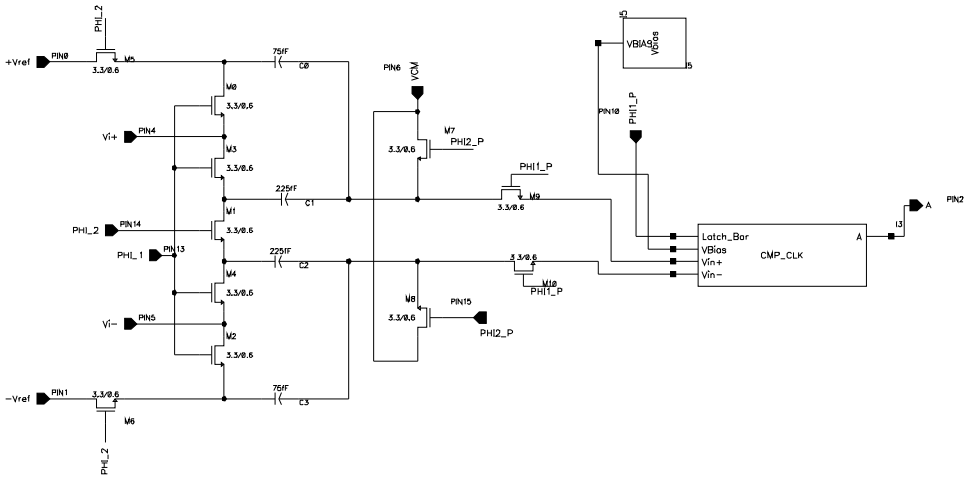

Figure 2.6: Differential comparator schematics.

speed comparator for the current ADC. The comparator had a tendency to change its decision when it should have been held constant so the sub-DAC could processes it. This problem occurred when the differential input was close to $\frac{+V_R}{4}$ or $\frac{-V_R}{4}$.

The high speed comparator design was taken from [7] and adapted to meet the required speed and accuracy. Figure 2.7 shows the final schematic of the clocked voltage comparator design. The design consists of pre-amplification stage followed by a decision making stage. The output is latched when $\overline{Latch}$ is high. After the comparison is made digital output levels are produced. The M0 and M1 transistors sense the change at the input and accordingly activate the current mirror pairs, M8, M11 and M9, M10. Depending on the difference in the input signals, one of the transistor pairs will be turned on and other will be turned off. These transistors are part of the pre-amplification stage. Depending on the decision of the pre-amplification stage, transistors M4 and M5 of the decision making stage will turn on/off to determine comparator's digital output. Transistors M7, M19 and M6, M20 are inverter pairs which buffer the output and restore the full logic levels. NMOS transistor of the inverter pairs (M7 and M6) are sized to be larger than the PMOS transistors because it took longer for the digital output to

settle to a low level than high level. To solve this problem the width of the NMOS transistors were increased to increase speed. Also, this particular design has a pre-charged output that will erase memory from the previous comparison. Whenever the comparator is not active the output is pulled high. This allows the PMOS transistors M19 and M20 to be minimum sized because if the comparator's decision is a logic high, the output has already been pre-charged. Transistors M12, M13 and M14 pre-charge the output to logic high during the comparator's off time. Transistors M16 and M17 function is to turn the decision making stage off during comparator's off time.

The current comparator design has a signal and its compliment as outputs. The design implemented does not implement the compliment signal of the comparator. Instead the compliment signal is obtained through the inversion of the comparator output. The inverter is part of the sub-DAC block. This was done to avoid indecisive comparator outputs. Four transistors whose sizes found to be crucial in determining the speed of the converter were M10 and M11 of the pre-amplification stage and M4 and M5 the decision making stage. These transistors were optimized to meet the speed and accuracy needed.

Bias Voltage Block

The bias voltage block generates 10μA of current needed by the current mirror in the voltage comparator. Figure 2.8 shows a schematic view of the voltage bias block. Three NMOS transistors are cascaded together and optimized in size to generate a current of 10μA. The circuit is very sensitive, meaning the current output can fluctuate between 10μA and 15μA, however this current fluctuation had no effect on the performance of the voltage comparator. This fluctuation can be due to the noise introduced by the components surrounding the biasing block. The advantage of the design was its small physical size once layed out. Refer to Appendix B for the layout of the bias voltage block.

Voltage Comparator Simulation Results

The voltage comparator was characterized separately before adding the capacitor and switching network to produced a differential comparator. The differential comparator performance will follow voltage comparator results.

Figure 2.9 shows the circuit used to test the performance of the voltage com-

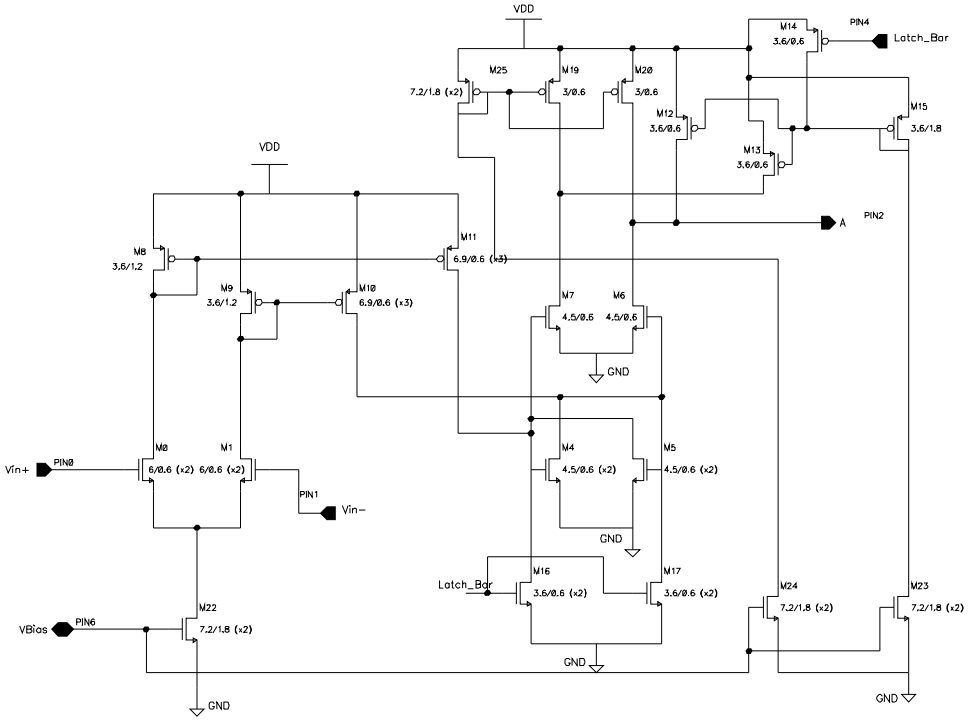

Figure 2.7: Voltage comparator schematic.

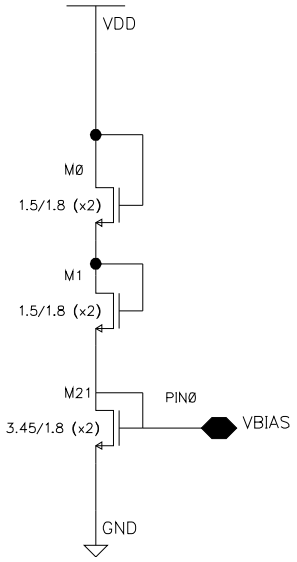

Figure 2.8: Biasing circuit.

parator. Particular tests were run at 50MHz. The performance of the comparator at 100MHz will be shown after the differential comparator results are discussed. For the simulation, $Vin-$ was held constant at 2.5V and $Vin+$ was ramped from 2.45V to 2.55V. This voltage ramp was used to show the accuracy of the decision being made by the comparator. At the same time this test illustrates the problem of comparator being indecisive about the decision being made. $\overline{Latch}$ was set to ϕ_1', meaning that outputs are valid on ϕ_2'. Figure 2.10 shows a plot of the input, output, $\overline{Latch}$, ϕ_1', and ϕ_2' when the output is valid. On the falling edge of ϕ_1' the input is latched and the decision is made by the end of ϕ_2'. When ϕ_1' is high, the comparator's output is pre-charged to erase any previous comparison state. When the inputs are very close to each other one can notice the indecisive output. However, even before the end of ϕ_2', the final output decision is made and it is stable. Figure 2.11 show an expanded view of the same plot. Here one can see the time required for the comparator to make a decision once the inputs are latched on the falling edge of ϕ_1'. The comparator settles to logic level of the decision being made in 600ps.

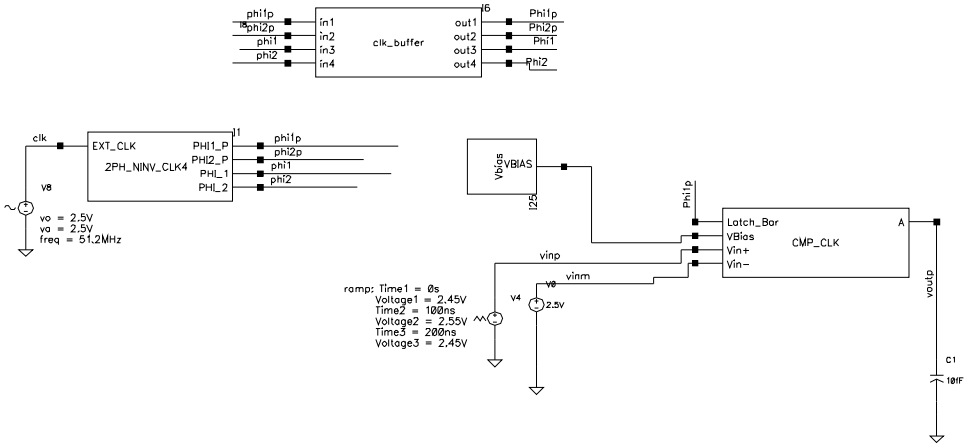

Figure 2.9: Circuit used to test voltage comparator.

2.2.2 Differential Comparator Simulation Results

Figure 2.12 shows the circuit used to simulate the performance of the differential comparator at two different threshold voltages. Block labeled DIFFERENTIAL_CMP contains a circuit shown in Figure 2.6. The differential comparator with output A has its threshold set to $\frac{+V_R}{4}$ and differential comparator with output B has its threshold at $\frac{-V_R}{4}$. This was accomplished by connecting $-V_{REF}$ to $+V_{REF}$ and vice versa. For the simulation, $Vi-$ was held at 2.3V and $Vi+$ was ramped from 2.45V to 2.55V. After the switching network, the positive side of the voltage comparator will see

$$Vi^{+} - \frac{+V_{REF} - V_{CM}}{4}$$

and the negative side of the voltage comparator will see

$$Vi^{-} + \frac{-V_{REF} - V_{CM}}{4}$$

Refer to Figure 2.6 for the switching network and voltage comparator combination. The amplitude of the clock was set to 5V and the frequency to 102.4MHz. Figure 2.13 shows the performance of two differential comparators at different threshold. The inputs are taken after the switching network, meaning before voltage comparator. By the end of ϕ_1' the input is latched for the comparison and on ϕ_2' the output is valid. It can be seen that the differential comparator is performing well at 100MHz.

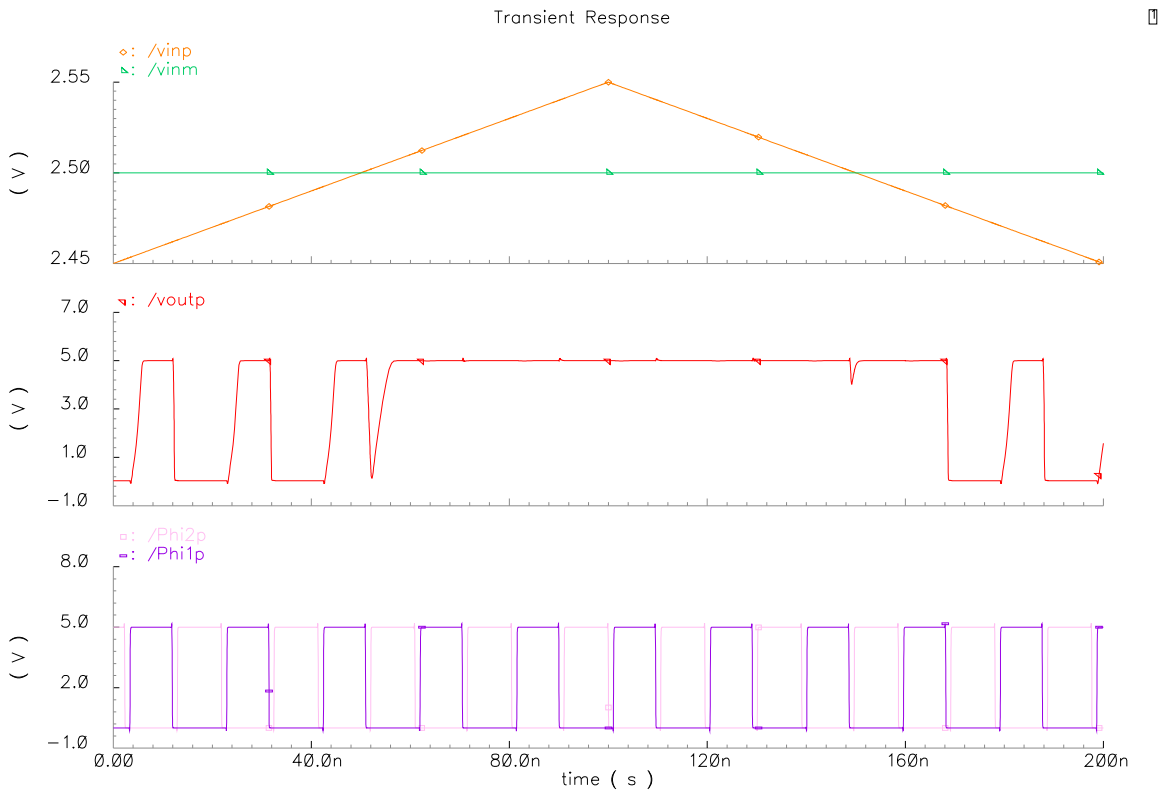

Figure 2.10: Voltage comparator performance at 50MHz.

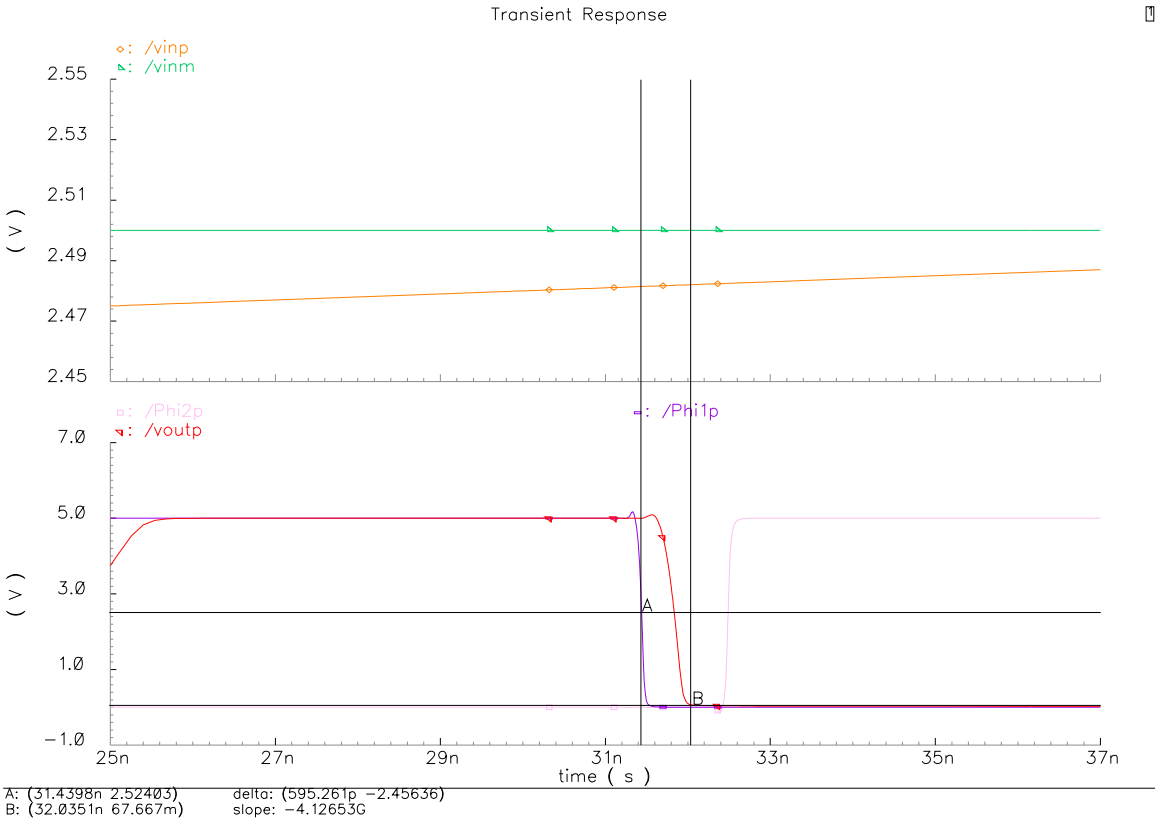

Figure 2.11: Voltage comparator transition time.

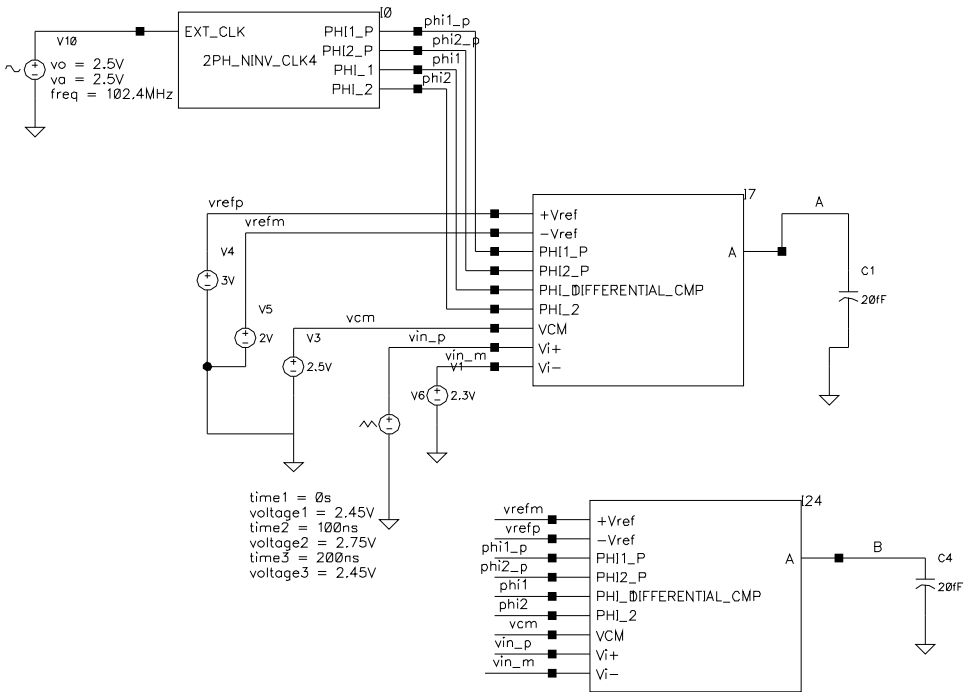

Figure 2.12: Circuit used to test differential comparator.

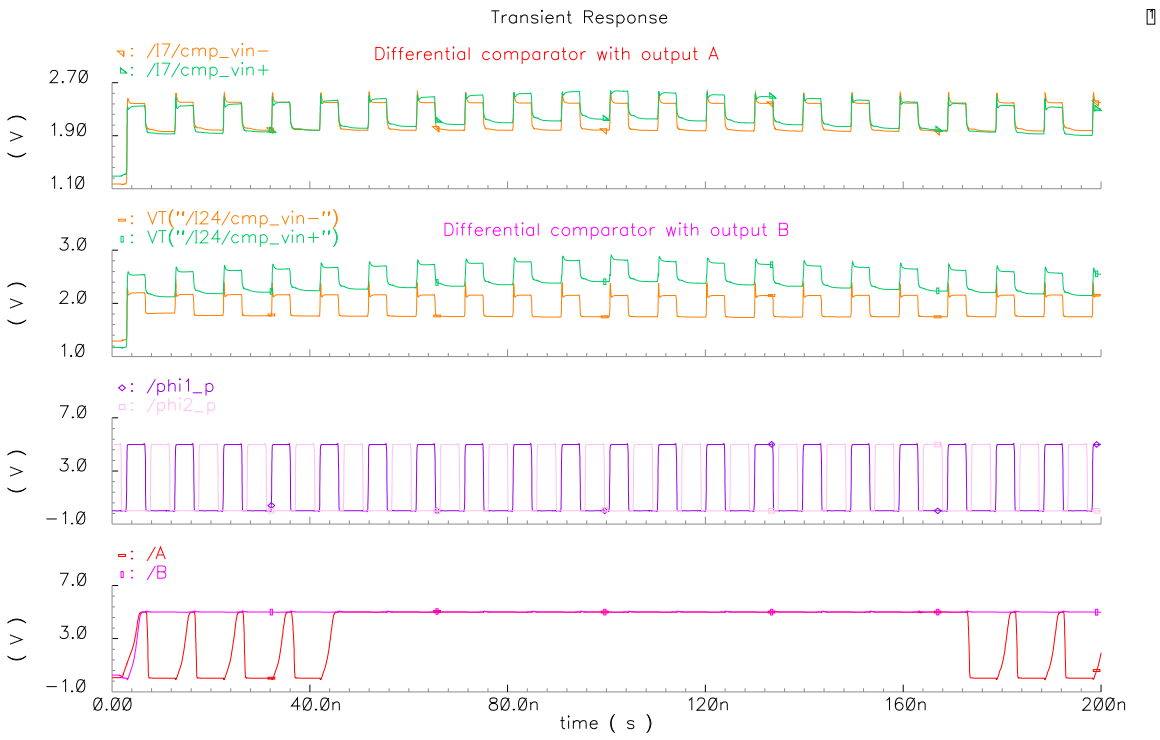

Figure 2.13: Differential comparator (sub-ADC) performance at 100MHz.

2.3 Sub-DAC

The role of the sub-DAC is to supply the gain stage with the analog voltage level that represents the quantized portion of the input sample. The quantized portion is subtracted from the input signal to create a residue that will be sent to the next stage. Also, as mentioned in section 2.2, the sub-DAC calculates the digital word for that stage according to the outputs from the sub-ADC. For an architecture with 1.5 bits per stage, the sub-ADC can have one of the three binary outputs: 00, 01, 10. These corresponds to the sub-DAC outputs of $\frac{-V_R}{2}$, 0, $\frac{+V_R}{2}$ respectively. Refer to Figure 2.5 for sub-DAC threshold locations and corresponding binary outputs for the stage.

2.3.1 Sub-DAC Circuit

The concept and logic for the sub-DAC circuit was adapted from [2, 3]. NMOS switches were implemented and optimized to run at 100MHz. Figure 2.14 shows the combination of logic and switches used to implement the sub-DAC and stage outputs. NMOS switches were used due to their reduced physical size. Combination of the clock, outputs of two differential comparators from the sub-ADC (A1 and B1) and their complimentary signals are inputs of the three 3-input NAND gates. The compliments of the sub-ADC outputs are obtained using inverters. MSB and LSB pins form one of the three allowed output binary states. These are the intermediate bits that are routed to the shift register where they are held until all the outputs off all nine stages are obtained. V_{dac}^{+} and V_{dac}^{-} are the analog outputs of the sub-DAC for a given binary output of the stage. These are inputs to the gain stage where they are subtracted from the original input signal to form the residual. The generated residual needs to be multiplied by a gain of two. The gain of two is needed to insure for the residual to remain in the proper threshold range as it propagates through the stages. Because of this, the sub-DAC outputs V_{dac}^{+} and V_{dac}^{-} are $-V_R$, 0 and $+V_R$ instead of $\frac{-V_R}{2}$, 0 and $\frac{+V_R}{2}$. The gain of two has been taken into consideration before the sub-DAC outputs are sent to the gain stage. Table 2.2 lists all the possible states of the sub-DAC output (V_{dac1} and V_{dac2}) and the corresponding outputs of the stage (MSB and LSB). The NMOS switching network that will generate the analog outputs have been optimized to meet the 100MHz clock requirement.

$A1$	$A2$	$B1$	$B2$	ϕ_2	MSB	LSB	V_{dac1}	V_{dac2}
0	1	0	1	1	0	0	V_{REF}^{-}	V_{REF}^{+}
0	1	1	0	1	0	1	V_{dac2}	V_{dac1}
1	0	1	0	1	1	0	V_{REF}^{+}	V_{REF}^{-}

Table 2.2: Truth table for the stage and corresponding sub-DAC outputs

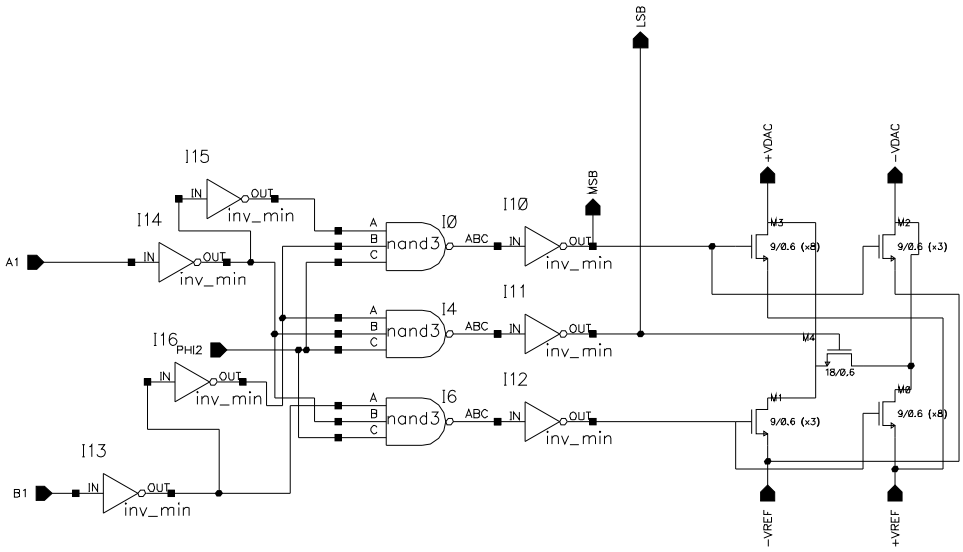

Figure 2.14: Sub-DAC circuit schematic.

2.3.2 Sub-DAC Simulation Results

Sub-DAC was simulated using the same test circuit and test conditions as for sub-ADC. Refer to Figure 2.12 for test circuit and subsection 2.2.2 for test conditions. The only addition was the circuit from Figure 2.14. Outputs of the two differential comparators (A and B) were connected as the inputs to the sub-DAC circuit in Figure 2.14, where A1 is connected to A and B1 to B.

Figure 2.15 shows a plot of sub-DAC inputs, analog outputs, digital outputs and ϕ_2 which show when the outputs are valid. Comparing Table 2.2 to results in Figure 2.15 it can be seen that the sub-DAC functions properly at a clock speed of 100MHz. In Table 2.2 V_{dac1} and V_{dac2} correspond to V_{dac}^{+} and V_{dac}^{-} in Figure 2.15, respectively. For example: for A1, B1 and ϕ_2 high, from Table 2.2 we can find that sub-DAC differential output will be V_{REF}^{+}-V_{REF}^{-} and corresponding digital word is 10. Figure 2.15 shows the same outcome.

2.4 Gain Stage

The final block of each stage is a gain stage. The function of the gain stage is to obtain the residue by subtracting the sub-DAC output from the original input and route it to the next stage. This block contains a S/H circuit, an OTA, integrating capacitors and switches. The OTA was designed by a fellow undergraduate student Erik McCarthy. For more on OTA design and simulation results refer to [6]. The S/H circuit was adapted from [3] and resized to meet current 100MHz frequency specifications.

2.4.1 Gain Stage Design

Figure 2.16 shows the gain stage circuit design. As mentioned before, the pipeline stages are divided into Even and Odd stages. For an odd stage, ϕ_1 is used to sample and quantize the input signal and during ϕ_2 the residual is generated by the gain stage and passed to the next (Even) stage. In figure 2.16 during ϕ_1 the 500fF capacitors are charged to the values of the differential input signals. During this time the differential outputs of the OTA are tided to common mode, VCM. Once ϕ_2 is active the residual is created by subtracting the sub-DAC output from the input signal and this difference is sent to the next stage. In order to transfer charge onto the 500fF capacitors during ϕ_1 and ϕ_2, the size of transistors M4, M5, M6,

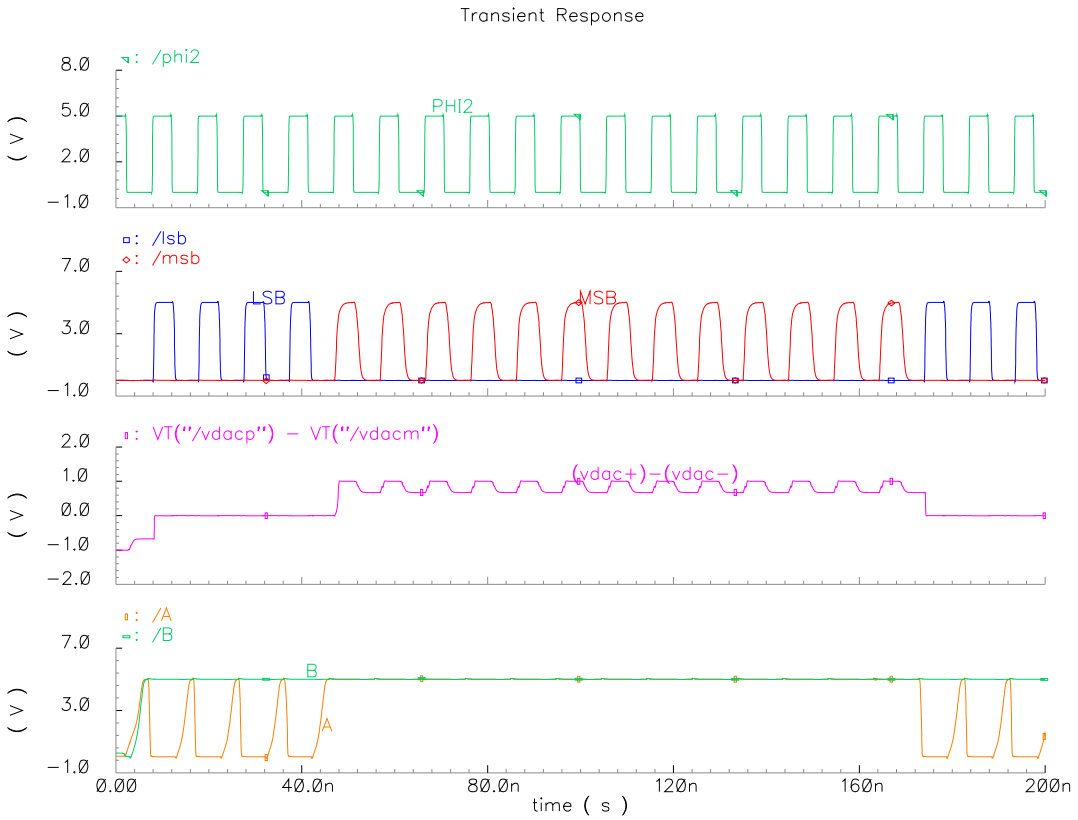

Figure 2.15: Sub-DAC performance at 100MHz.

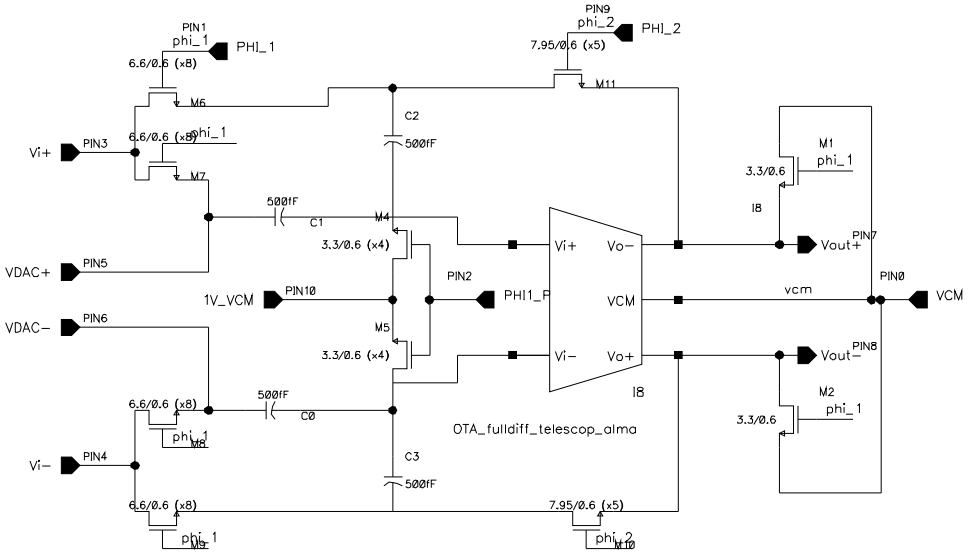

Figure 2.16: Gain Stage Circuit.

M7, M8 and M9 had to be increased from the original design. Transistors M4 and M5 were increased to $3.3/0.6$(x4) microns and transistors M6, M7, M8 and M9 were increased to $6.6/0.6$(x8) microns. This was found to be necessary for 100MHz operation. The performance of the gain stage can be found in Chapter 3, where the entire pipeline stage is put together and simulated.

2.5 Last Stage

Last stage in the pipeline differs from the other stages because it does not contain the gain stage. There is no residual to be passed on to the next stage. Instead, the last stage provides a full 2-bit conversion for possible outputs of 00, 01, 10 and 11. The last stage compares the input to four thresholds: $\frac{-V_R}{4}$, 0, $\frac{+V_R}{4}$ and $\frac{+V_R}{2}$. The additional threshold, $\frac{+V_R}{2}$, divides the 10 range into two, providing 10 and 11 output. Figure 2.17 shows the locations of the thresholds of the last stage together with allowed digital outputs.

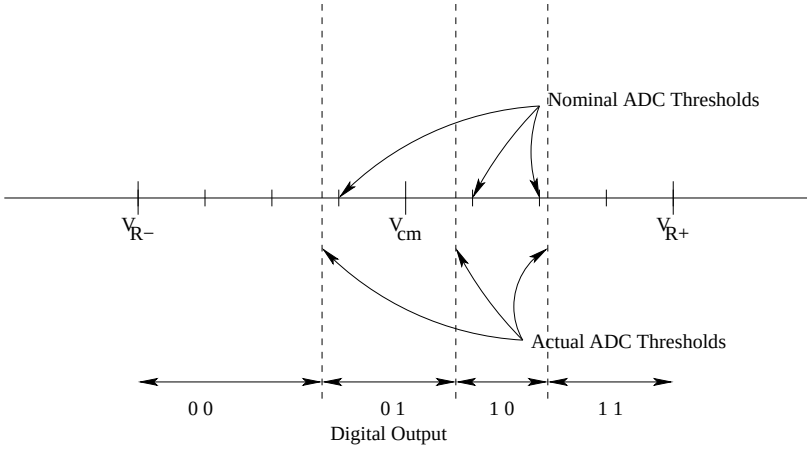

Figure 2.17: Threshold locations in the last stage.

2.5.1 Last Stage Circuit Design

The design and concept of the last stage logic was adopted from [3]. The last stage contains three differential comparators. Two of the differential comparators are the same once implemented in the sub-ADC and the third one differs only in a threshold level. As mentioned before, the last stage can have 11 for a digital output and therefore the third differential comparator has a threshold set to $\frac{+V_R}{2}$. Figure 2.18 shows the circuit schematic of the last stage. Setting the capacitor values to 100fF provided 1:2 voltage ratio as opposed to 1:4 in the other two differential comparators. Because the last stage does not have a gain stage associated with it, the sub-DAC is redesigned to provide only a 2-bit digital output. Figure 2.19 shows the logic circuit needed to calculate the correct digital output. Inputs A, B and C are the outputs of the three differential comparators, where C is the output of the comparator with a $\frac{+V_R}{2}$ threshold. The truth table for the logic in Figure 2.19 is given in a Table 2.3. The two inverters in the path of A1 provide a propagation delay to insure the outputs (LSB and MSB) are ready at the same time. The truth table and logic circuit are adopted from [3].

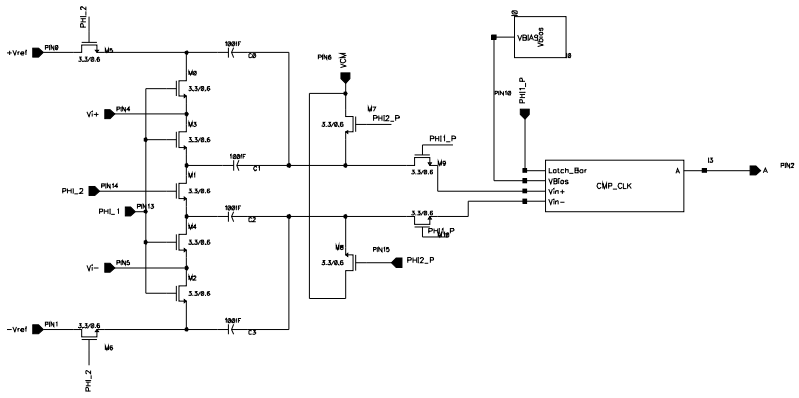

Figure 2.18: Schematics of the last stage.

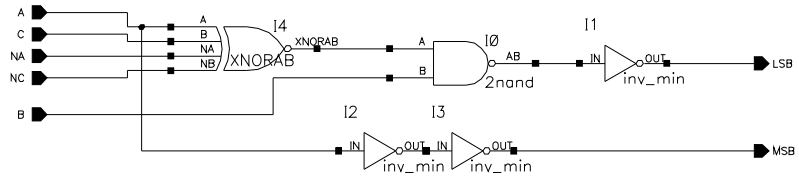

Figure 2.19: Schematics of the last stage logic.

$A1$	$A2$	$B1$	$C1$	$C2$	ϕ_2	MSB	LSB
0	1	0	0	1	1	0	0
0	1	1	0	1	1	0	1
1	0	1	0	1	1	1	0
1	0	1	1	0	1	1	1

Table 2.3: Truth table for the last stage logic.

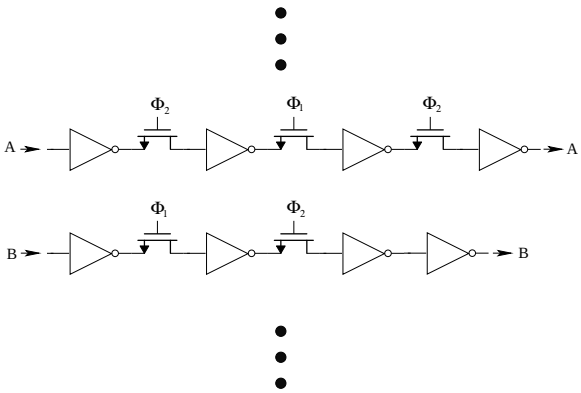

Figure 2.20: Shift register design.

2.6 Shift Register

In the current design the intermediate bits of each stage are not digitally corrected for a 10-bit output. Instead, the converter outputs are the intermediate bits. For a 10-bit pipeline converter there will be 18 output lines. For a valid output to be available, all stages must have quantized the input sample. In a pipeline architecture the outputs of the first $n-2$ stages must be stored in memory until the last stage ($n-1$ stage) has quantized the sample, where n is the $n-bit$ converter. This memory function is implemented using a shift register. The design of a shift register is adopted from [8]. The shift register consists of minimum sized inverters connected with NMOS switches. The basic structure of the shift register is shown in Figure 2.20. In the current design there are 9 stages and all odd stages have outputs available on ϕ_2 and all even stages on ϕ_1. In Figure 2.20 it can be seen that two clock phases are used. On every clock phase, stage outputs are stored and shifted in memory. Also, every other stage will need an extra inverter at the end in order to restore the original input signal. In Figure 2.20, the outputs are available when ϕ_2 is high. Also, it can be seen that output B will be available a clock phase after A. For example: if stage 1 output is valid during ϕ_2, stage 2 output will be valid during ϕ_1, stage 3 output will be valid during the next high of ϕ_2 and so on. Complete schematics of the shift register used to implement 9 stages can be found in the Appendix A.

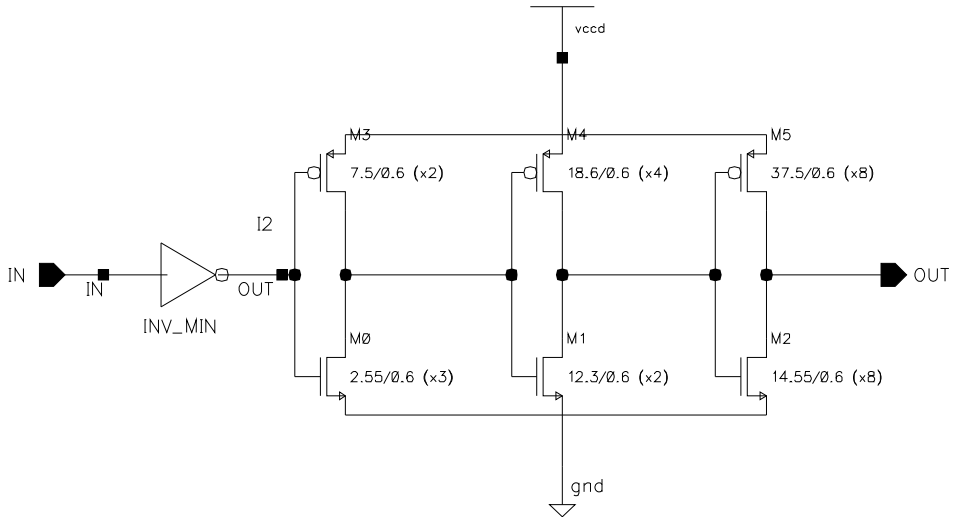

Figure 2.21: Schematics of the output buffer.

2.7 Output Buffers

The digital output pins of the converter are buffered to comfortably drive a 10pF load at 100MHz. The outputs of the ADC will be collected with the logic analyzer and a 10pF load represents the package and logic analyzer. Originally, the output buffers were supposed to drive 20pF load at 100MHz. This load was based on the capacitance of the oscilloscope probe. If used, oscilloscope probe will be in a direct contact with the converter outputs. On the other hand, there will be resistor packs and latches located between logic analyzer and converter outputs. Refer to Chapter 6 for test configuration of the packaged chip. The number of buffers needed (19) and their physical size would not fit inside the chip together with nine stages, clock and shift register. Due to the limited size of the chip, constraints had to be put on buffers. The digital buffers had to fit inside the output pad and the available space inside the output pad was limiting the physical size of the buffer and therefore the load of the buffer at 100MHz. At the same time the ADC tests do not rely on the use of the oscilloscope and therefore this reduction in the load will not effect the ADC performance. The design methodology for the output buffer was adopted from [9]. Four inverter stages were used in the buffer design. They were sized using the design concept from [9]. The final design together with the inverter sizings is shown in Figure 2.21.

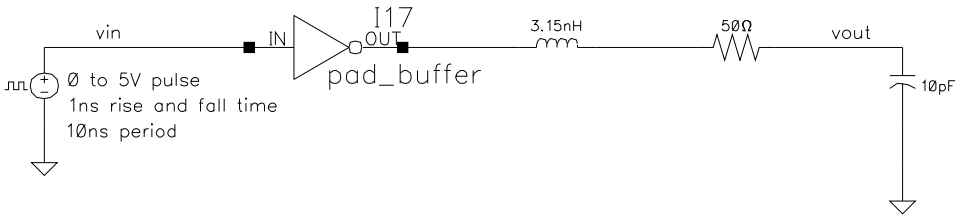

Figure 2.22: Test circuit for the output buffer.

2.7.1 Output Buffer Simulation Results

Figure 2.22 shows a simulation circuit for output buffers. Presents of the inductor and the resistor in a simulation circuit accounts for the package model used. They are provided by MOSIS and they simulate pins used for the digital outputs of the converter. Figure 2.23 shows the simulation results for the output buffer used in the current design. A test was done using a 100MHz square wave with the amplitude of 5V. The output load was set to 10pF. According to the results, output buffer are capable of driving a 10pF load at 100MHz. Figure 2.24 shows if the speed was slowed down to 50MHz, buffers would comfortably drive a 20pF load if necessary.

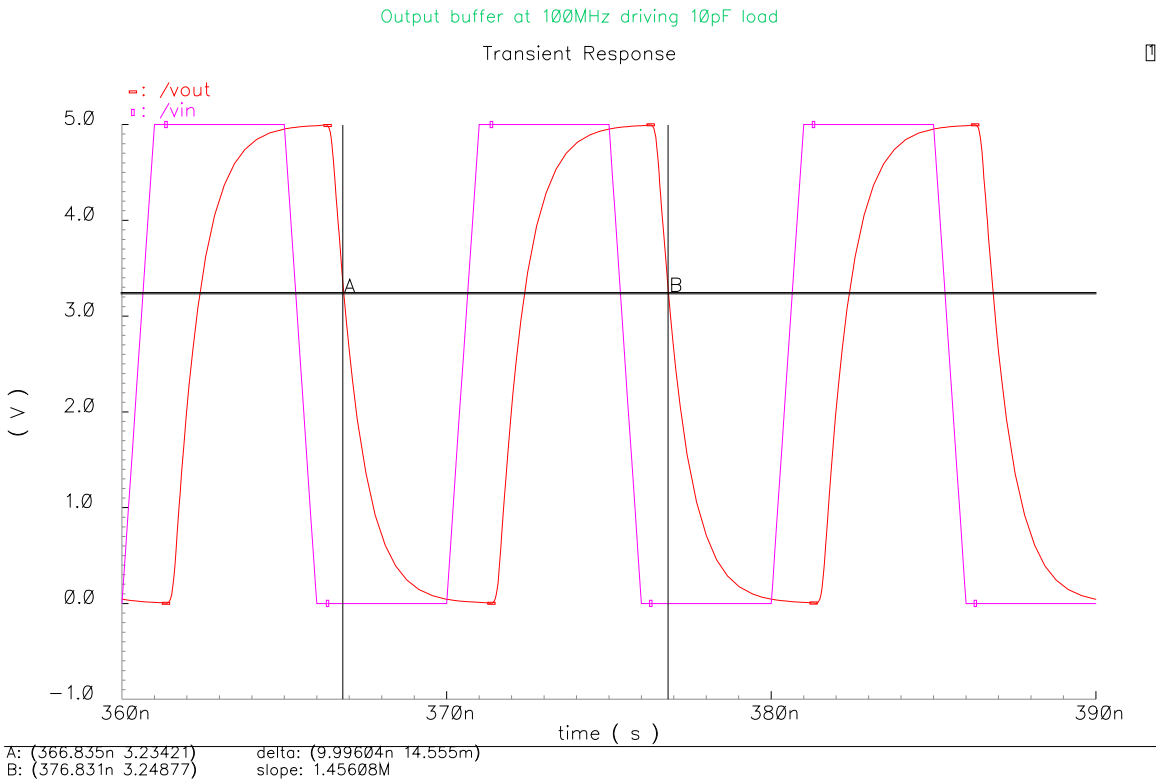

Figure 2.23: Simulation results for the output buffer at 100MHz and 10pF load .

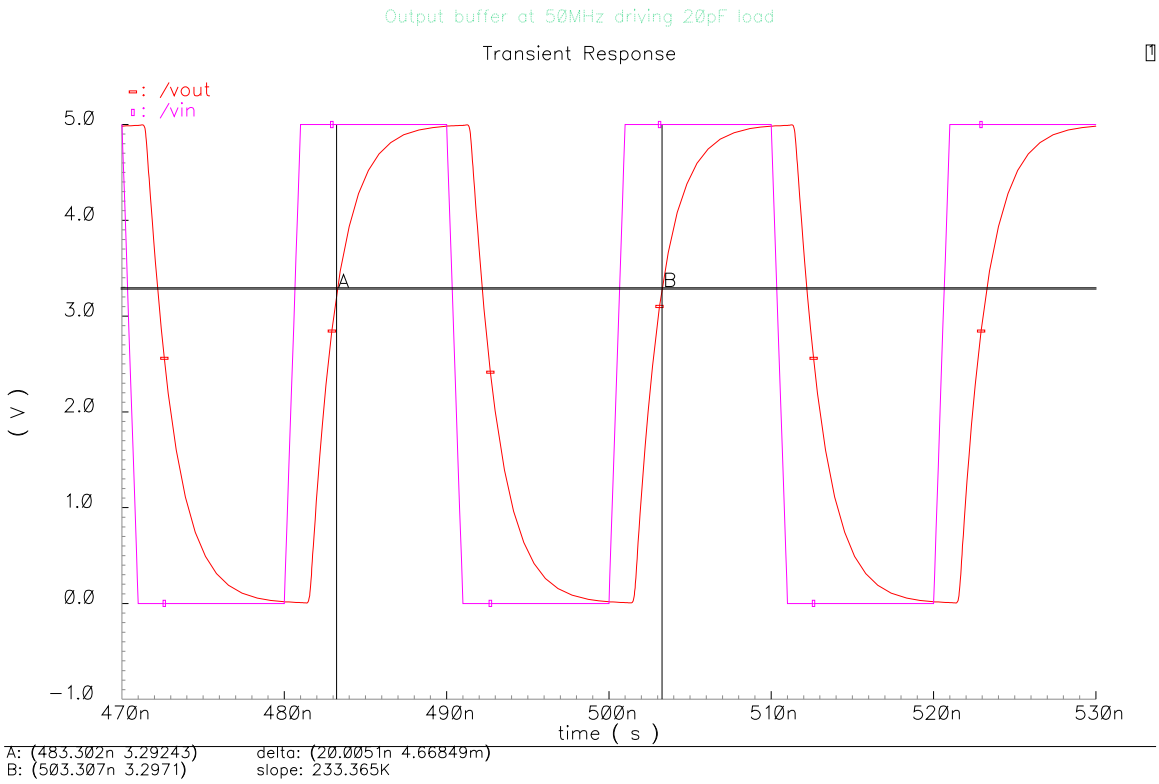

Figure 2.24: Simulation results for the output buffer at 50MHz and 20pF load.

Chapter 3

Circuit Performance

Chapter 2 discussed the design and performance of the individual building blocks of a pipeline stage. This chapter will analyze the performance of the pipeline converter when all nine pipeline stages are cascaded to obtain a desired resolution converter. All simulations in this chapter were run on the schematics level. Simulations including parasitic capacitances can be found in Chapter 5. It will be seen that once the pipeline stages are cascaded to obtain a higher resolution converter, performance degrades at 100MHz.

3.1 5-Stage Pipeline Converter

Five stages were cascaded to obtain a 6-bit converter. Refer to figure 3.1 for the circuit configuration and simulation conditions. The simulation was designed to show that each stage is capable of obtaining the desired stage output for a given input, where input of the next stage is the output of the previous stage. Two tests were conducted. For both tests the differential input signals were set to a square wave with 200ns period and differential input of +/- 0.8V. $VREF^{+}$, $VREF^{-}$ and VCM were set to 3V, 2V and 2.5V respectively. The difference between the two test was the clock frequency. Table 3.1 shows the expected outputs of the first five stages for a given input of +/- 0.8V. V_{diff} corresponds to differential input signal and sub-DAC output was found using $2 * (V_{diff} - V_{DACth})$, where V_{DACth} is sub-DAC threshold. For sub-DAC thresholds refer to Chapter 2.

Figure 3.2 shows inputs and outputs of the first five stages when the clock frequency was set to 100MHz. It can be seen that for the first 100ns the outputs agree with the values in table 3.1. However, once the differential input switches

V_{diff}	$Intermediatebits$	$DACoutput$
0.8	10	0.6
0.6	10	0.2
0.2	10	-0.6
	01	0.4
-0.6	00	-0.2
0.4	10	-0.2
-0.2	01	-0.4
	00	-0.6
-0.8	00	-0.6
-0.6	00	-0.2
-0.2	00	0.6
	01	-0.4
0.6	10	0.2
-0.4	00	0.2
0.2	10	-0.6
	01	0.4

Table 3.1: Outputs for the first 5-stages of a pipeline converter.

the state from +0.8 to -0.8 the outputs become indecisive and eventually wrong. This problem occurs at the comparator level. Due to the time constraint for this project, the problem was fixed by slowing down converter to 50MHz. Figure 3.3 shows inputs and outputs for the first five stages where the clock frequency was set to 51.2MHz. Frequency of 51.2MHz is used because it corresponds to a test frequency of 800KHz for 64 samples. Frequency of 51.2MHz is close to 50MHz and it gives a nice round number for the input frequency. Odd multiples of 800KHz will give coherent test frequencies. The coherent test frequency is found using the $Fin = Fs * (k/N)$, where Fin is a test frequency, Fs is a sampling frequency, N is a number of samples used and k is a bin number. Therefore, test frequency of 800KHz corresponds to a bin number k = 1. It can be seen the output results do agree with the values in table 3.1.

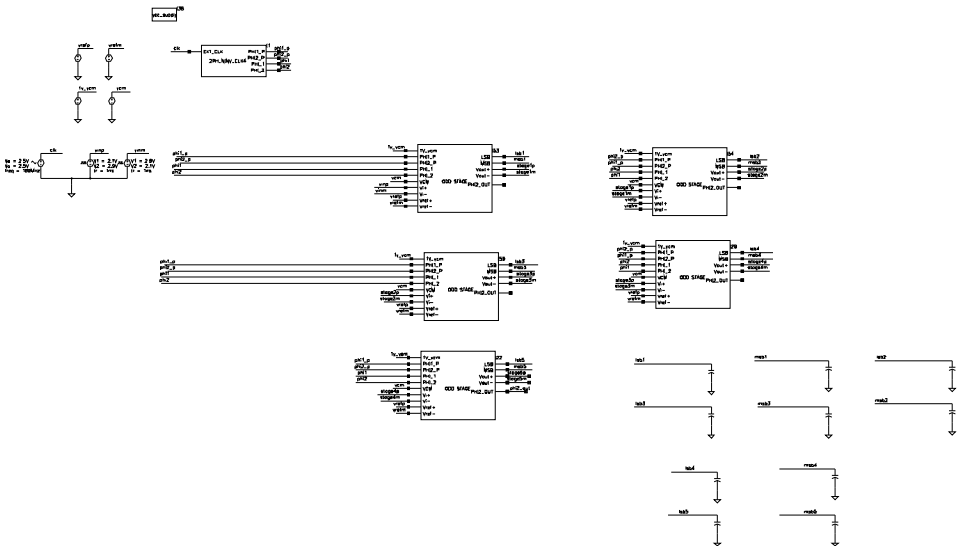

Figure 3.1: Circuit configuration for cascading 5-stages.

3.2 Pipeline Simulation

After deciding to drop the sampling frequency down to 50MHz due to the comparator limitations, the next step was to assemble and test 9-stage pipeline ADC. The content of the entire pipeline can be found in Appendix A. All simulations were conducted using a Cadence simulation toolbox and afterwords data was collected and imported into the MATLAB for further processing and analyzing. Because most tests on a top schematic level take at least 5 hours to run, it was decided to collect only 64 samples from the converter. Running at a 51.2MHz clock frequency, 64 samples corresponds to an 800KHz sine wave. To take into account the inherent pipeline delay the simulation was run for 2.5μs which corresponds to two periods of a 800KHz sine wave. Each simulation on the schematics level took approximately 5 hours to run plus at least 3 hours to load and process the data in the MATLAB.

3.2.1 Linearity of a Pipeline ADC

The first test conducted on a schematics level was a linearity test. A constant differential input ranging from -1V to +1V was applied to the converter and outputs were compared to the ideal characteristics of a 10-bit ADC. Test conditions for a

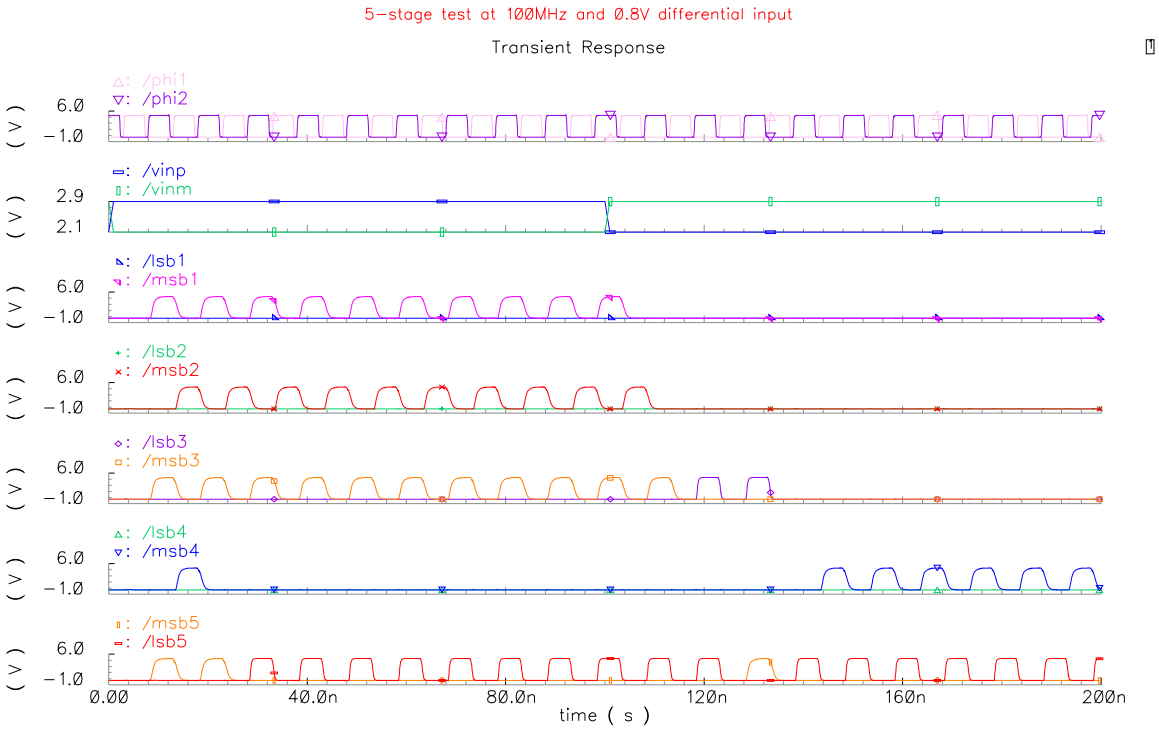

Figure 3.2: 5-stage output for 0.8V differential input at 100MHz.

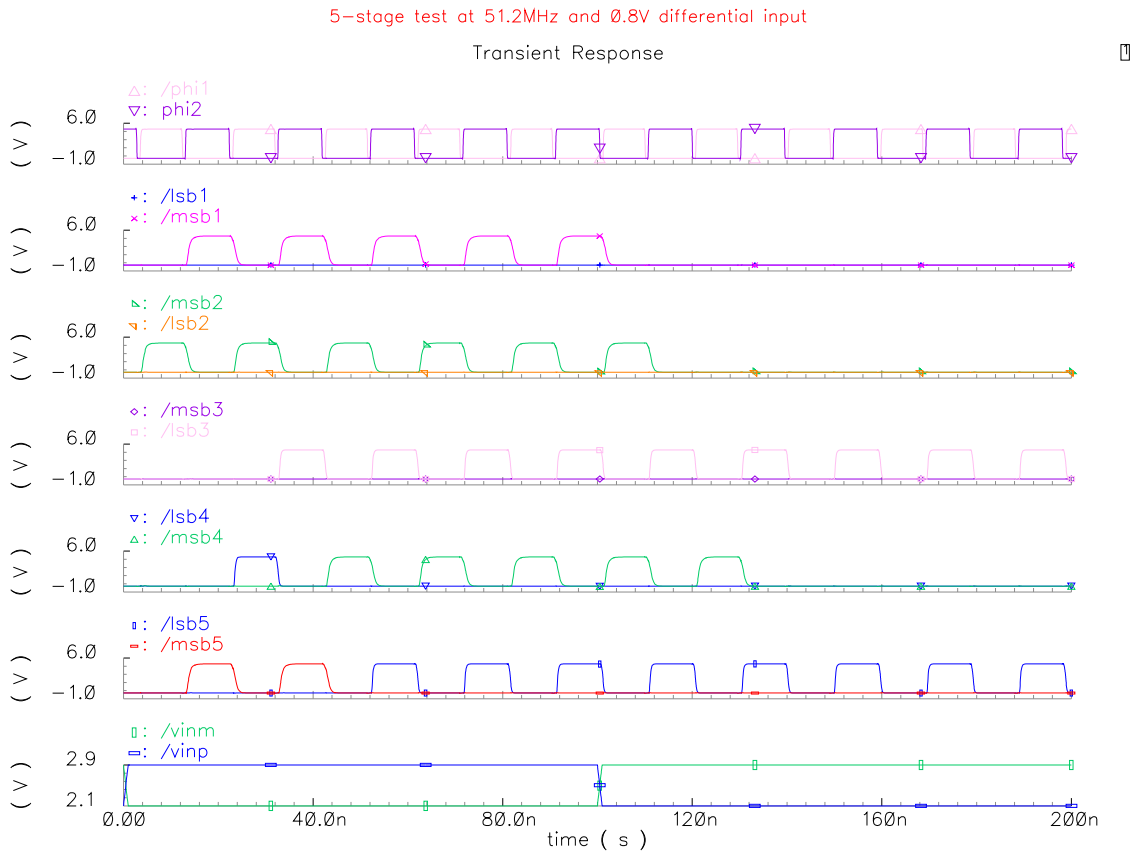

Figure 3.3: 5-stage output for 0.8V differential input at 51.2MHz.

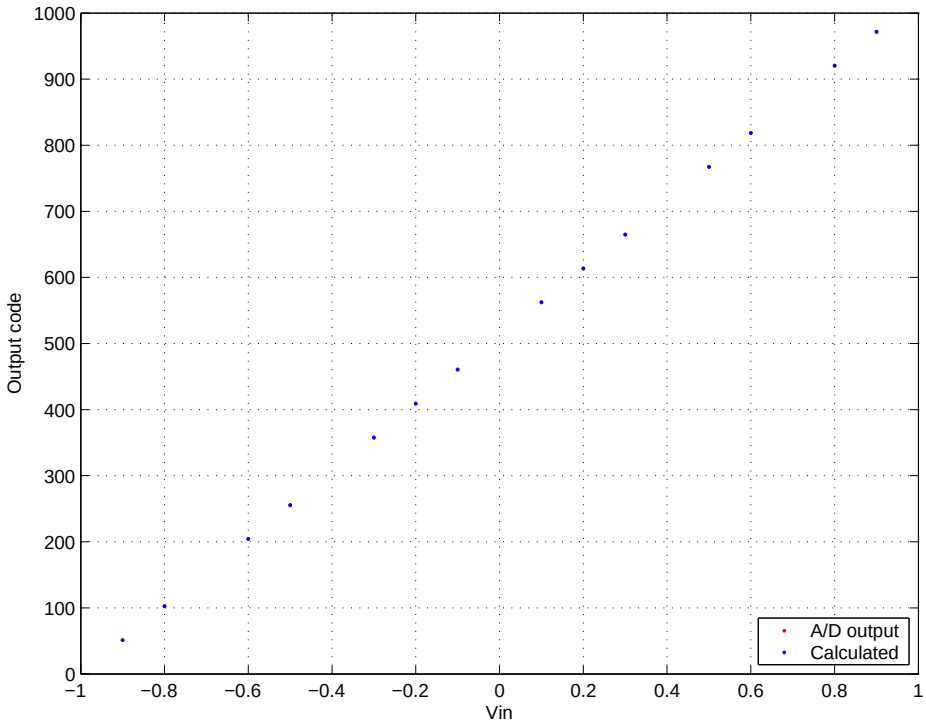

Figure 3.4: Linearity of a 10-bit Pipeline ADC at 51.2MHz - schematics level simulation.

linearity test were: Fs = 51.2MHz, V_{ref}^{+} = 3V, V_{ref}^{-} = 2V, VCM = 2.5V, VCM_{OTA} = 1V. Vin^{+} and Vin^{-} was changed to obtain the differential input ranging from -1V to +1V. Figure 3.4 shows the linearity test results. It can be seen that the 10-bit converter is showing the characteristics of the ideal converter.

3.2.2 Low Test Frequency (bin 1)

The performance of the ADC on a schematic level was analyzed using three different test frequencies: test frequency, Nyquist frequency and high frequency. The frequency test is designed to determine the accuracy of the converter when a slow changing input is applied. This slow changing dynamic test will allow us to see if there are more problems introduced by the differential comparators or even timing problems due to cascading the 9-stages together. The test conditions for all three test frequencies are: Fs = 51.2MHz (sine wave, 0-5V), V_{ref}^{+} = 3V, V_{ref}^{-} =

2V, VCM = 2.5V, VCM_{OTA} = 1V. Vin^+ was a sinusoid with amplitude Ain = 450mV (-1dBFS) and low test frequency was set to 800KHz. Vin^- = Vin^+ with 180° phase shift. It should also be mentioned that in this and later simulations the package pins were modeled and two separate supply voltages were used (VDD and VCCD). VCCD was a supply for the output buffers which were incorporated inside the pad set and VDD was a supply for all nine stages and shift register. Refer to Appendix A for the configuration of the two supplies used and electrical characteristics of the package pins that were modeled. Also, the package pins for the external clock and signal inputs were modeled. Depending on the pins used the particular RLC network was configured according to package handbook provided by MOSIS. Additional information on the pin assignment is described in Chapter 4.

Figures 3.5, 3.6 and 3.7 show the performance of the low frequency test. The spurious free dynamic range of the converter (SFDR), effective number of bits (ENOB) and error characteristic for the particular test frequency can be seen in the above mentioned figures. For this simulation, ENOB was 9.35 bits and SFDR was 63.5dB. The output error for the converter should be within +/-1LSB and from Figure 3.7 one can see that this is accomplished.

3.2.3 Nyquist Test Frequency (bin 31)

The Nyquist frequency test is designed to provide maximum switching throughout the pipeline. It will allow us to test S/H accuracy. For this test the input signal was still a sinusoid with amplitude Ain = 450mV (-1dBFS) and test frequency, Fin = 24.8MHz. Vin^- = Vin^+ with 180° phase shift. Figures 3.8, 3.9 and 3.10 show the performance of the converter at the Nyquist frequency. There is a small degradation in the performance which is to be expected once the maximum switching throughout the pipeline is applied. The test showed that S/H circuitry and the rest of the converter components are optimized enough to run accurately at 51.2MHz with a fast changing dynamic input. As mentioned before these tests were conducted on a schematics level and results are expected to degrade once the simulation is done with parasitics incorporated. More on physical design and simulation results can be found in Chapter 4. At the Nyquist frequency the power consumption of the converter was also tested. The converter was found to consume 191mW of power. Running from a 5V supply this corresponds to a current draw close to 40mA.

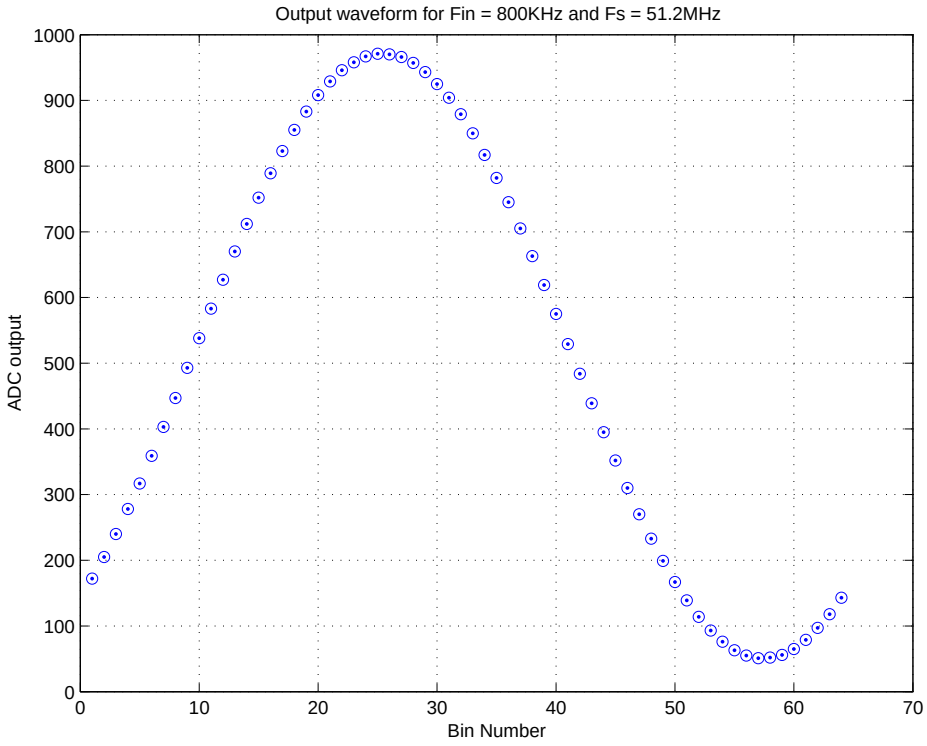

Figure 3.5: Output waveform for a test frequency in bin 1 (800KHz).

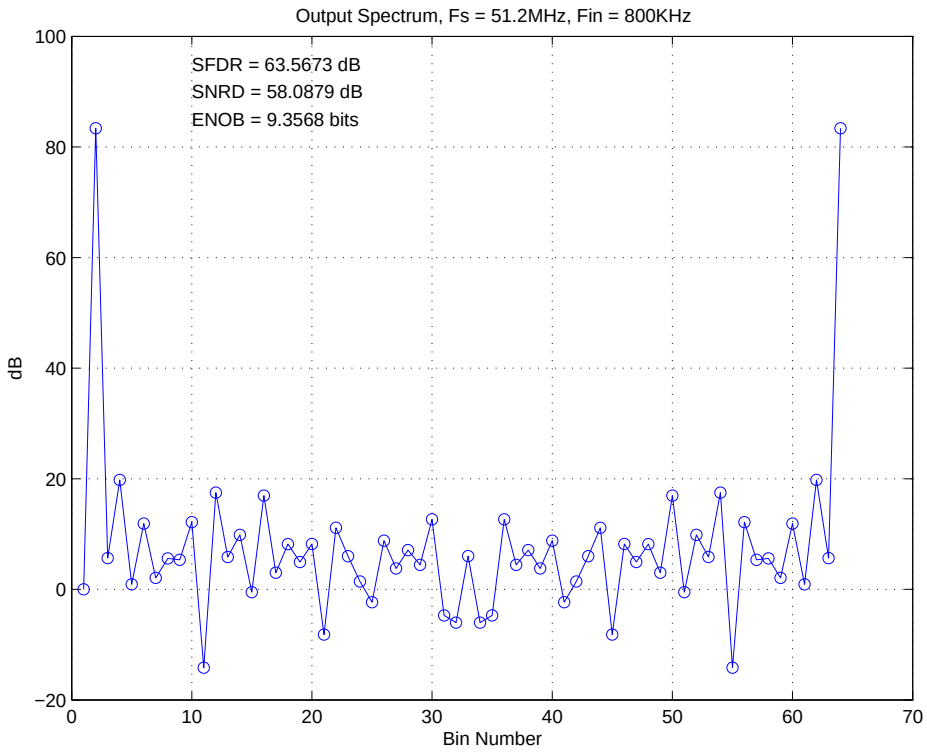

Figure 3.6: Performance of the ADC at low test frequency - schematics level.

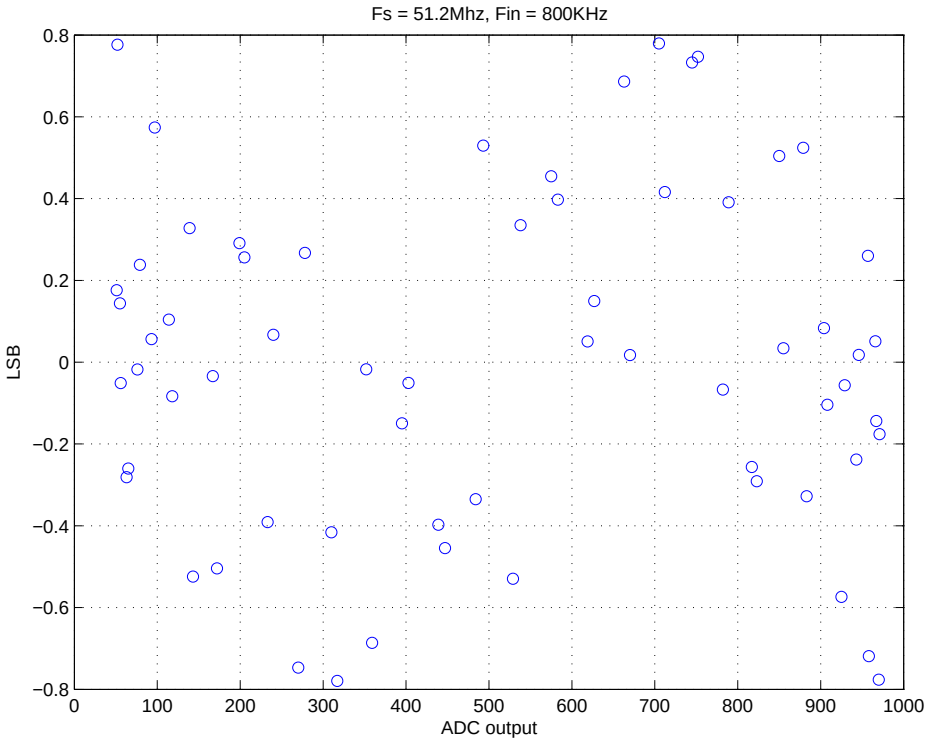

Figure 3.7: Output error including all harmonics except DC and test signal, Fin = 800KHz.

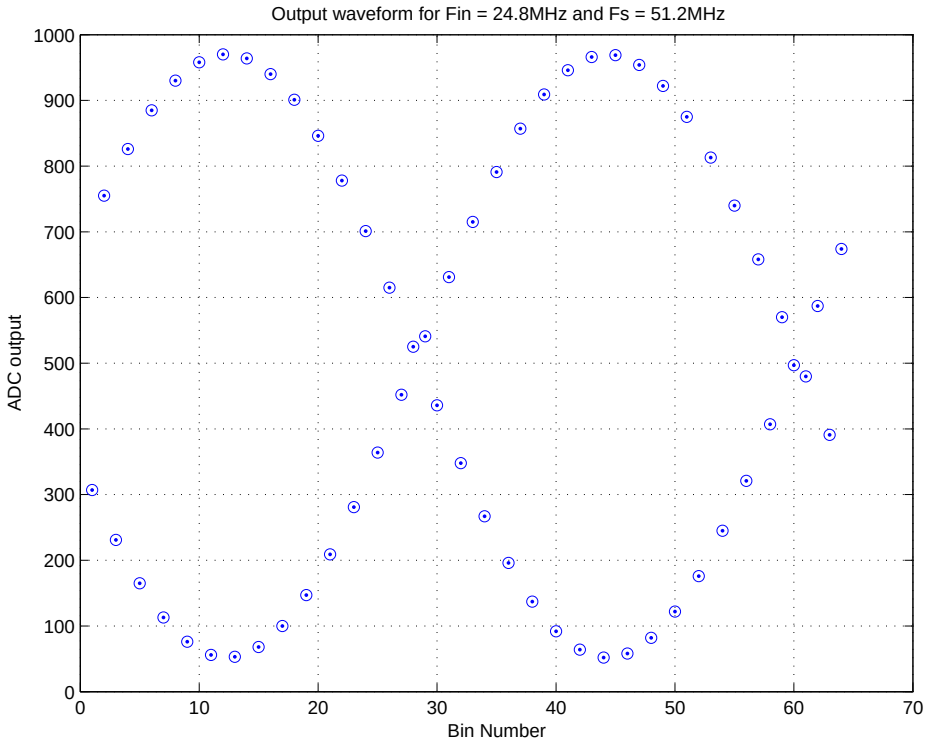

Figure 3.8: Output waveform for a test frequency in bin 31 (Nyquist frequency).

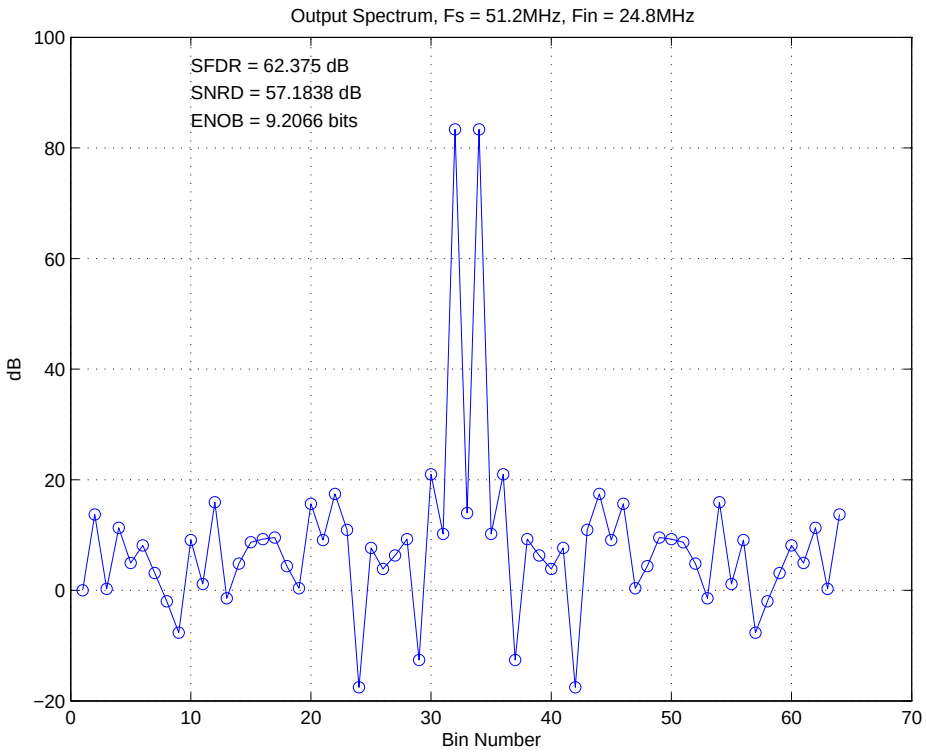

Figure 3.9: Performance of the ADC at the Nyquist test frequency - schematics level simulation.

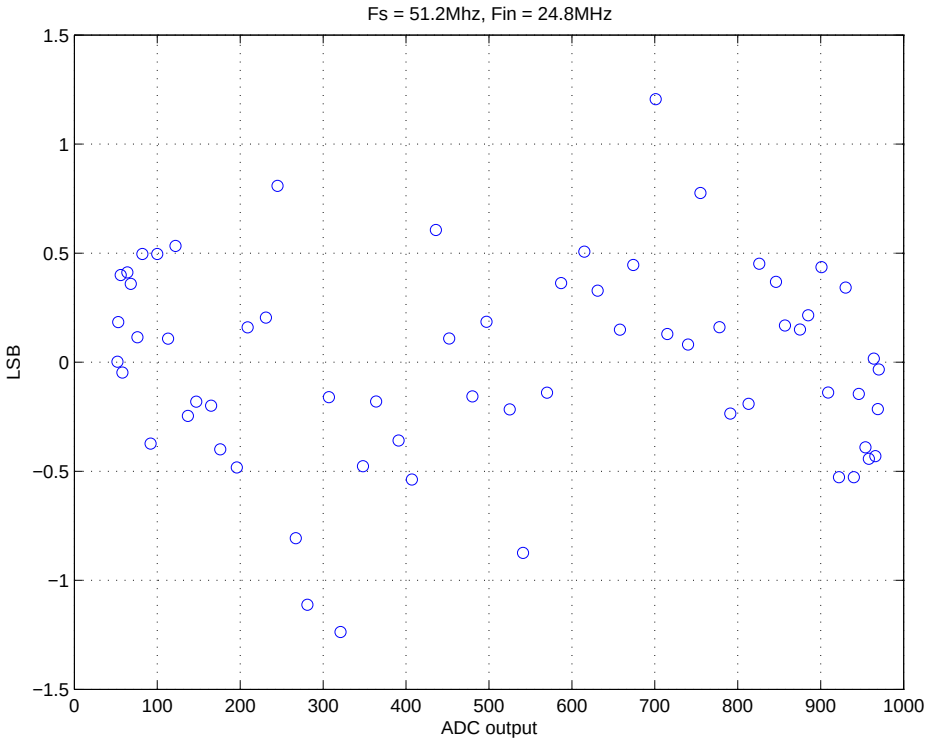

Figure 3.10: Output error including all harmonics except DC and test signal, Fin = 24.8MHz.

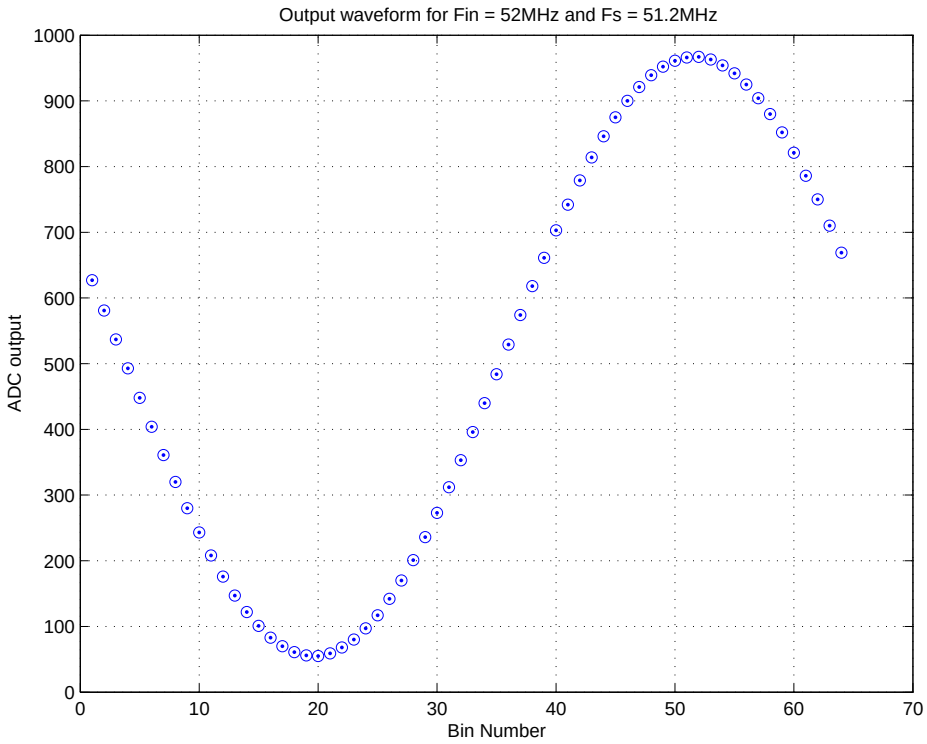

Figure 3.11: Output waveform for a test frequency in bin 65.

3.2.4 High Test Frequency (bin 65)

The high test frequency helps to analyze the input bandwidth of the converter as well as S/H accuracy because the signal is changing as fast as the clock. The input signal was still a sinusoid with amplitude Ain = 450mV (-1dBFS) and test frequency, Fin = 52MHz. Vin^- = Vin^+ with $180°$ phase shift. Figures 3.11, 3.12 and 3.13 show the performance of the converter at the high test frequency. There seems to be no input bandwidth limitation and the results are comparable to the low test frequency simulations. Again this shows that on the schematics level circuits were optimized to run and perform well at 50MHz. There seems to be no visible problems due to timing or comparator problems which have been an issue at 100MHz.

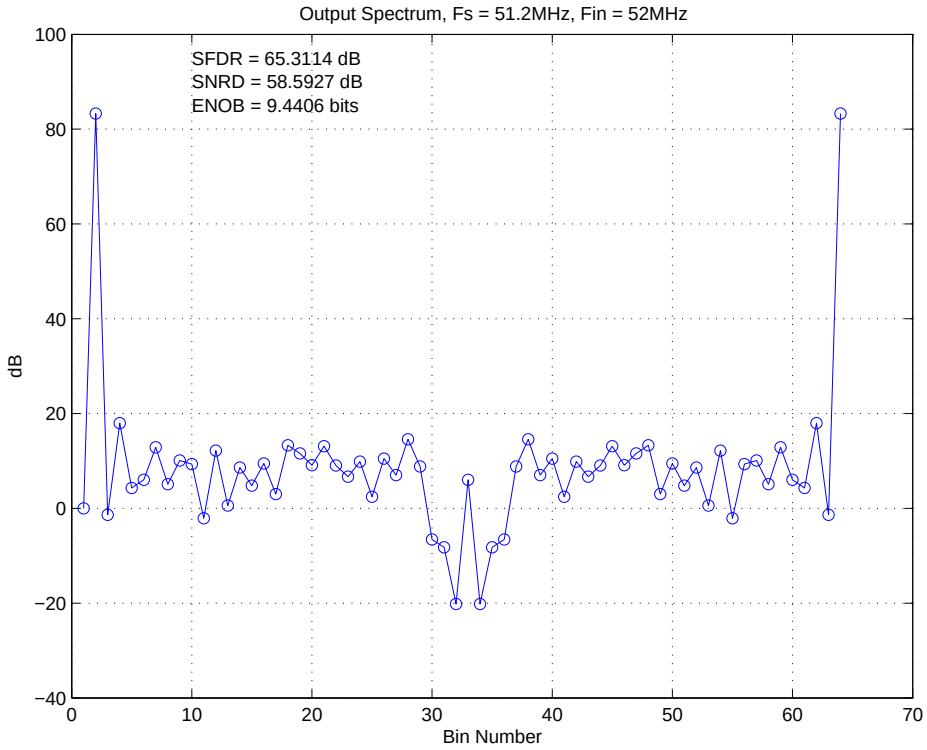

Figure 3.12: Performance of the ADC at the high test frequency - schematics level simulation.

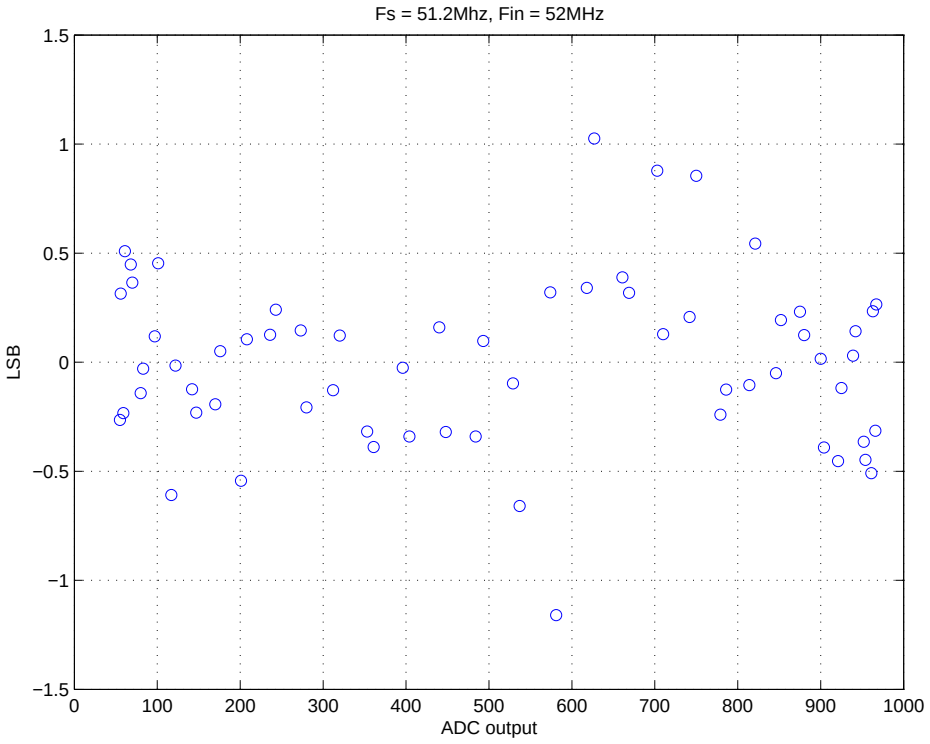

Figure 3.13: Output error including all harmonics except DC and test signal, Fin = 52MHz.

3.2.5 Discussion of Simulation Results

All the tests discussed above were simulated at the room temperature ($27°C$). Simulation results meet the design goals where the effective number of bits is above 9 and the dynamic range is greater than 60dB. As mentioned before the performance is expected to decrease with temperature and parasitics added. Simulations at different temperatures were not conducted do to the time constraints and simulation results with parasitics added are discussed in Chapter 5.

Chapter 4

Physical Design

This chapter discusses the pin assignment, constraints and considerations taken into account while doing a layout and floor planning of the final chip.

4.1 Pin Assignment

The die size that was available for the current design was 1.5 X 1.5 mm and it was packaged in a 40 pin DIP. The physical design of the final chip and floor planning of the die can be found in Appendix B. Depending on the location some pins have higher parasitic impedance than others which has a negative affect on the signal transmission. Pins were assigned based on the sensitivity of the ADCs signals and electrical characteristic of the package used. Table 4.1 contains the electrical characteristics of the 40 pin DIP. For the pin assignment refer to Table 1.3 in Chapter 1. Pins with the lowest parasitic impedance were used for the critical signals, such as input signals and clock, in order to minimize the noise that may be introduced by the pin trace. Also multiple pins were used for the two supply voltages, VDD and VCCD. VDD is a supply for all nine stages plus shift register and VCCD is a supply for the output buffers. Having the output buffers on a separate supply reduces the noise introduces within each stage which helps the functionality of the analog components within the stage. Five pins were used for the VDD supply, two pins were used for the VCCD supply and seven pins were used for ground (GND) in order to reduce the parasitic impedance of the pins as much as possible.

PIN	R(Ω)	L(nH)	C(pF)	t_{of}(ps)
1,20,21,40	0.217	8.18	5.32	209
2,19,22,39	0.177	7.92	4.39	187
3,18,23,38	0.154	7.34	3.37	157
4,17,24,37	0.110	6.48	2.34	123
5,16,25,36	0.103	5.69	2.16	111
6,15,26,35	0.0661	4.37	1.43	79
7,14,27,34	0.0646	4.54	1.48	81.9
8,13,28,33	0.0498	3.69	1.05	62.3
9,12,29,32	0.0378	3.54	0.863	55.3
10,11,30,31	0.0247	3.15	0.660	45.6

Table 4.1: Electrical characteristics of the 40 pin DIP.

4.2 Floor Planning

The general idea for the floor planning was adapted from [3]. What was taken into consideration was the symmetry when distributing input signals and clock to each stage. By having a symmetric signal distribution the introduction of the extra delays is avoided. Figure 4.1 shows the floor planning and signal distribution for the current design. The clock is centered between the stages to allow for the equal delay introduced to each stage. Also to avoid degradation of the clock signal, each stage contains a 100fF buffer to buffer a clock signal before being used within the stage. The input signals are distributed from the top in a symmetric manner. For the signal distribution to each stage, *metal 1* and *metal 2* were used. Different metal layer have different resistance and by using the same metal for distributing signal to stages assured the least mismatch in signal distribution on each stage.

4.3 Component Layout and Outer Guard Ring

Appendix B contains the layout of each component within the stage, odd/even stage cells and final chip layout. Because the same die size was used as in [3] the approximate dimensions of a stage were known. In order to fit nine stages within a 1.5 X 1.5 mm die size the stage had to be within 195μm x 296μm. The final width and height of the stage was 191μm x 296μm, and odd/even stage together with interconnects had dimensions of approximately 402μm x 305μm. The layout for

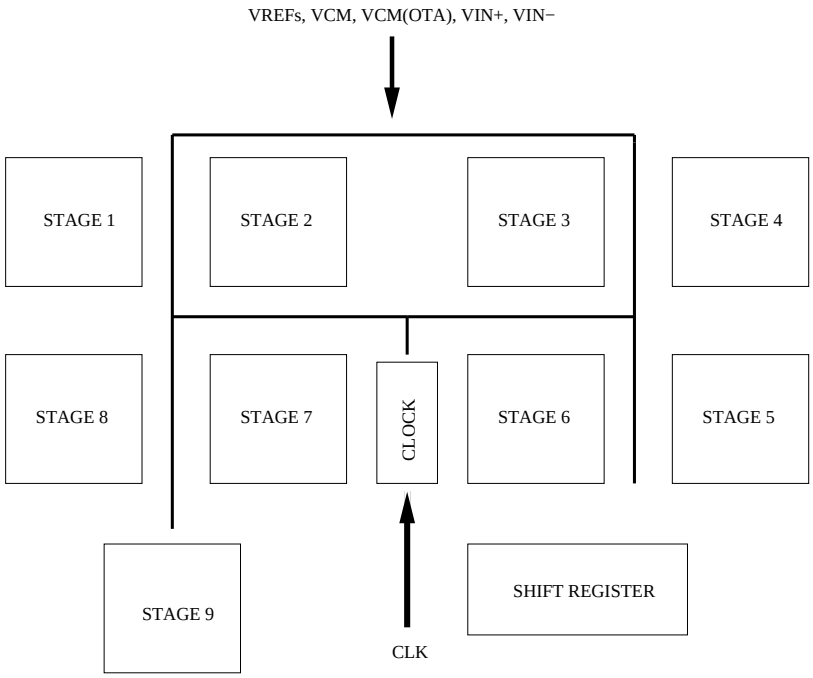

Figure 4.1: Floor planning and signal distribution within the chip.

all components share same general characteristics where the idea was to reduce the cell size, minimize the noise and introduce large number of contacts. Multipliers and fingers were used wherever appropriate to help reduce the cell size. Ground (GND) and VDD rings were implemented to minimize the noise coupling between components. To fill empty space GND and VDD taps were used to insure good GND and VDD contact. In order to provide two separate supplies, VDD and VCCD, the outer guard ring had to be broken. The ground guard ring was kept intact while the VDD guard ring was broken at pins 2 and 19. The top part of the ring was used to provide VDD supply and the bottom part of the ring is used for VCCD supply for the output buffers. Due to the space limit the output buffers had to be placed inside the pad set. The bottom half of the chip contains 19 output buffers. No test circuitry was implemented because there was not enough space on the chip and insufficient pins available. All 40 pins were utilized. Also, to satisfy the design fill rules additional poly had to be included in the final layer.

Chapter 5

Design Verification

5.1 Introduction

Verification of the physical design is accomplished with two software checks: *Design Rule Check (DRC)* verifies that the layout does not violate any manufacturing process rules and *Layout versus Schematics (LVS)* verifies that the physical layout logically matches the schematic in the number of terminals, components, component sizes and interconnections. After design and layout verification, the analog extracted schematics was created in order to verify the circuit performance with parasitics included. Analog extracted schematics were obtained from the physical layout and includes parasitic capacitances not depicted in the original schematics.

5.2 Design Rule Verification (DRC)

DRC and *LVS*, were performed on the individual components before running verification on the circuit level and finally on the top-level layout (complete chip). Top-level layout was *DRC* clean, meaning there were no errors.

5.3 Layout versus Schematics Check (LVS)

LVS verifies that the physical layout logically matches schematics. As mentioned before, *LVS* verification was performed on the individual components before running top-level layout verification. The top-level layout of the current design does pass *LVS*. Figures 5.1 and 5.2 show the *LVS* output file from Cadance.

```
Creating /usr/grads/adelic-i/ECE547/LVS/xref.out file.
Fixed device checking is enabled.
Using terminal names as correspondence points.

    Net-list summary for /usr/grads/adelic-i/ECE547/LVS/layout/netlist
       count
        1126            nets
        29              terminals
        8               res
        276             cap
        2292            pmos
        3283            nmos

    Net-list summary for /usr/grads/adelic-i/ECE547/LVS/schematic/netlist
       count
        1126            nets
        29              terminals
        8               res
        108             cap
        837             pmos
        1270            nmos


    Terminal correspondence points
          1     1VCM
          2     CLK
          3     LSB1
          4     LSB2
          5     LSB3
          6     LSB4
          7     LSB5
          8     LSB6
          9     LSB7
         10     LSB8
         11     LSB9
         12     MSB1
         13     MSB2
         14     MSB3
         15     MSB4
         16     MSB5
         17     MSB6
         18     MSB7
         19     MSB8
         20     MSB9
         21     PHI2
         22     VCM
         23     VIN+
         24     VIN-
         25     VREF+
         26     VREF-
         27     gnd!
         28     vccd!
         29     vdd!

The net-lists match.
```

Figure 5.1: LVS check for a top-level layout - Terminal correspondence.

```
The net-lists match.

                          layout  schematic
                             instances
        un-matched           0       0
        rewired              0       0
        size errors          0       0
        pruned               0       0
        active               5859    2223
        total                5859    2223

                               nets
        un-matched           0       0
        merged               0       0
        pruned               0       0
        active               1126    1126
        total                1126    1126

                             terminals
        un-matched           0       0
        matched but
        different type       0       0
        total                29      29
```

Figure 5.2: LVS check for a top-level layout cont..

5.4 Simulation Results with Parasitics Included

Circuit performance can be greatly effected by the physical design. Extracted simulation provides a more accurate representation on on what to expect from the fabricated chip. Refer to Chapter 3 for the simulation results without parasitics. Simulation of the extracted schematics with parasitic capacitances was done using a Nyquist test frequency at the room temperature and following input conditions:

- Fs = 51.2MHz (sine wave, 0-5V)
- Fin = 24.8MHz (Nyquist frequency, bin = 31)
- Ain = 450mV (-1dBFS)
- V_{ref}^{+} = 3V
- V_{ref}^{-} = 2V
- VCM = 2.5V
- VCM_{OTA} = 1V

The extracted simulation results were compared to the schematics simulation results from Chapter 3. Figures 5.3 and 5.4 show the results for the fully extracted top-level layout. Degradation of 20dB in SFDR and 10dB in SNRD can be noticed between the extracted simulation and schematics simulation. In order to trace back this degradation in the performance, the extracted simulation was run on all nine stages, clock and shift register. Metal lines providing inputs and outputs were not simulated. Figures 5.5 and 5.6 show the simulation results of this test. Degradation of 10dB in SFDR and 5dB in SNRD can be noticed between this extracted run and schematics simulation from Chapter 3. Before making a definite decision that the problem lies in the interconnect lines another extracted simulation was conducted. This time the output drivers were only extracted to insure that they are not a cause of such degradation. Figures 5.7 and 5.8 show the simulation results for this test. The output drives were found not to be the source of the problem. From the above results one can conclude that degradation in SFDR and SNRD is mostly contributed by the interconnect metal lines providing inputs and outputs, or the pad set itself once extracted is supplying noise to the input signal which in turn will significantly degrade the performance of the ADC. The Tanner pad set was provided by MOSIS.

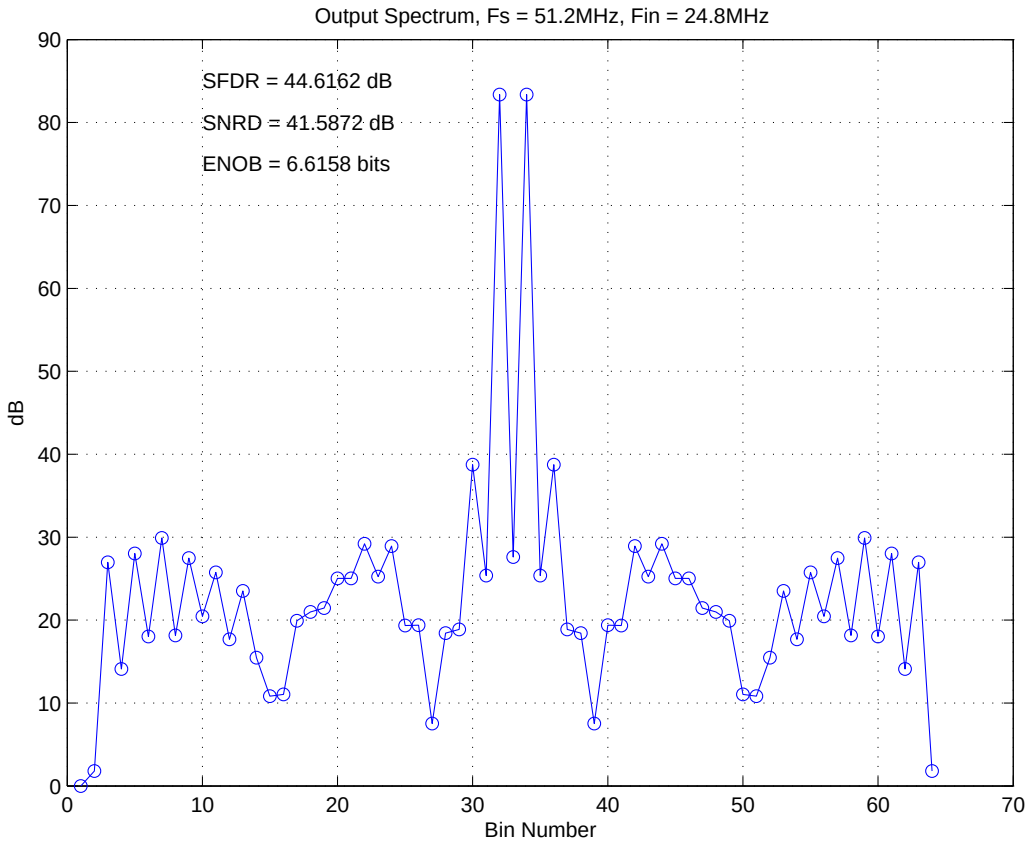

Figure 5.3: Spectrum of the fully extracted ADC at 24.8MHz.

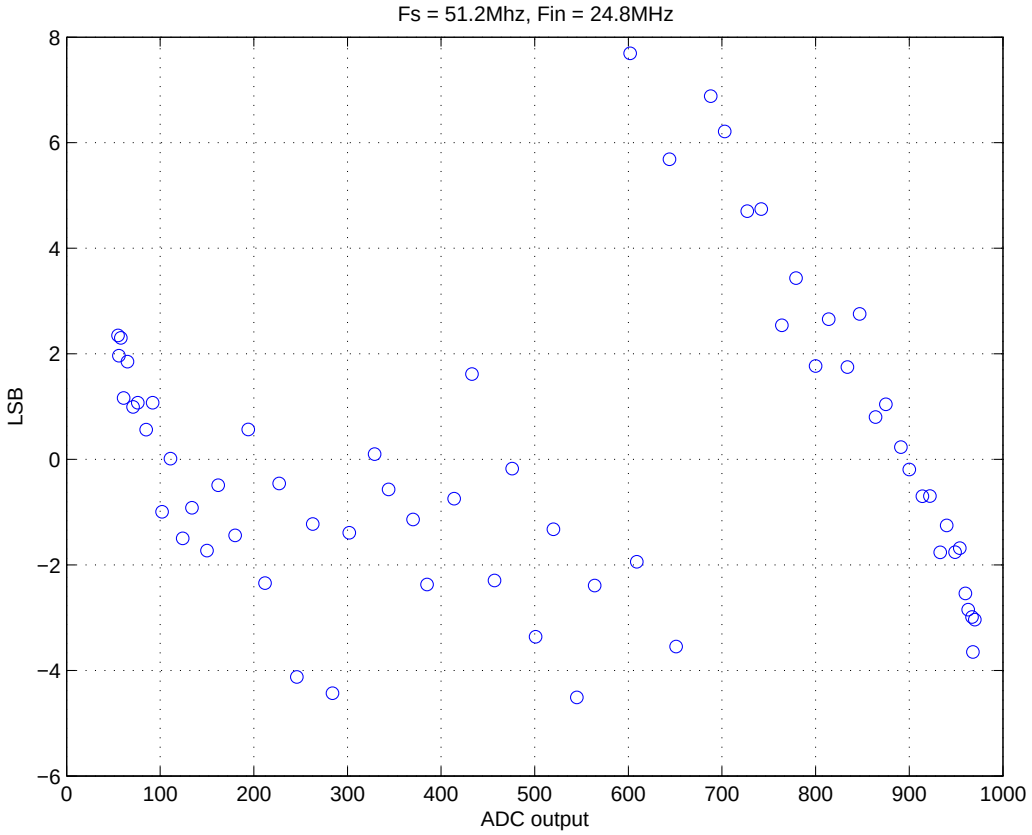

Figure 5.4: Output error including all harmonics except DC and test signal for fully extracted ADC at 24.8MHz.

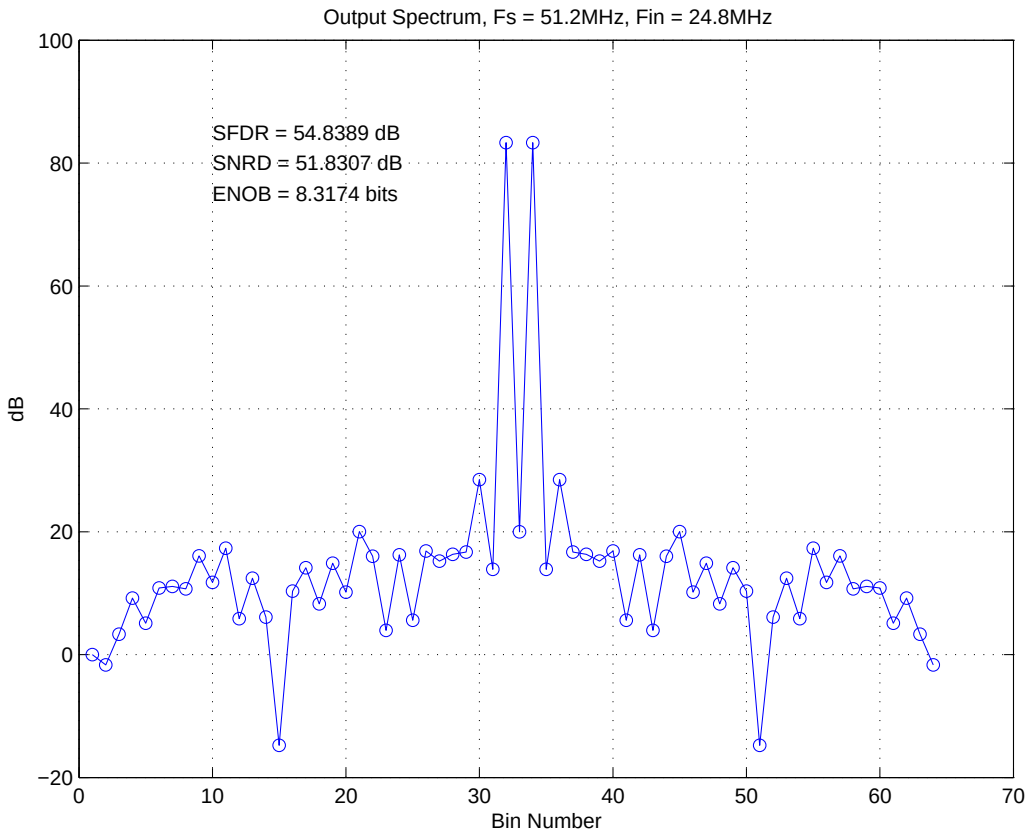

Figure 5.5: Spectrum for extracted stages, clock and shift register at 24.8MHz.

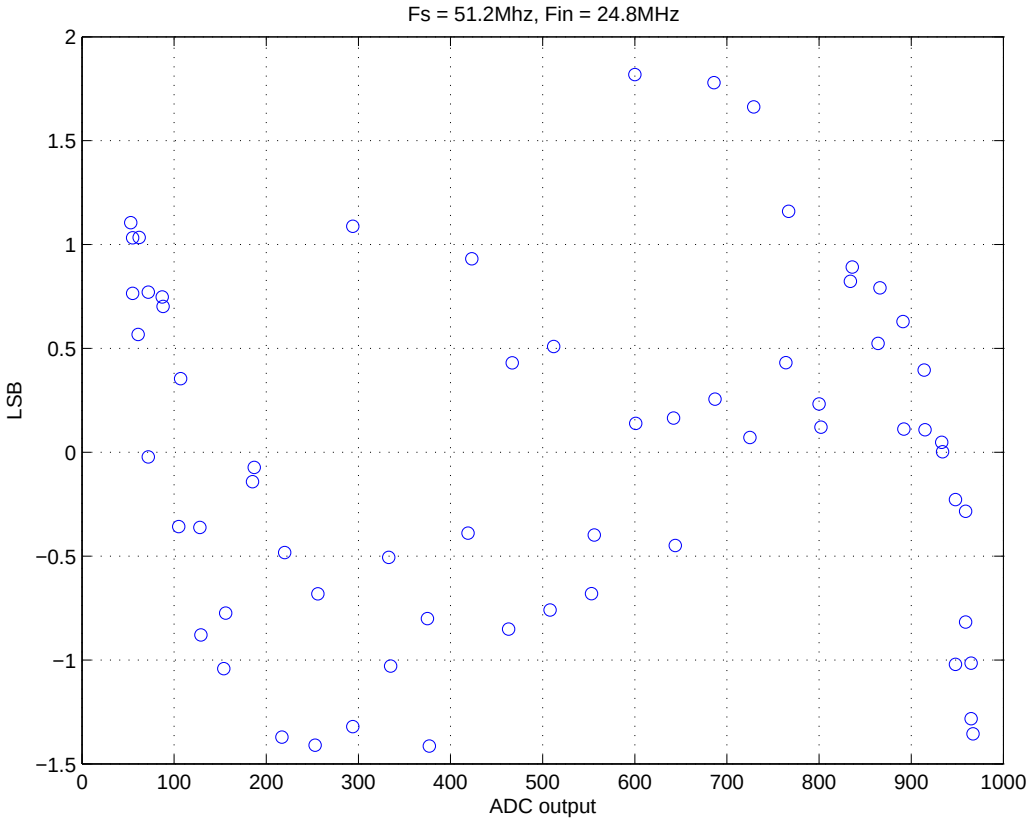

Figure 5.6: Output error including all harmonics except DC and test signal for extracted stages, clock and shift register at 24.8MHz.

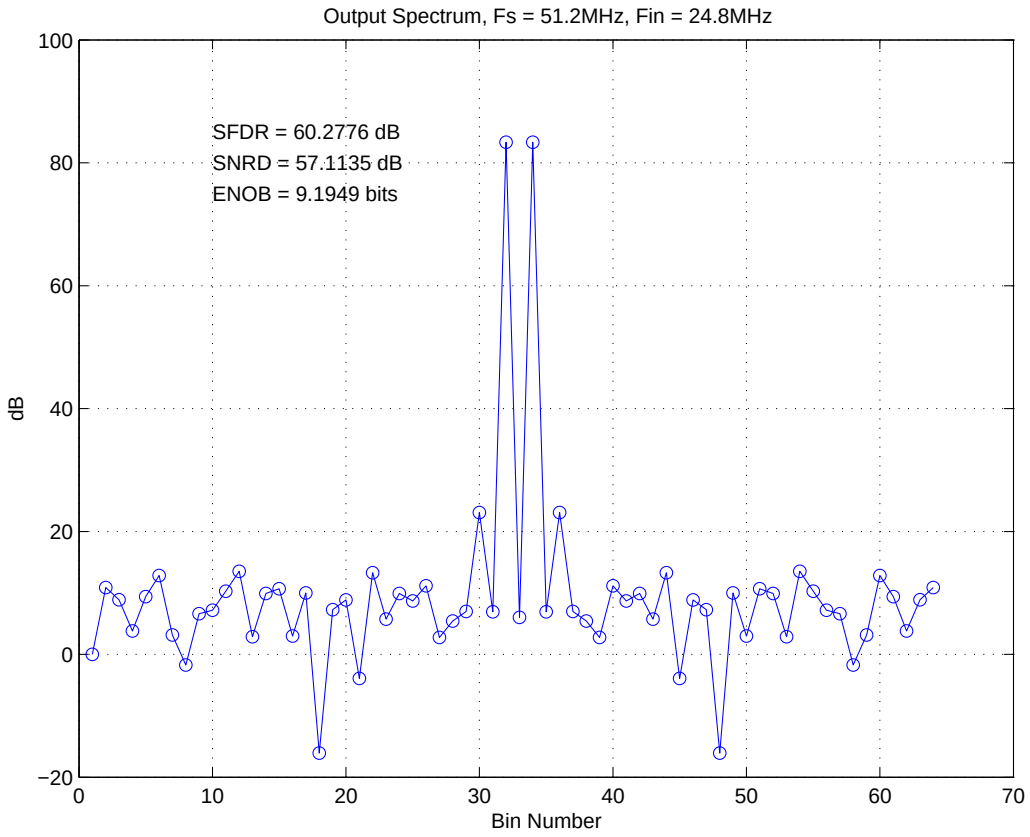

Figure 5.7: Output error including all harmonics except DC and test signal for extracted output drivers at 24.8MHz.

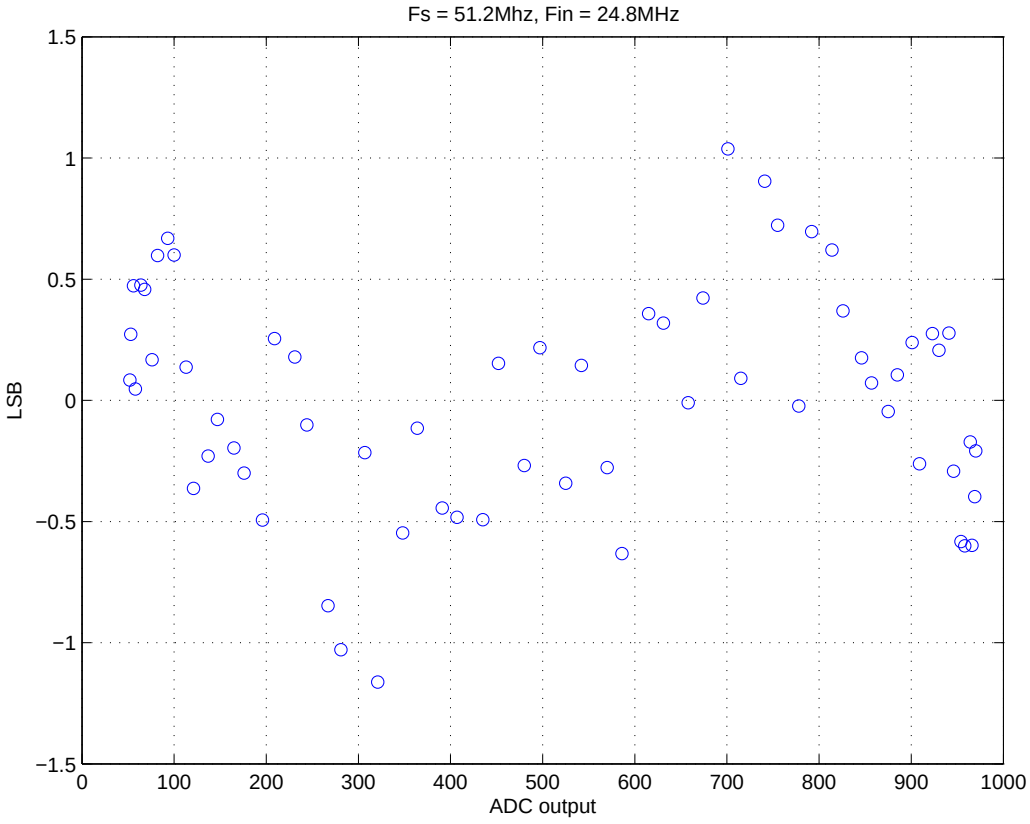

Figure 5.8: Output error including all harmonics except DC and test signal for extracted output drivers at 24.8MHz.

Chapter 6

Test and Characterization

6.1 Introduction

This chapter discusses the performance characteristics of the fabricated ADC. In order to test the functionality and performance of the chip, a two-layer PCB test board was designed and fabricated. The test board is designed to provide the chip with differential input signal from a single source function generator, a clean clock signal, reference and common mode voltages and clean power supply. The test board also contains circuitry to latch and buffer the output data from the chip which is captured by the logic analyzer. Collected data is processed using MATLAB. Figures 6.1 and 6.2 show the schematics of the test board. Equipment used to conduct ADC tests is listed in Table 6.1.

6.2 Power Consumption

The first test conducted on a chip was a power consumption test. Once the chip was powered up the total current draw was 40mA. Running from 5V power supply this corresponds to power consumption of 200mW. This is comparable to simulated result of 191mW. Performance specifications are listed in Table 1.1.

6.3 Performance test

Initially, the clock provided by the chip was used to latch the output data. To test the chip, sampling frequencies in the range of 20MHz - 80MHz were used. The

Device	Model	Function
Signal Generator	HP8645A	Input signal
Signal Generator	HP8642A	Clock
DC Power Supply	HP6205B	Helps generate VCM, VREF+ and VREF-
DC Power Supply	XP-660	VDD and VCCD supply for the chip
DC Power Supply	LA-200	1VCM for the chip
Logic Analyzer	HP16500B	Used to capture data

Table 6.1: Description of test equipment used.

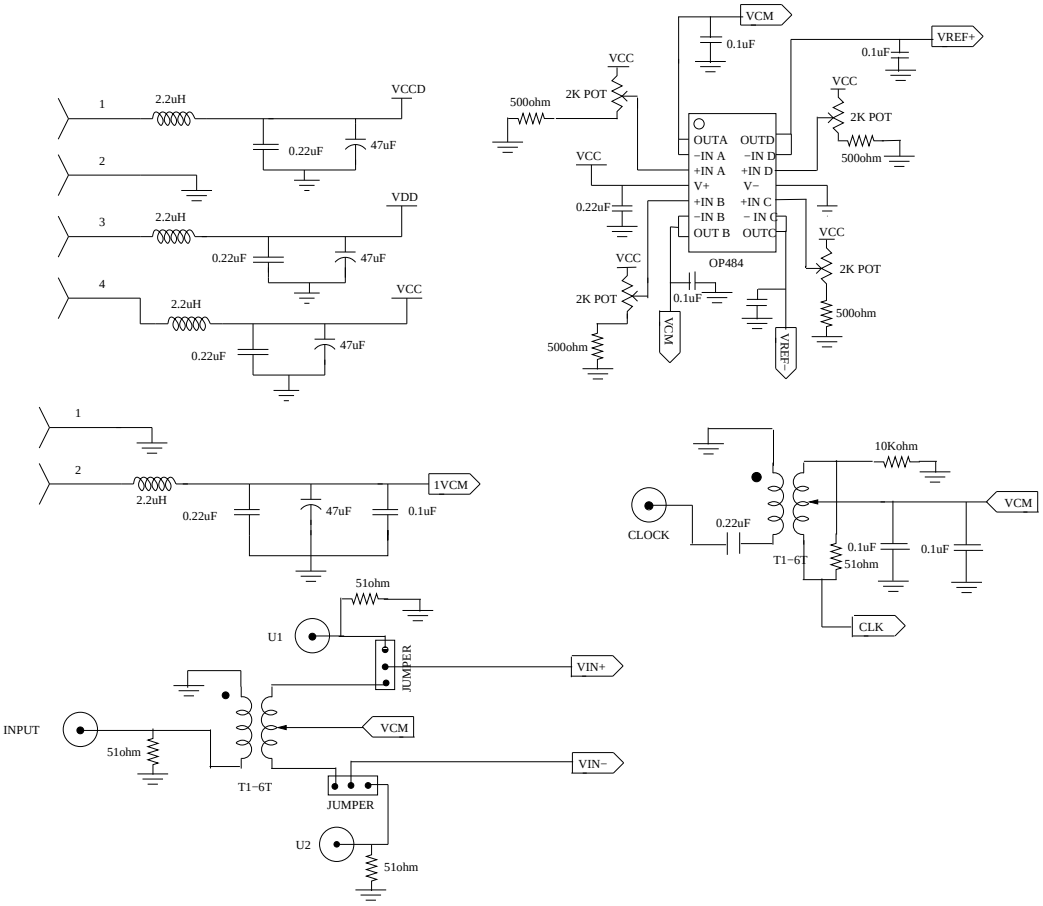

Figure 6.1: Test board schematic for the supply and reference voltages, input signal and clock.

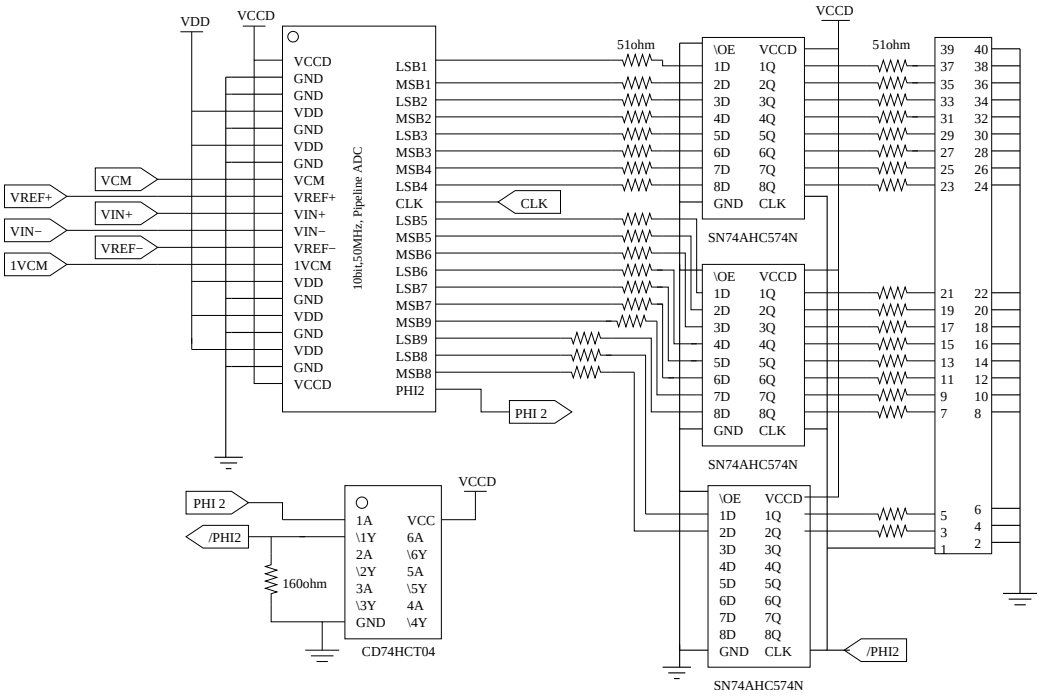

Figure 6.2: Test board schematic for data capture interface.

logic analyzer used to collect the output data cannot run at the frequencies less than 20MHz.

First test conducted was at sampling rate of 50MHz and input frequency of 1MHz. Once the data was processed in MATLAB intermediate bits from the first eight stages of the pipeline were having as output 11 state. For a 1.5bits/stage architecture, only 00,01 and 10 states are allowed. Only the last stage of the pipelined converter can output 00, 01, 10 and 11. After slowing down the clock and not seeing any changes in converter's performance, the output data after the latch was looked at. Refer to Figure 6.2 for the test board schematics of the data capture interface. The latch used on the test board triggers on the rising edge of the clock. Using the oscilloscope the rising edge of the output clock together with the output data was examined. It was noticed that during rising edge of the clock, output data was unstable and it was changing. Having unstable data during the capture phase can cause the undesired state of 11 to occur. The problem was fixed by inverting the clock and using the new clock to capture the output data. Figure 6.2 shows the clock from the chip after being inverted. Modification of the test board fixed the data capture problem for a clock frequency of 41MHz. Anything below or above this frequency introduced instability on data capture interface side. This may be due to the test-board design and poor signal routing considerations. The logic analyzer used is operating at minimum frequency of 20MHz and therefore test with the clock frequency below 20MHz were not conducted.

6.3.1 Low Frequency Tests

To show the performance of the converter different test frequencies were looked at. All tests were run at the sampling speed of 41MHz and input amplitude of -1dBFS. Figures 6.3 to 6.6 show the output spectrum for low input frequencies from 1-8MHz. These figures also list the SFDR, SNRD and ENOB values for a given input frequency. It can be seen that SFDR, SNRD and ENOB values are comparable to simulation results discussed in Chapter 5.

6.3.2 High Frequency Tests

The high test frequencies were used to compare performance of the converter to the simulation results from Chapter 5. Figures 6.7 to 6.10 show the output spectrum for different high input frequencies from 15 - 20MHz. These figures also list SFDR, SNRD and ENOB values for a given input frequency. It can be

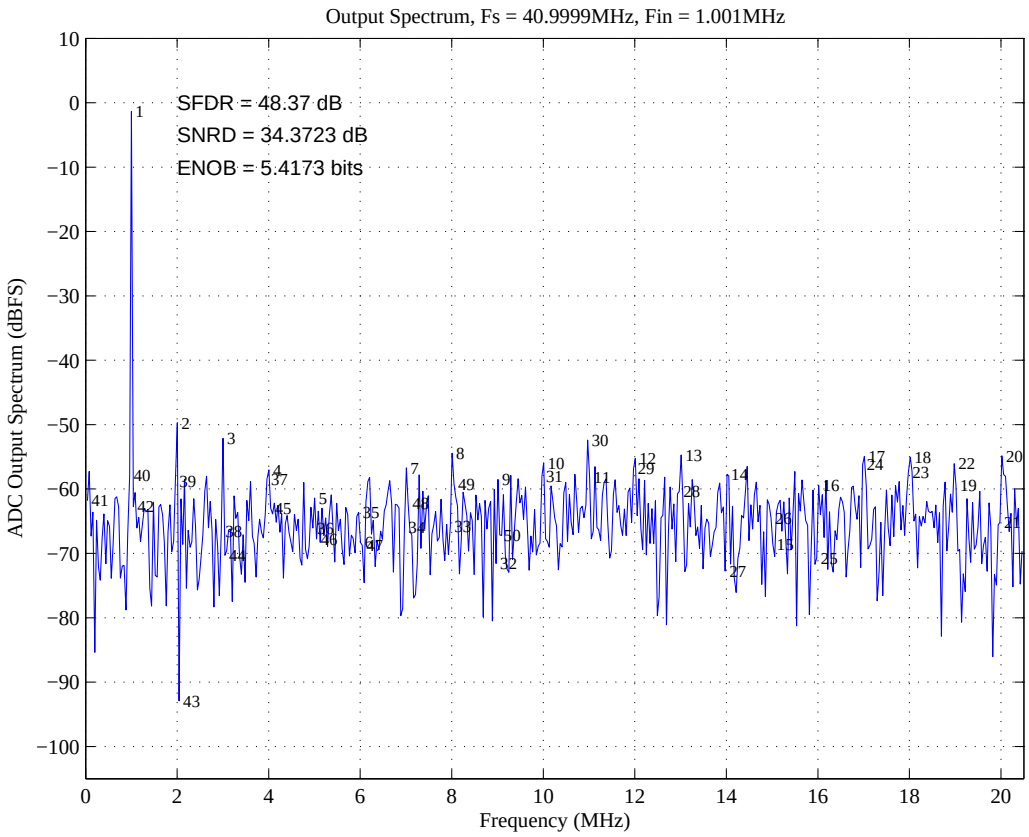

Figure 6.3: Output spectrum for a 1MHz test frequency at 41MHz sampling rate.

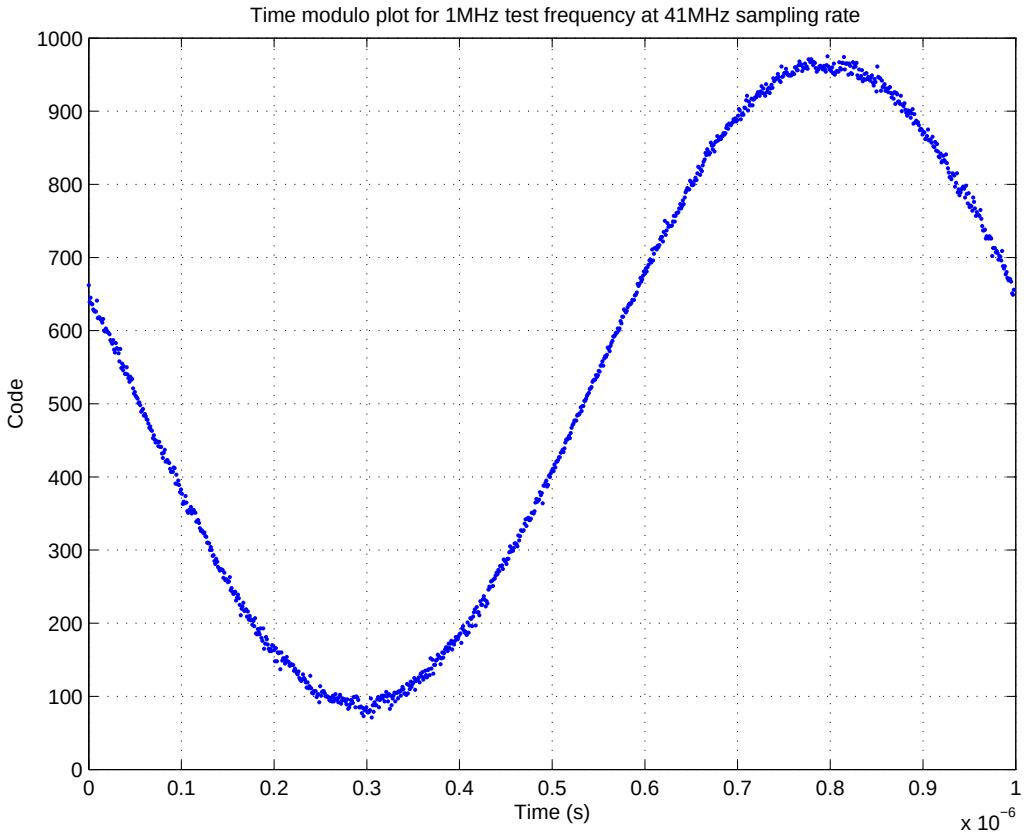

Figure 6.4: Time modulo plot for 1MHz test frequency at 41MHz sampling rate.

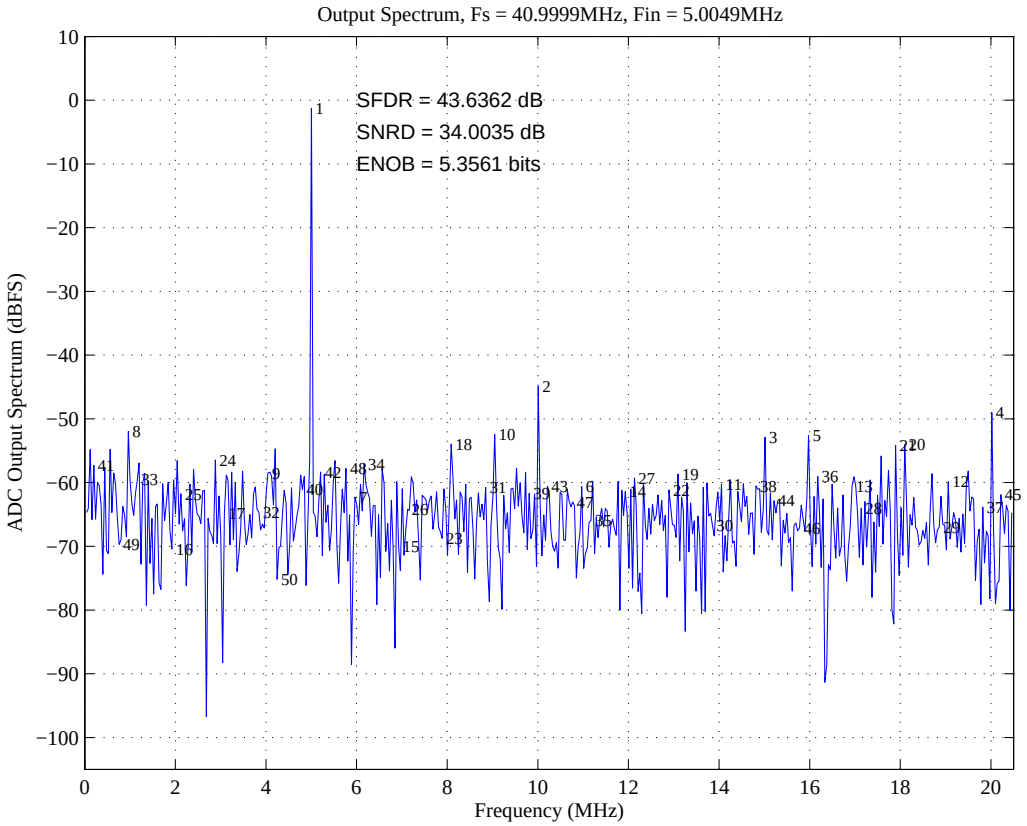

Figure 6.5: Output spectrum for a 5MHz test frequency at 41MHz sampling rate.

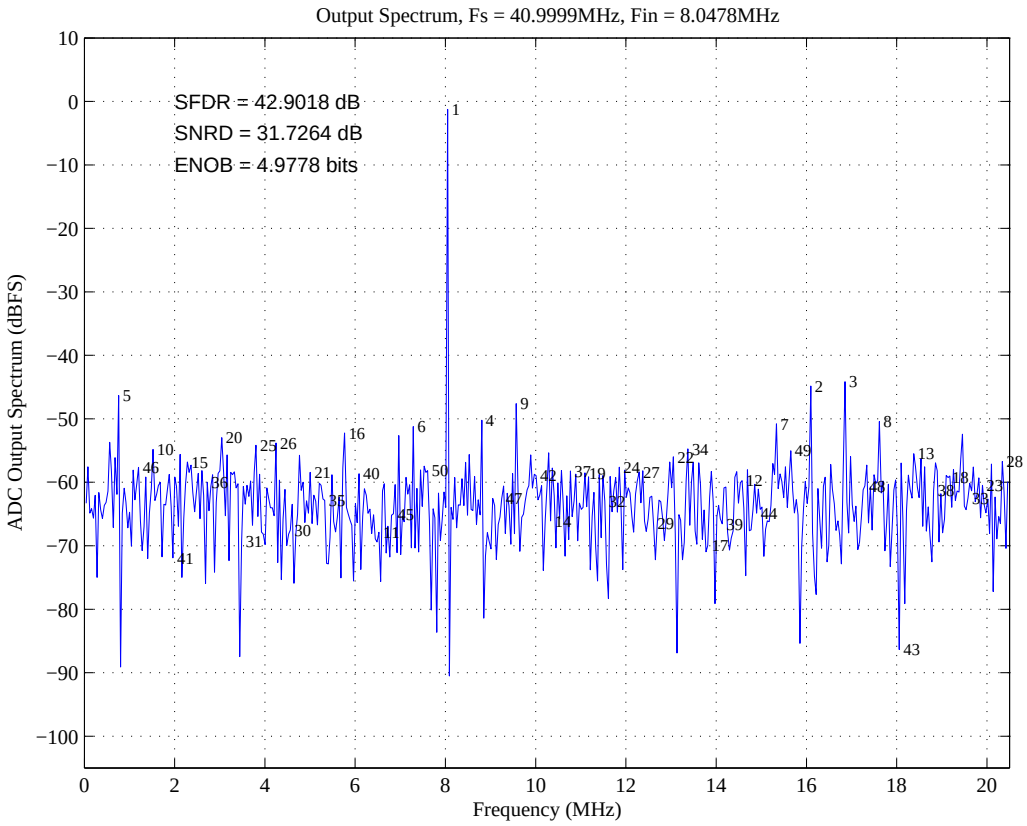

Figure 6.6: Output spectrum for a 8MHz test frequency at 41MHz sampling rate.

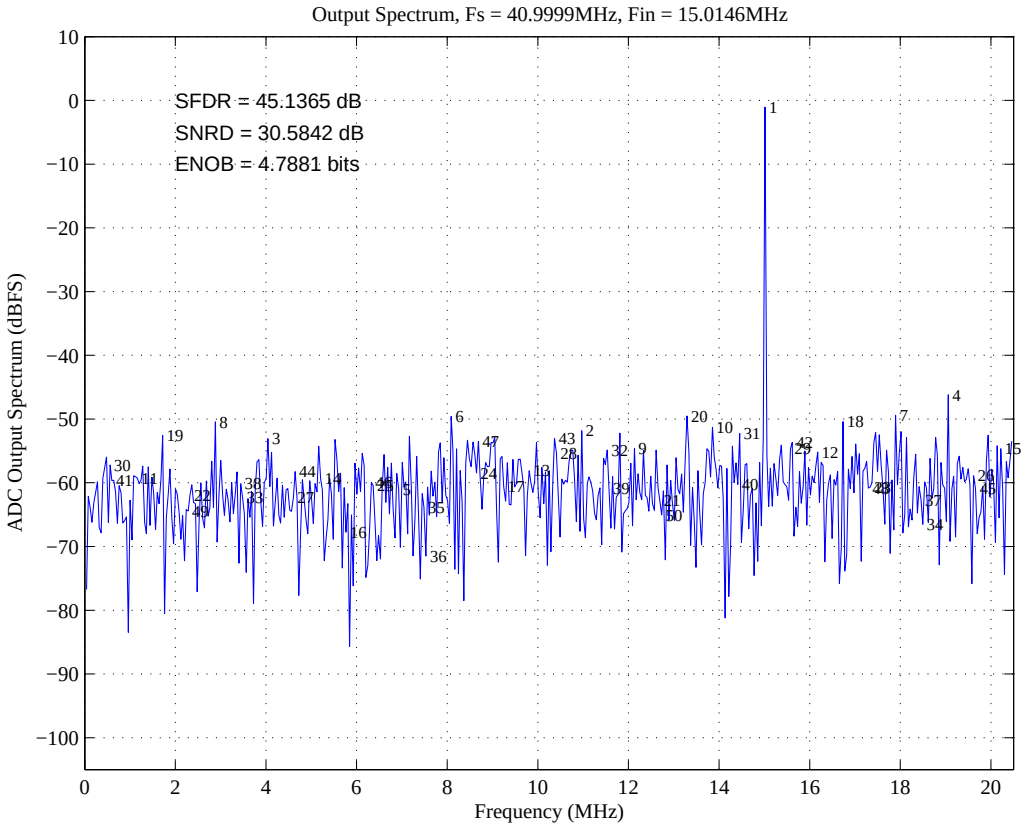

Figure 6.7: Output spectrum for a 15MHz test frequency at 41MHz sampling rate.

seen that test results correlate with simulated results discussed in Chapter 5 where simulations with parasitic capacitances were conducted. Small degradation in results is to be expected because when running simulations power supply noise was not simulated.

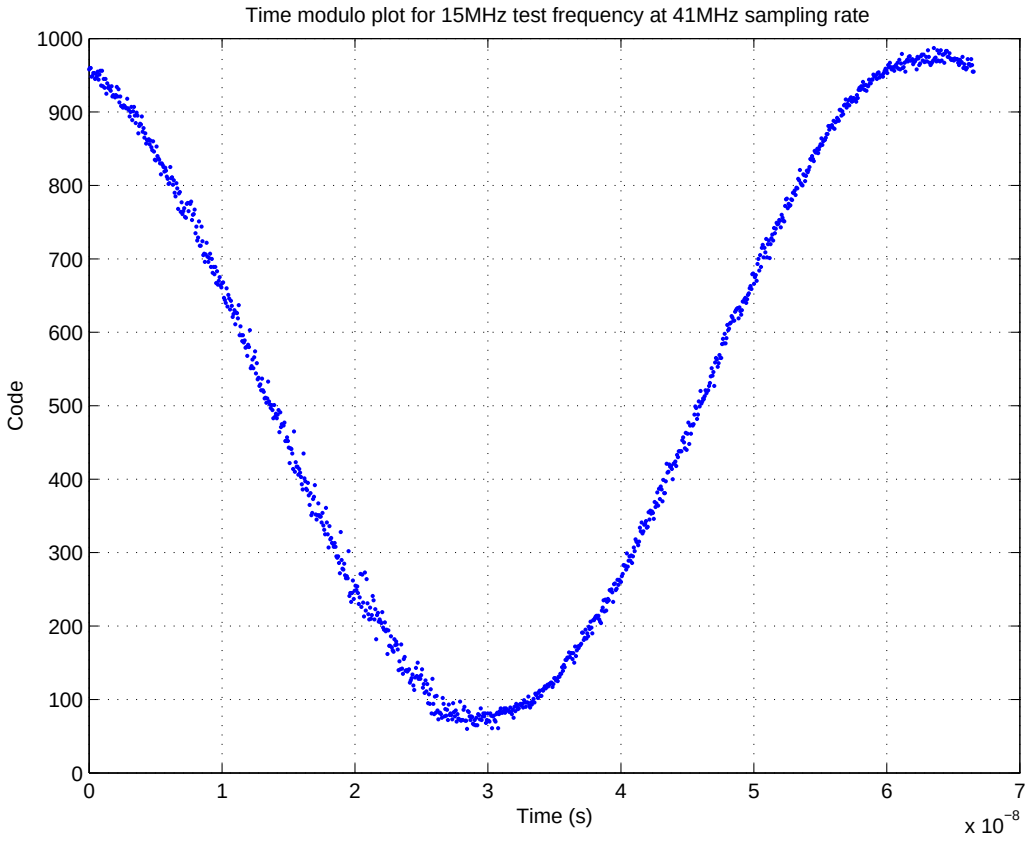

Figure 6.8: Time modulo plot for 15MHz test frequency at 41MHz sampling rate.

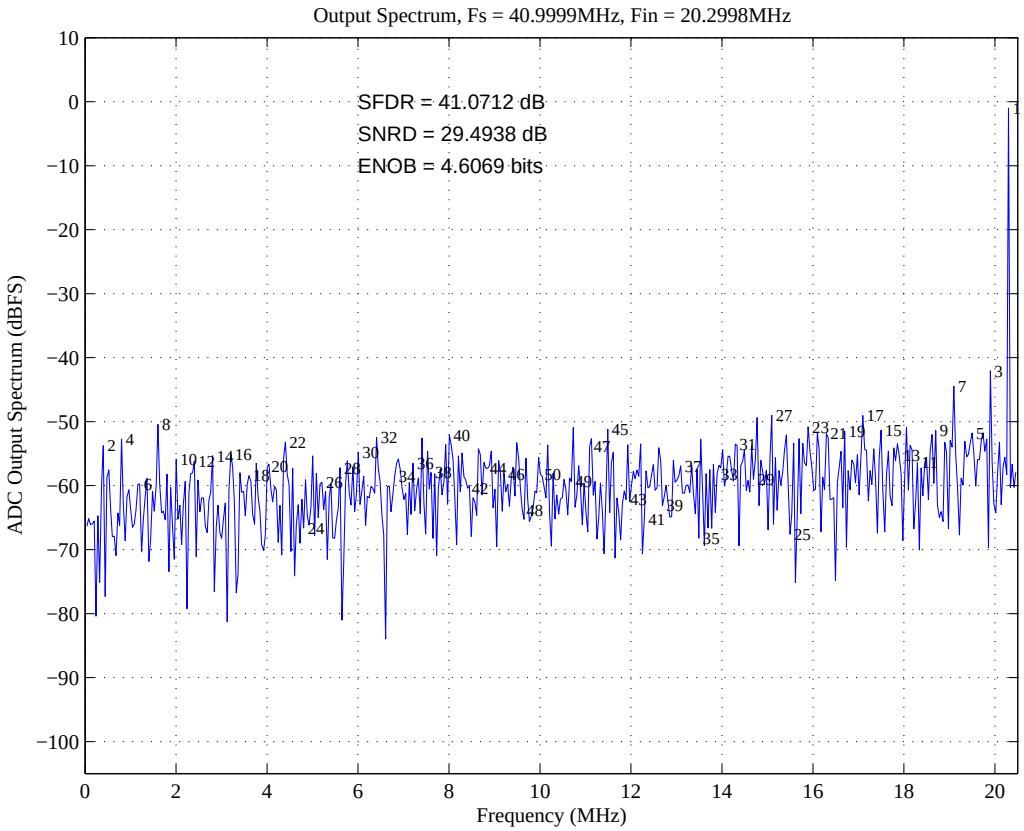

Figure 6.9: Output spectrum for a test frequency close to the Nyquist at 41MHz sampling rate.

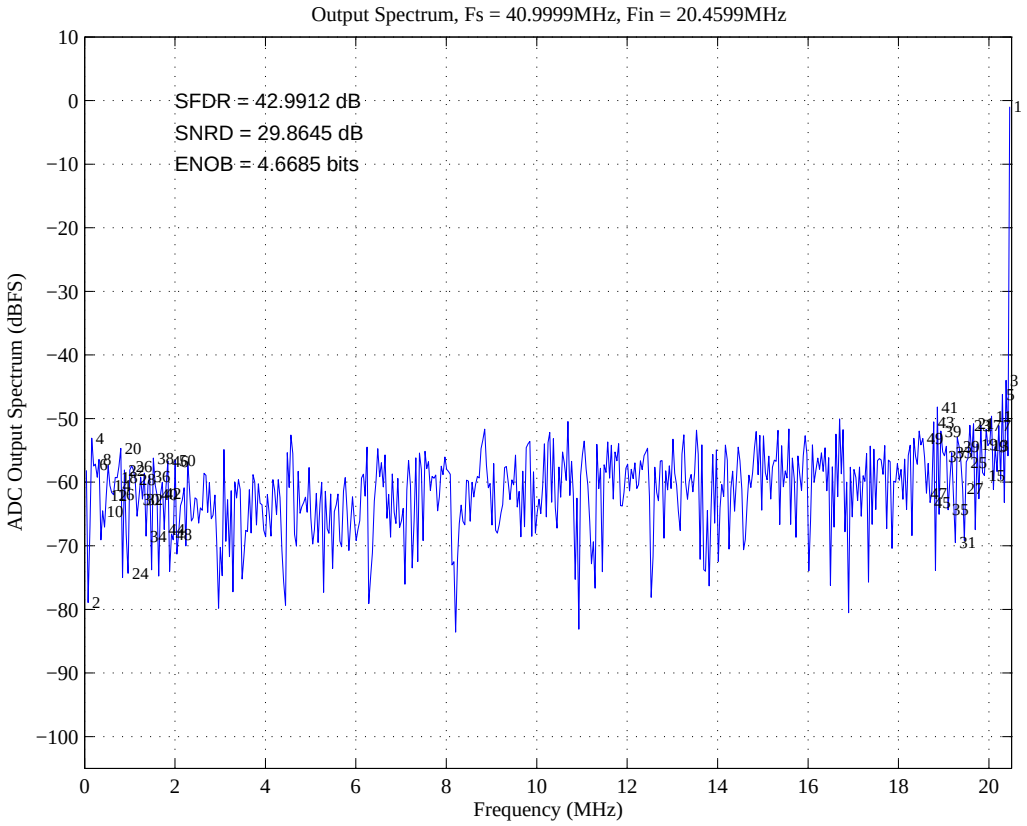

Figure 6.10: Output spectrum for a Nyquist test frequency (bin 511) at 41MHz sampling rate.

Chapter 7

Conclusions

7.1 Summary of the Results

The objective of the project was to design a high speed, analog to digital converter (ADC) which will operate from a 5V power supply and provide the intermediate stage outputs off chip. The converter should accept -1 to 1 volt (2.5V common mode offset) fully differential input. All of the objectives were accomplished. The current design is running at 50MHz and simulation results on the schematics level showed to be promising. Refer to Chapter 3. However the extracted simulation has shown a significant degradation in the converter performance and fabricated chip is resembling these results. Test and characterization results of a fabricated chip are comparable to the extracted simulation. However, two layer PCB test-board showed to be of a poor design to be able to conduct tests at clock frequencies higher than 41MHz. Too much noise on the board, probably due to signal routings, introduced only one good test frequency for the chip. This was a frequency of 41MHz. Compared to the extracted simulation results, fabricated chip shows lower effective number of bit (ENOB) and spurious free dynamic range (SFDR). ENOB was down by 1.5 bits and SFDR was lowered by 3dBs.

7.2 Future Work

The initial design goal was to have a pipeline ADC running at 100MHz. The building blocks of the stage were designed to run at 100MHz, however once stages were cascaded together the performance has degraded significantly to slow down the converter to 50MHz. This was shown in Chapter 3. One known problem are

comparators. Current comparator design has shown a tendency to change a decision state when it should be stable. New comparator designs should be looked at and implemented to see if the speed can be brought back to at least 80MHz.
Once the extracted simulation was run there was a significant degradation in the performance compared to the simulation results conducted on the schematics level. There was a 20dB drop in SFDR and 10dB drop in SNRD. What should be looked at are the interconnect metal lines which provide input and output. They may contribute enough parasitic capacitance to effect the input signal and cause degradation in the final performance. Also, more emphasis should be put on the PCB test-board design. Details such as best signal routings to reduce the noise on the board should be taken into consideration.

7.3 Biography of the Author

Alma Delić-Ibukić was born in Bihać, Bosnia-Herzegovina on October 20th, 1978. She came to US in 1996 and completed her last year of high school before enrolling in the Electrical Engineering program at the University of Maine in 1997. She received a BS in Electrical Engineering from the University of Maine in May of 2002. She is currently a Research Assistant and graduate student pursuing a masters degree in the Department of Electrical and Computer Engineering at the University of Maine, Orono. She was a Texas Instruments scholar who spent eight month at Texas Instruments in Dallas working on test and characterization of ADCs. Her work at Texas Instruments is the driving force behind her research in error compensation methods on Pipeline A/D Converters. (alma.delic-ibukic@umit.maine.edu)

Appendix A

Circuits - Schematics

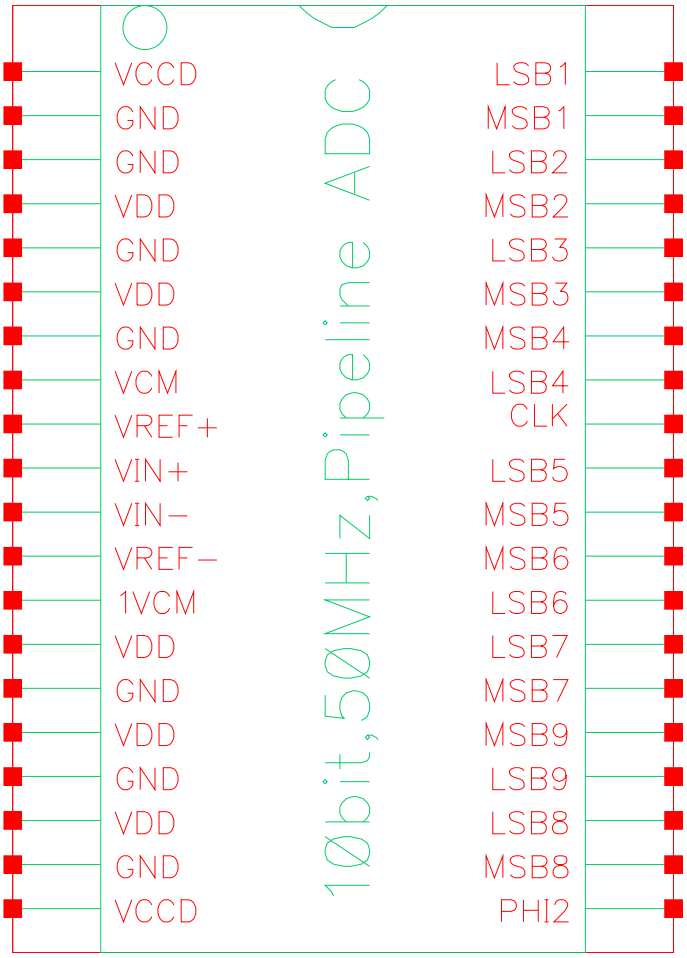

Figure A.1: Final Chip (External View).

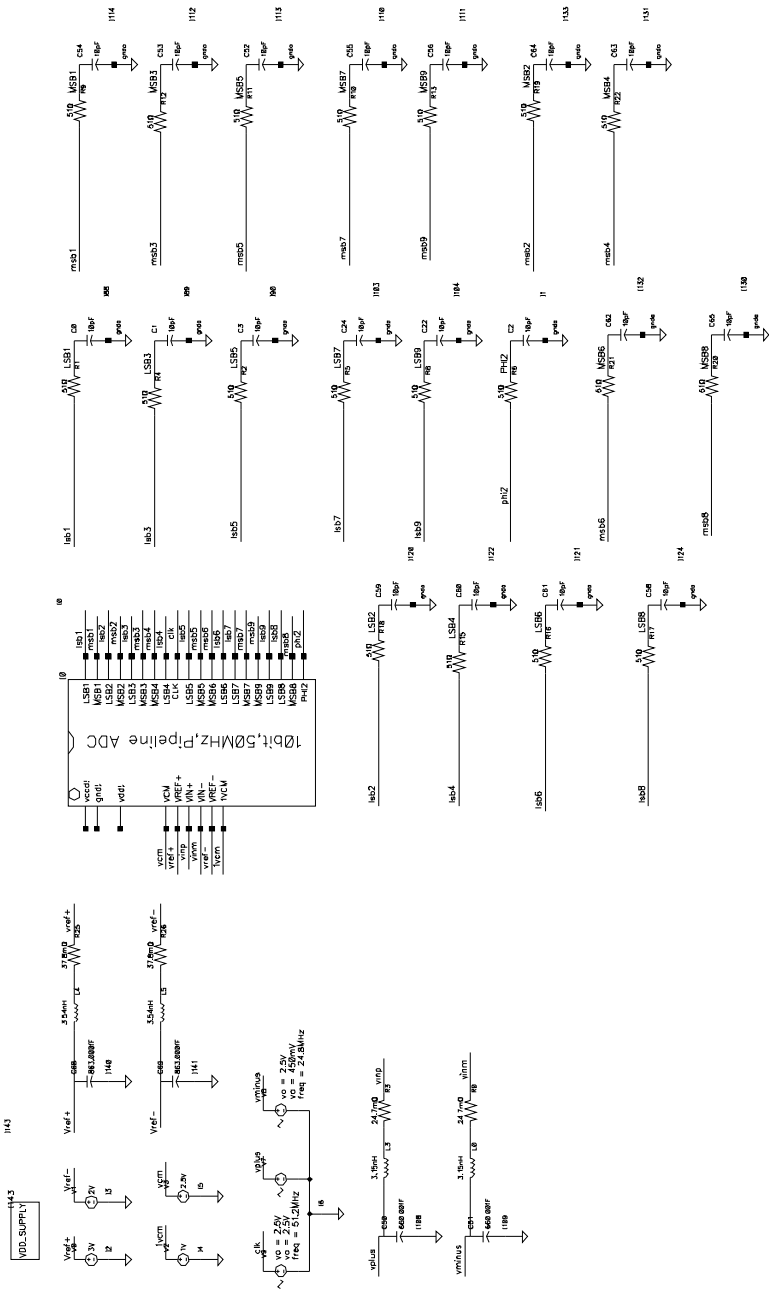

Figure A.2: Test configuration of the top-level schematics of the ADC.

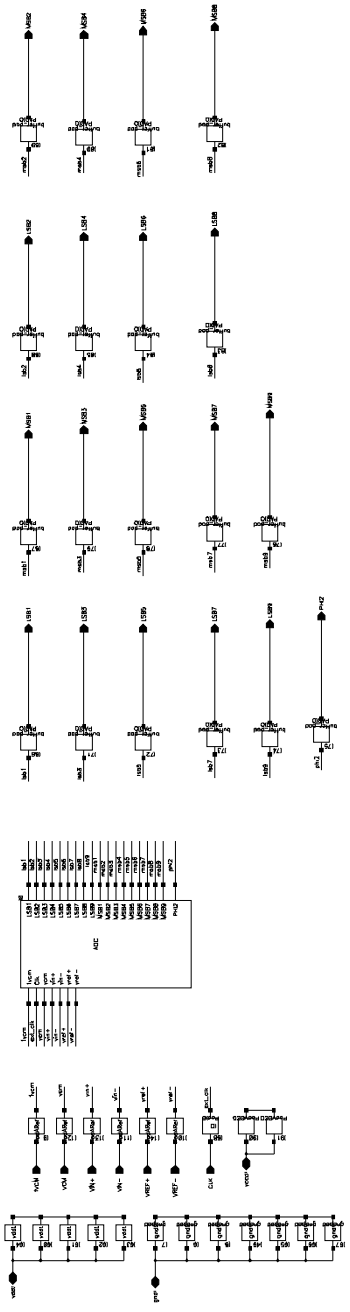

Figure A.3: Top-level schematics of the ADC.

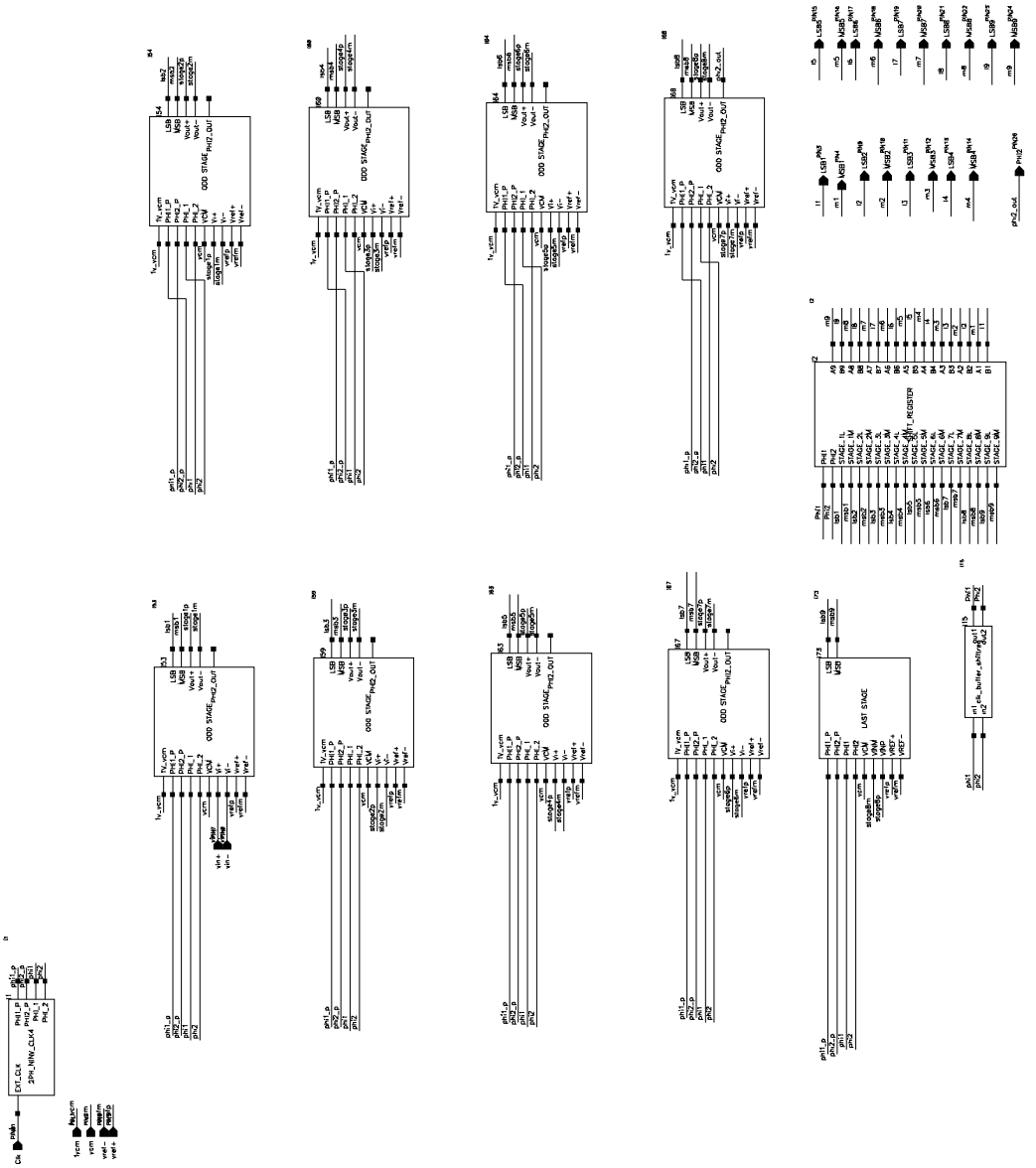

Figure A.4: 9-stages implemented together with the clock and shift register.

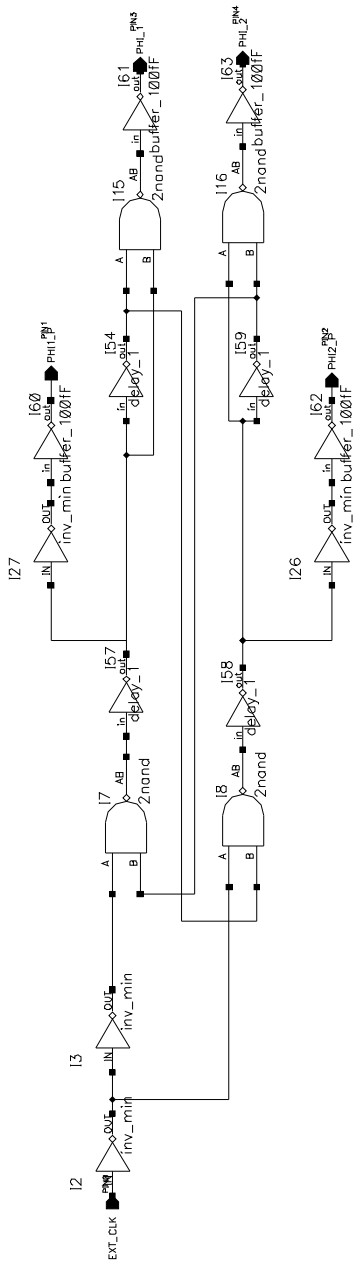

Figure A.5: Two phase non-overlapping clock.

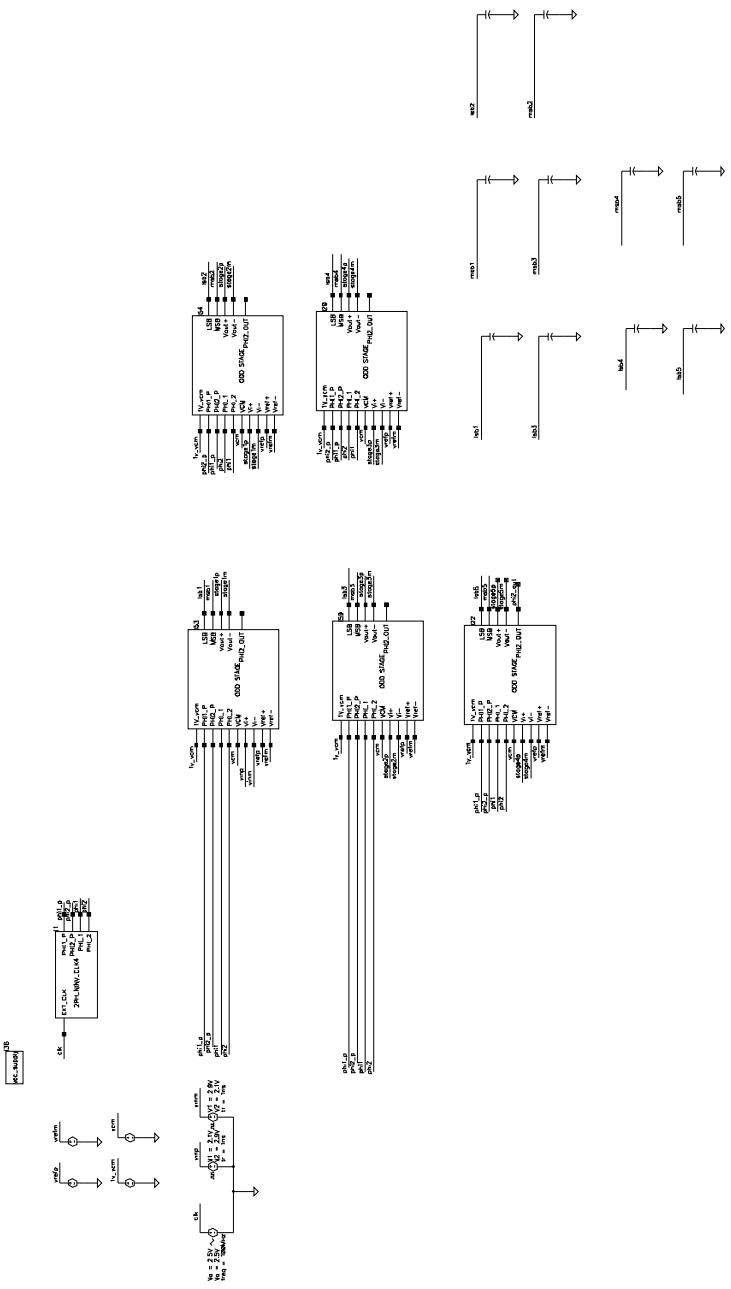

Figure A.6: Circuit configuration for testing 5-stages.

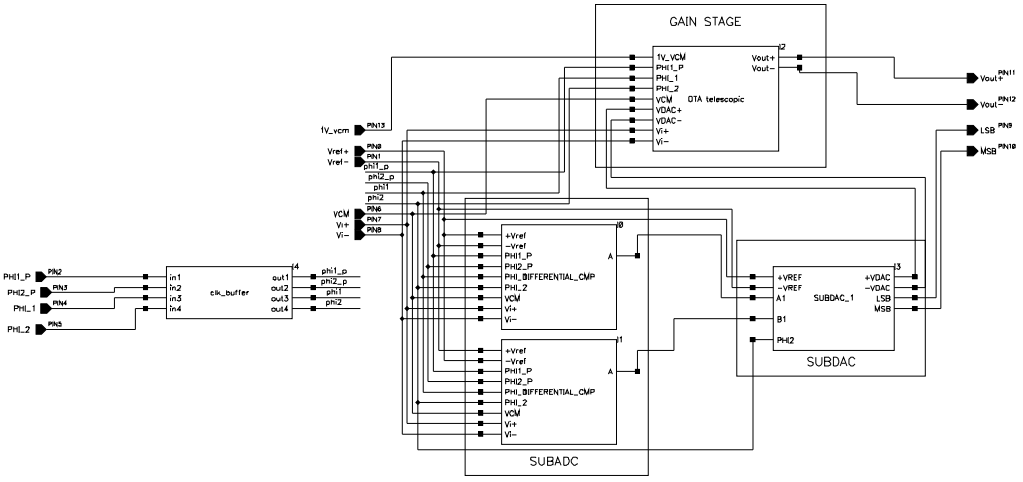

Figure A.7: Odd stage block. NOTE: Even stage has clock inputs interchanged.

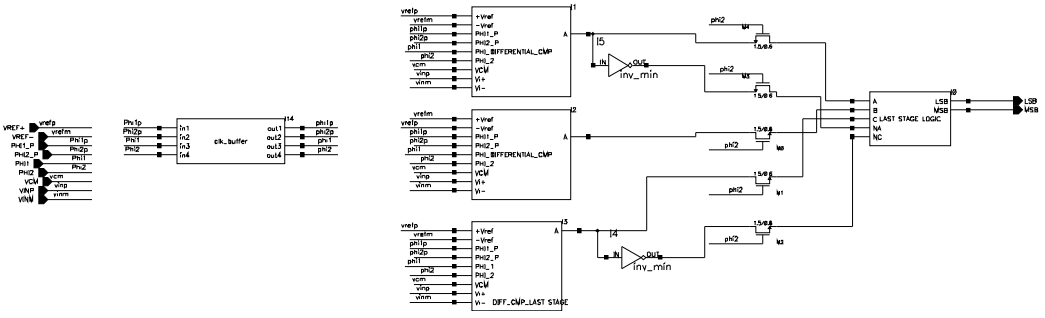

Figure A.8: Last stage block.

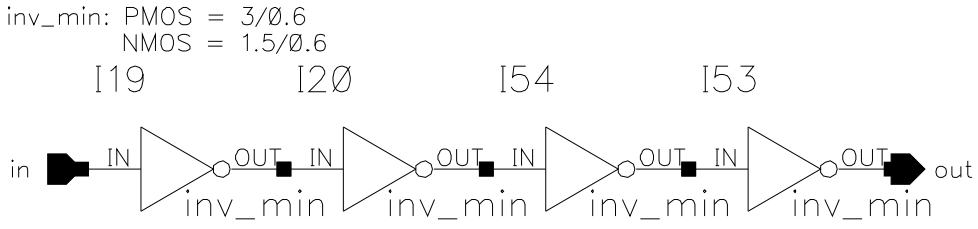

Figure A.9: Delay circuit used within the clock design.

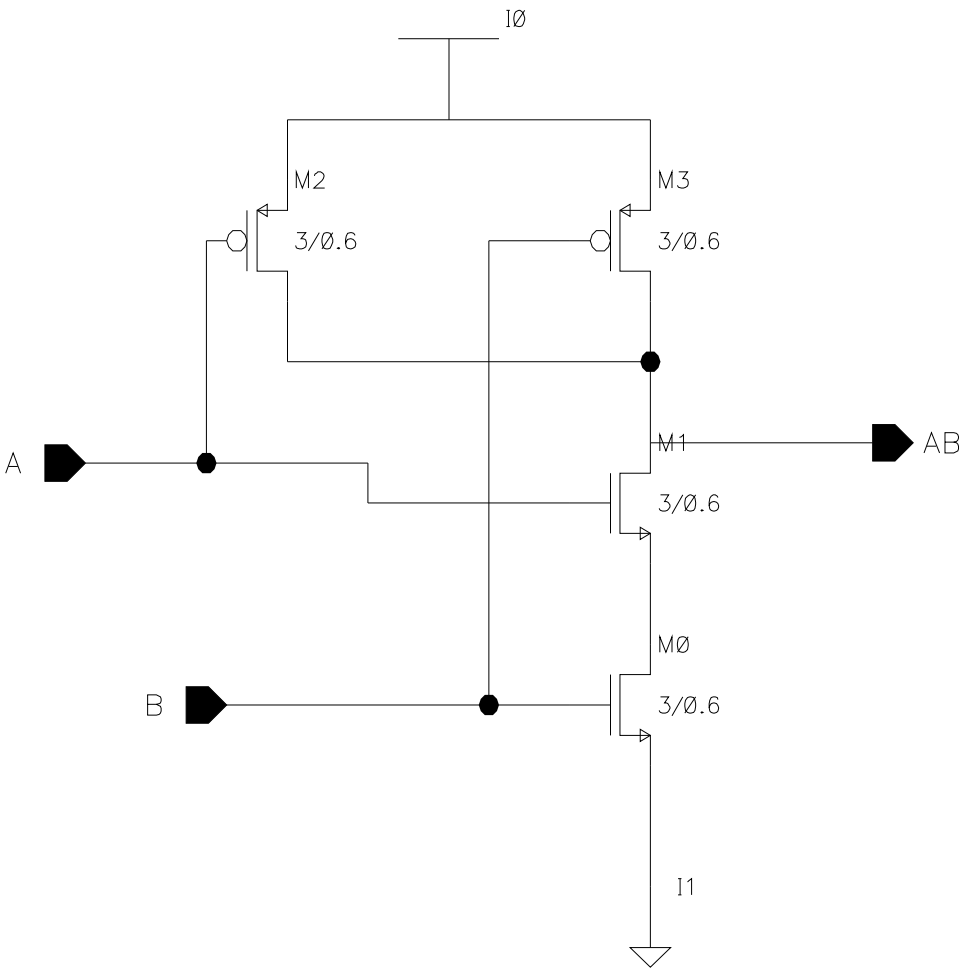

Figure A.10: 2-input NAND gate.

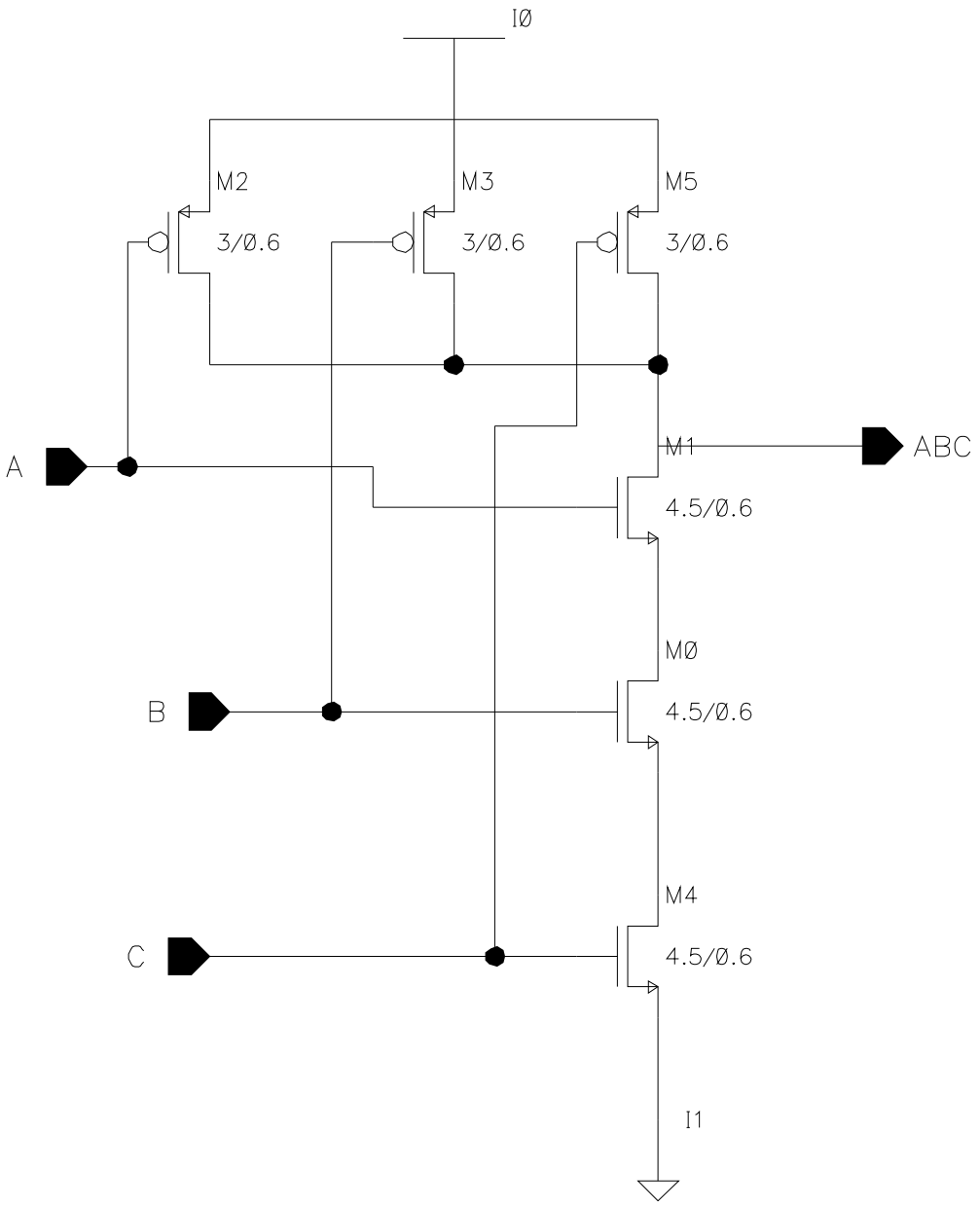

Figure A.11: 3-input NAND gate.

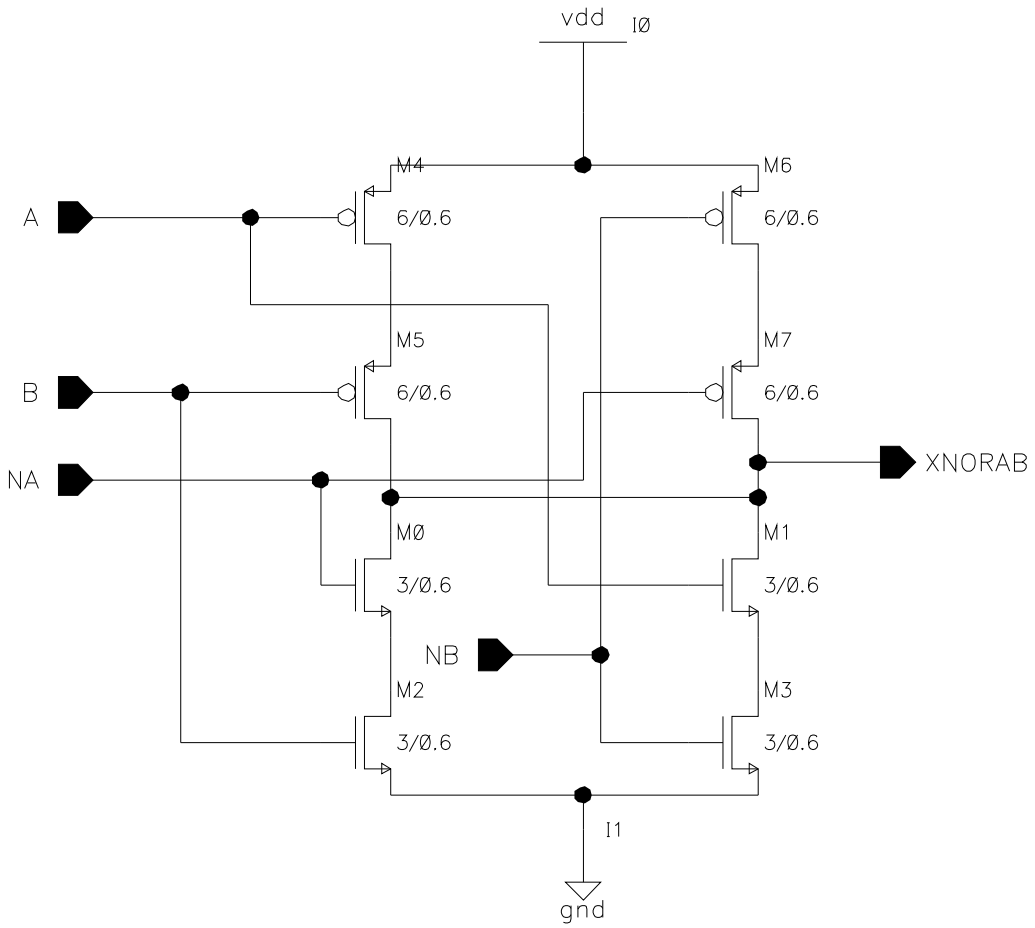

Figure A.12: Exclusive NOR.

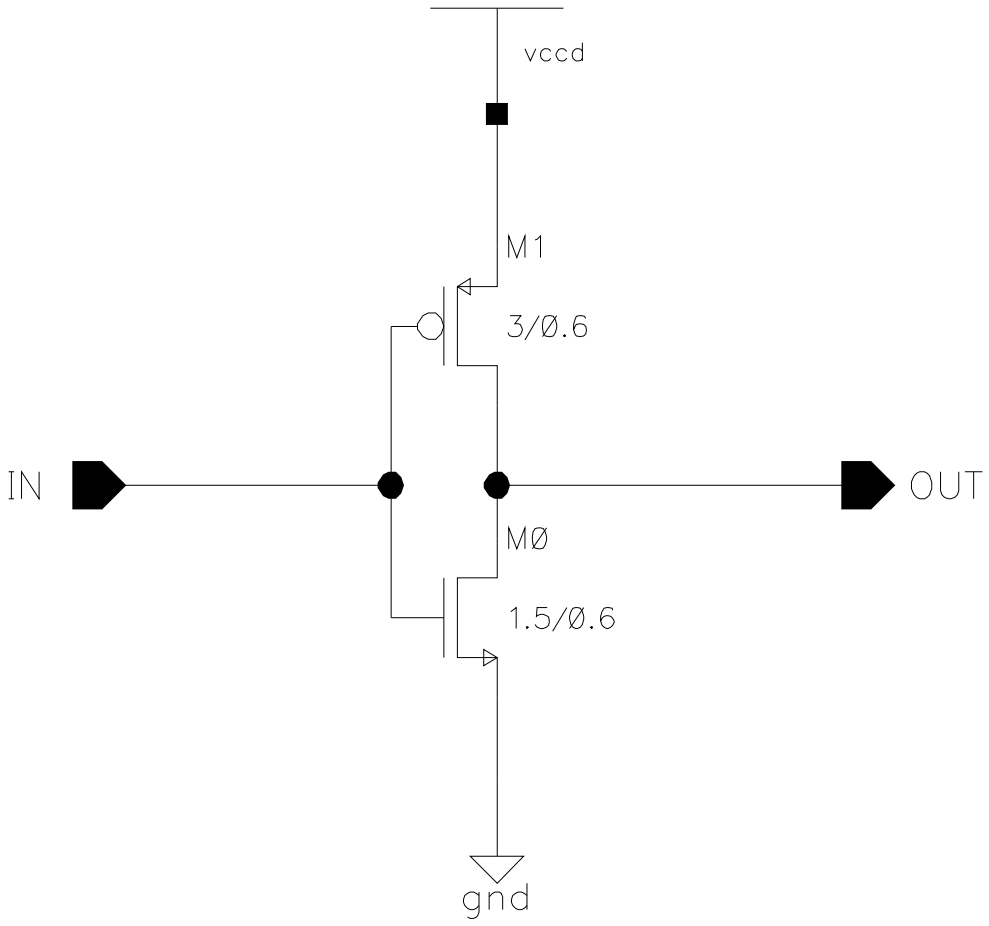

Figure A.13: Minimum sized inverter with PMOS connected to VCCD (used for output buffers).

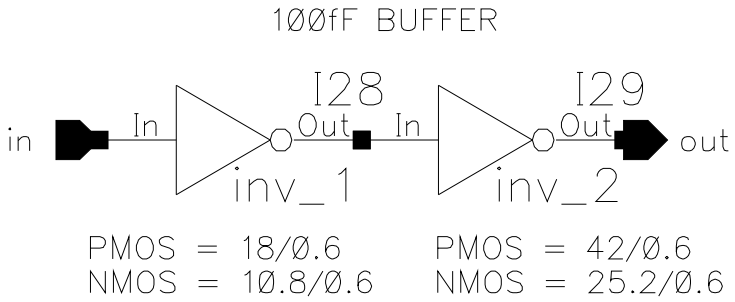

Figure A.14: 100fF buffer design.

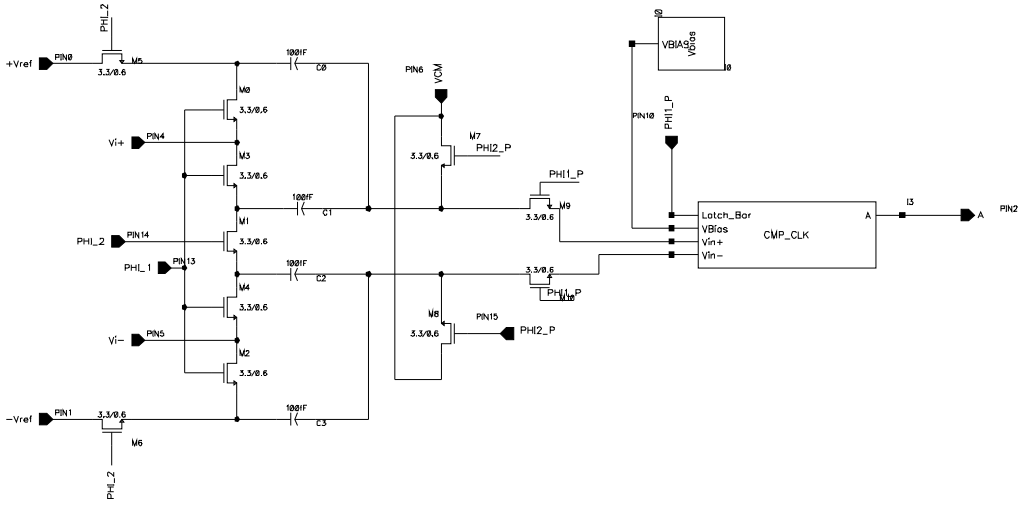

Figure A.15: Last stage differential comparator.

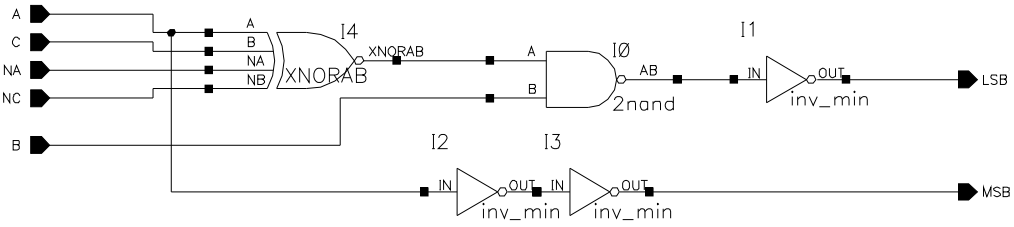

Figure A.16: Last stage logic.

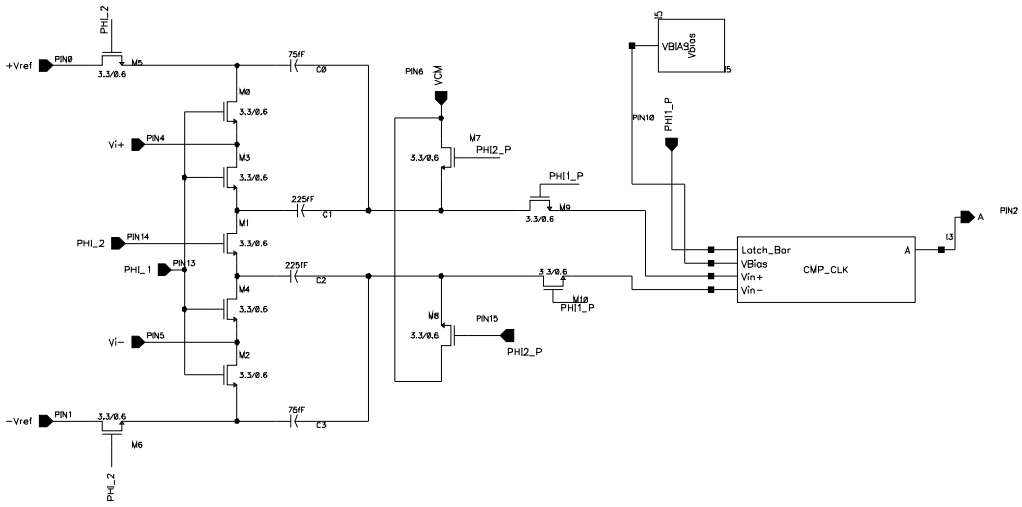

Figure A.17: Differential comparator (sub-ADC block).

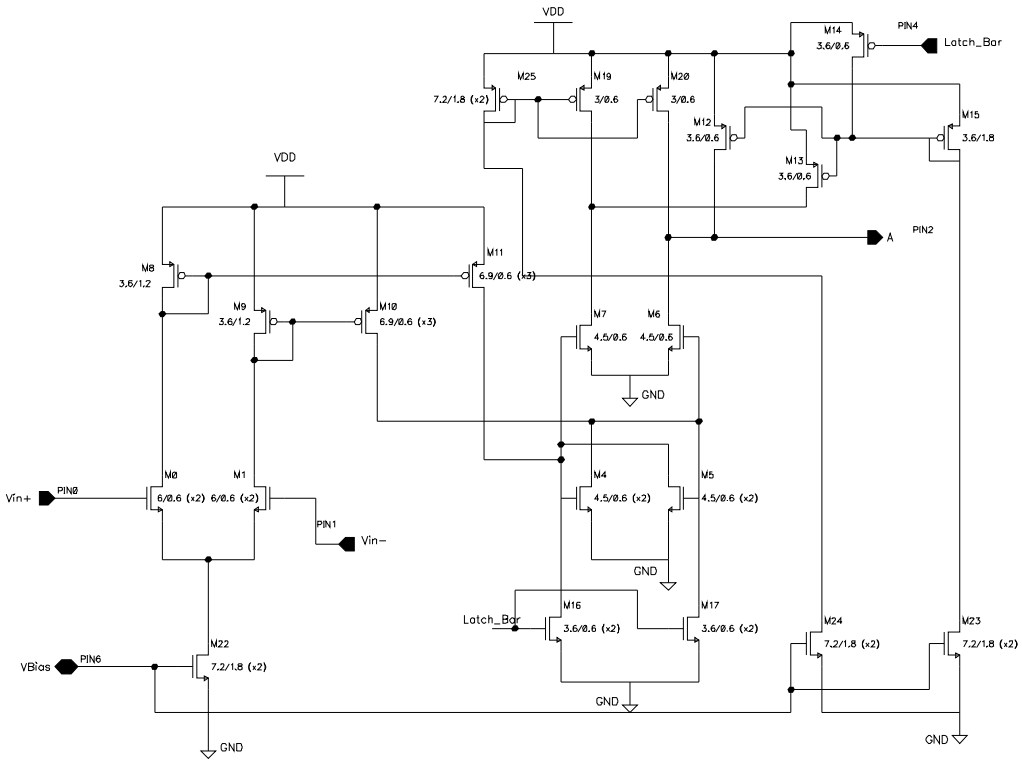

Figure A.18: Comparator design. (sub-ADC block).

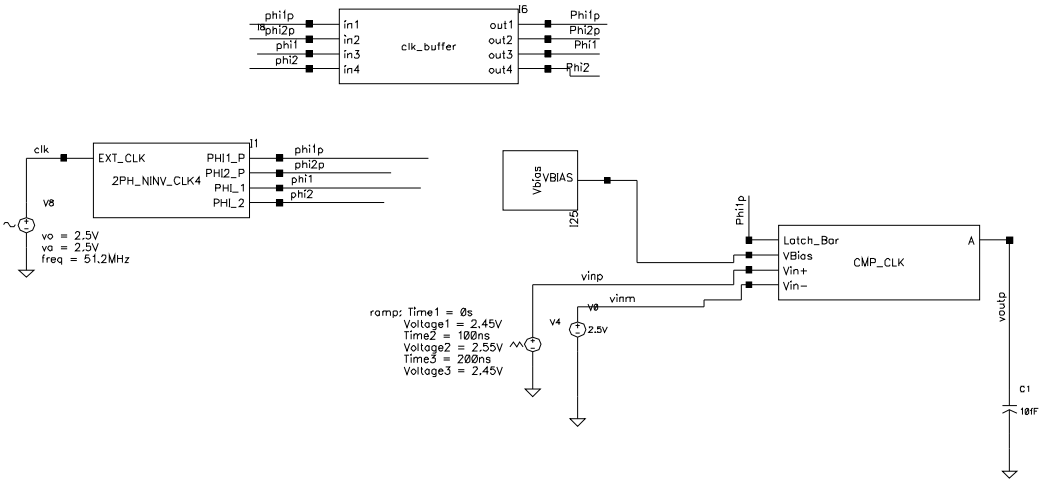

Figure A.19: Comparator test circuit.

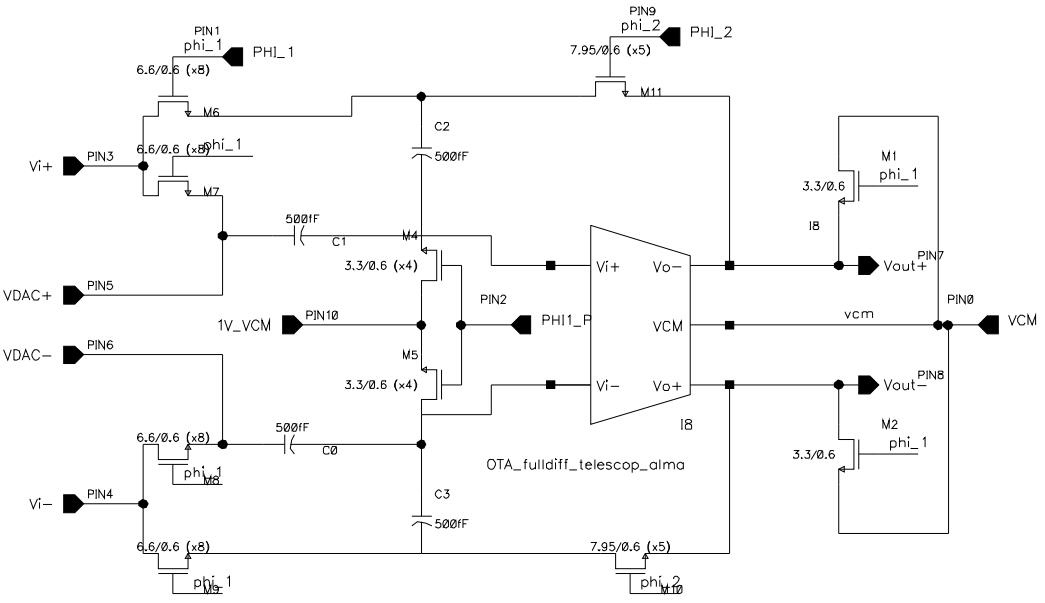

Figure A.20: Gain stage block.

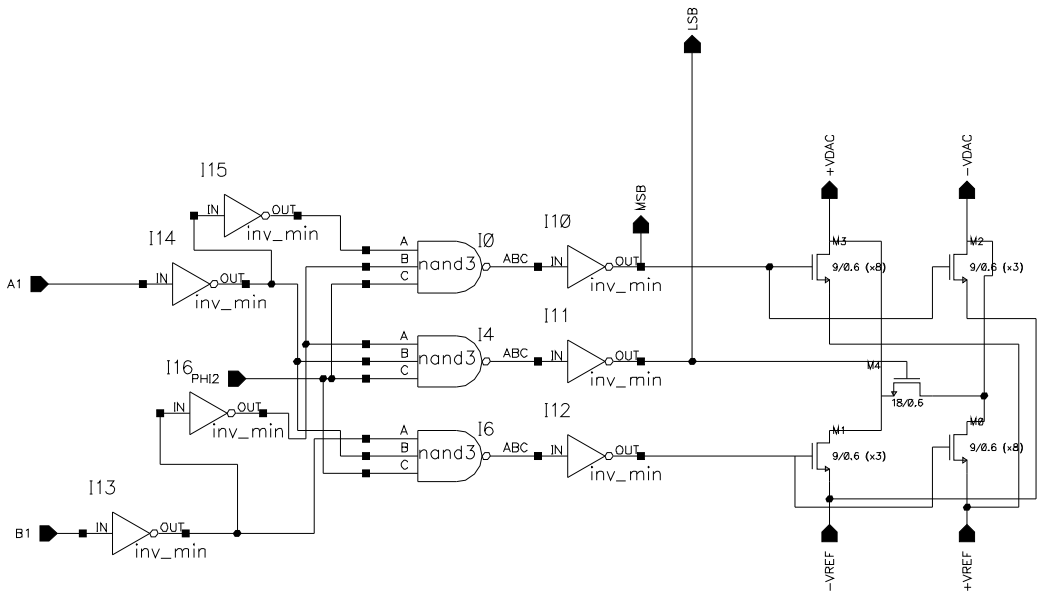

Figure A.21: Sub-DAC block.

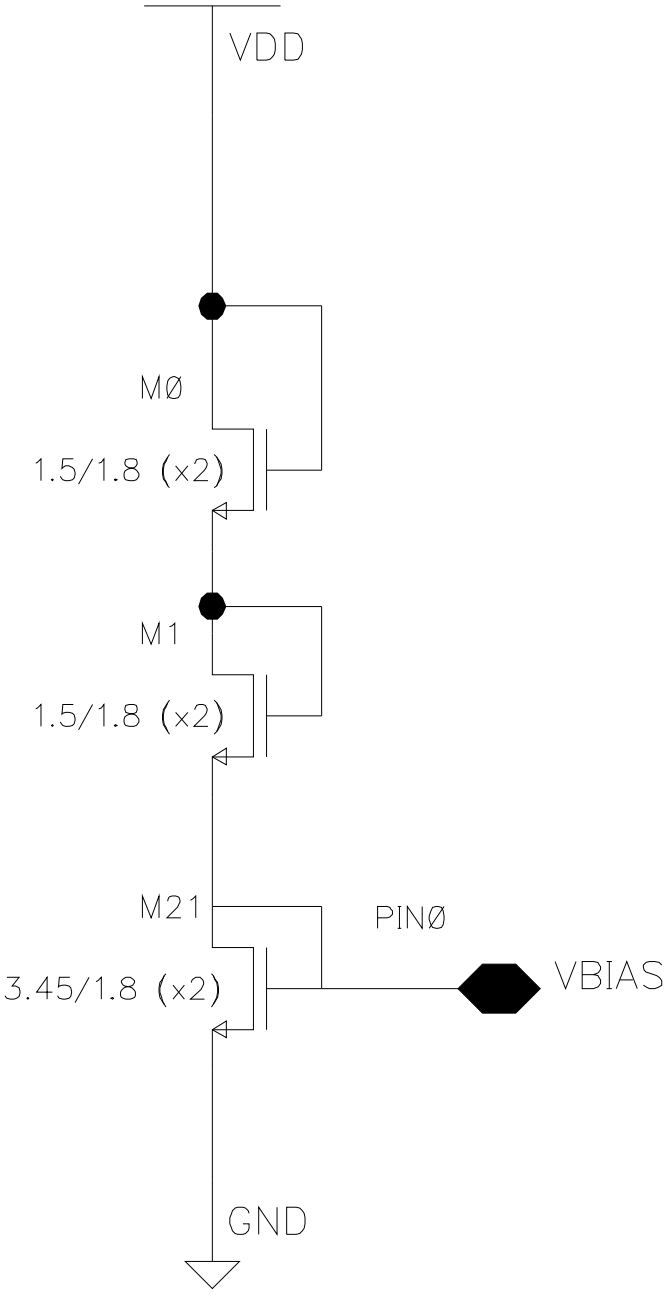

Figure A.22: Bias voltage circuit used in sub-ADC block.

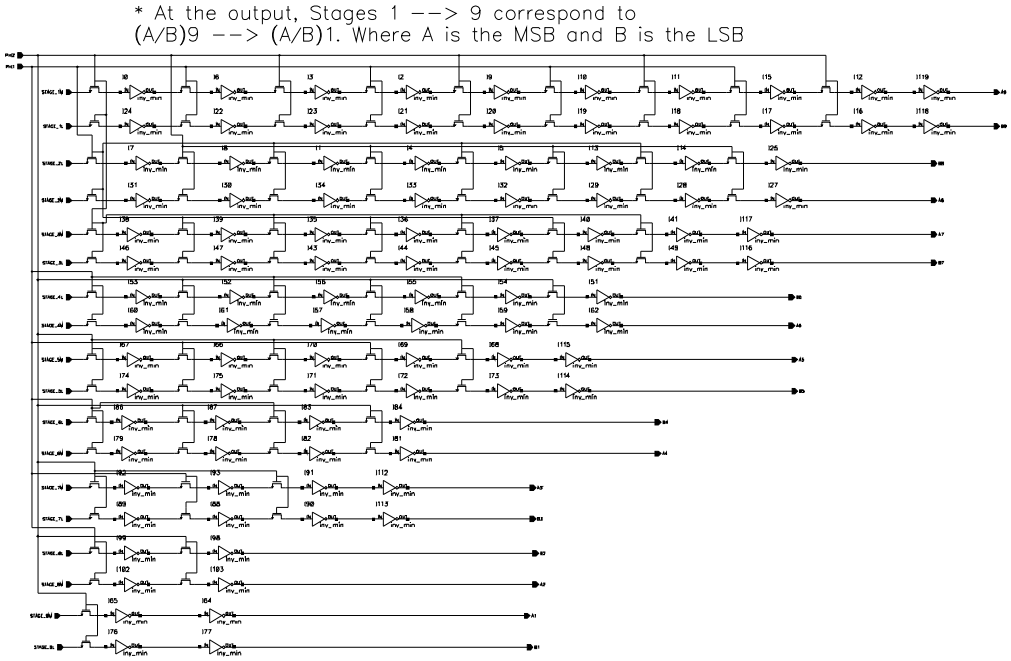

Figure A.23: Shift register block.

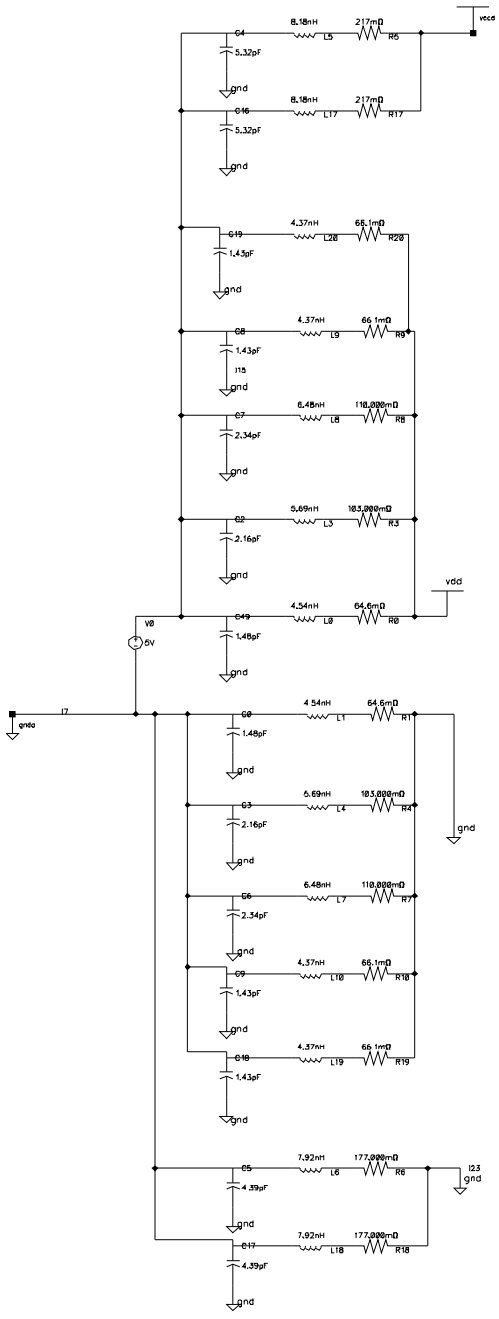

Figure A.24: Supply circuit used for testing ADC. Package pins are modeled.

Appendix B

Circuits - Physical Design

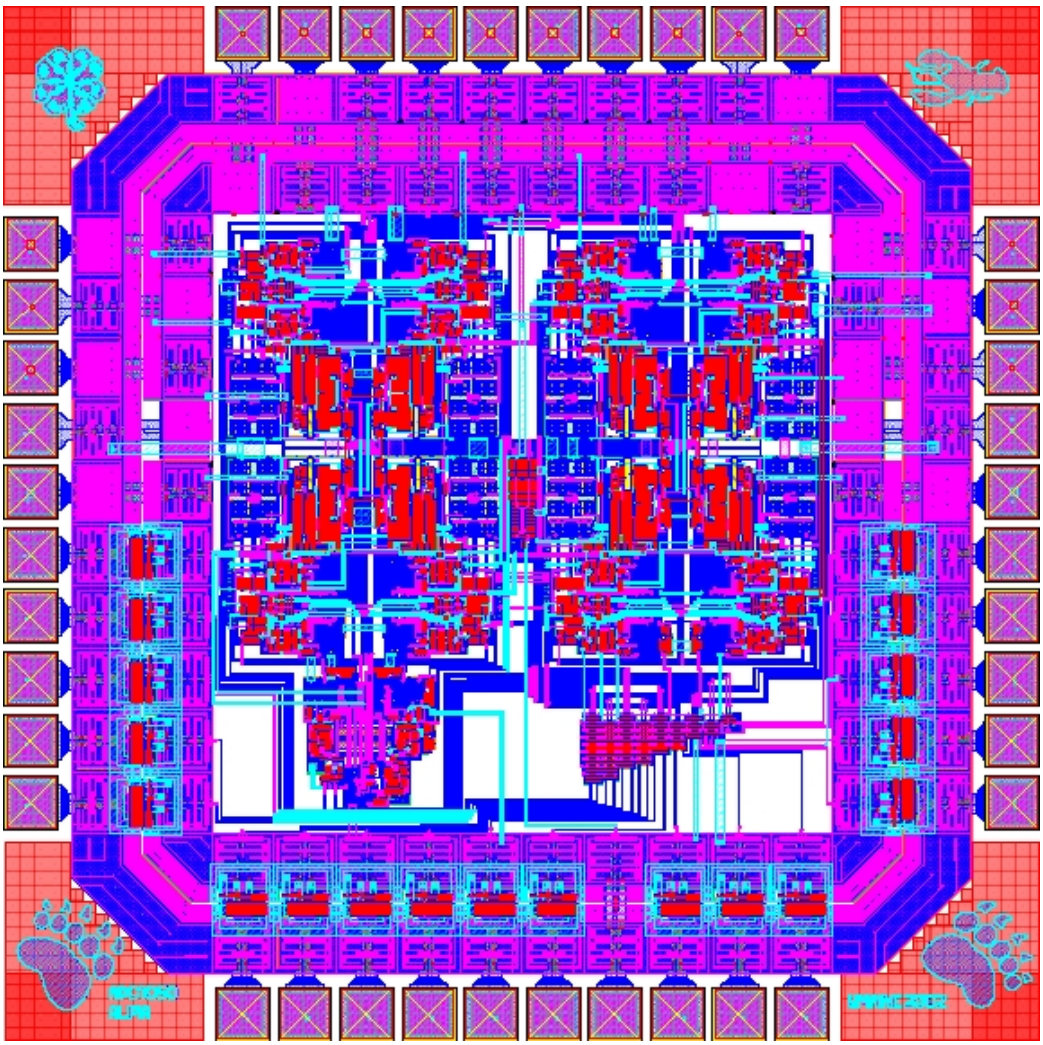

Figure B.1: Final Chip Layout.

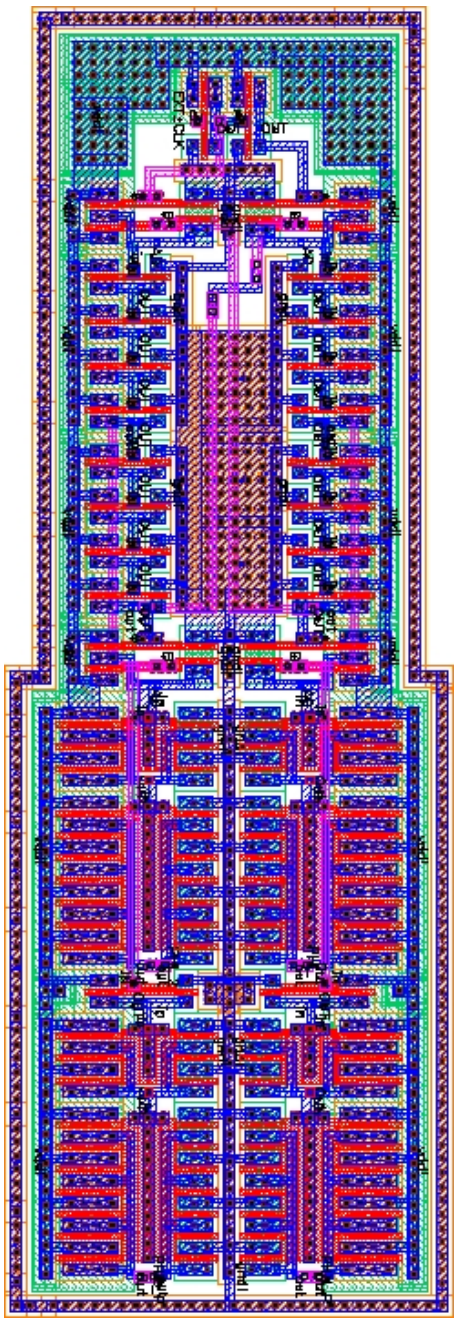

Figure B.2: Two phase non-overlapping clock layout.

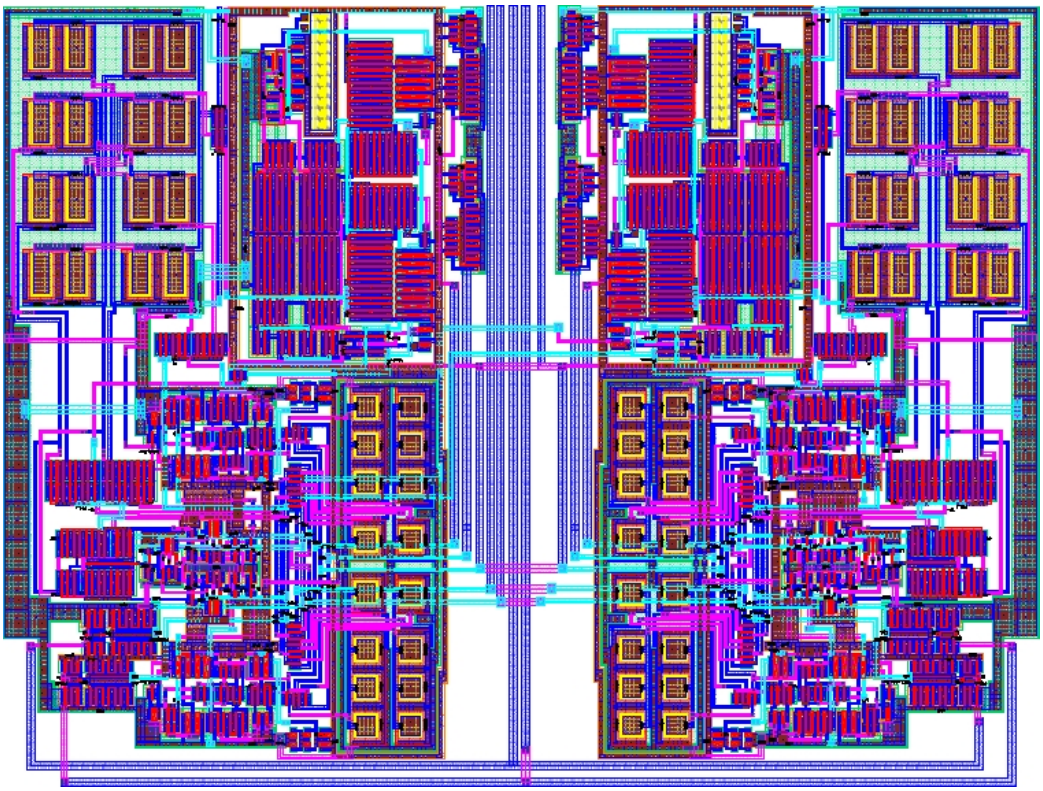

Figure B.3: Odd/Even stage layout.

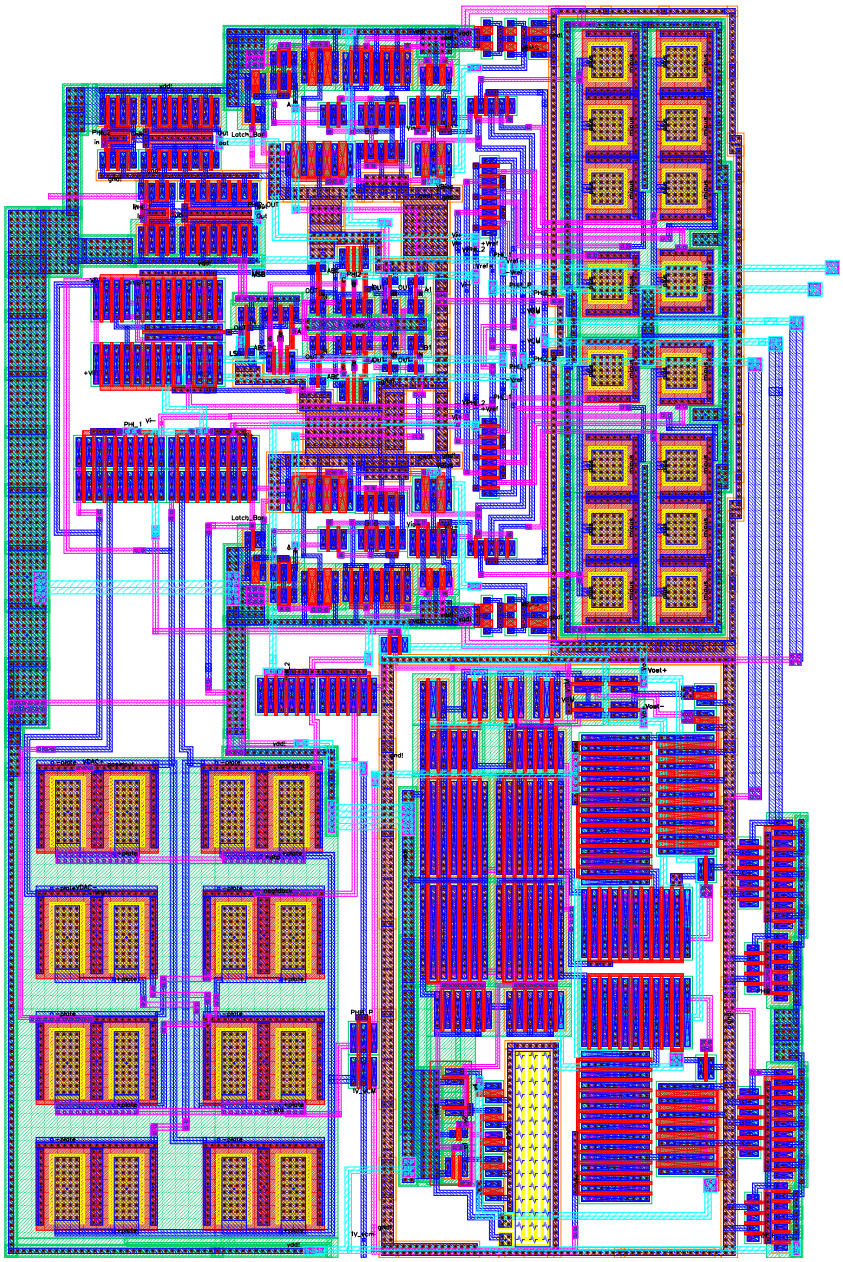

Figure B.4: Odd stage block layout.

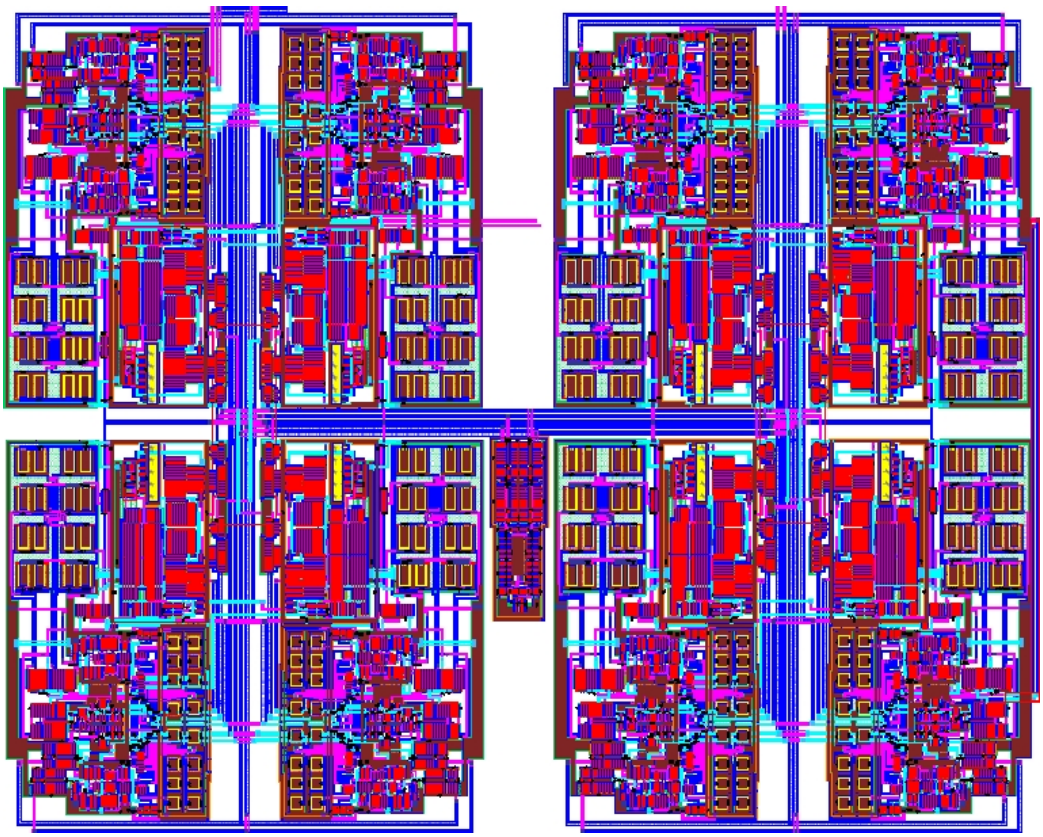

Figure B.5: Layout of the first 8 stages (Odd/Even).

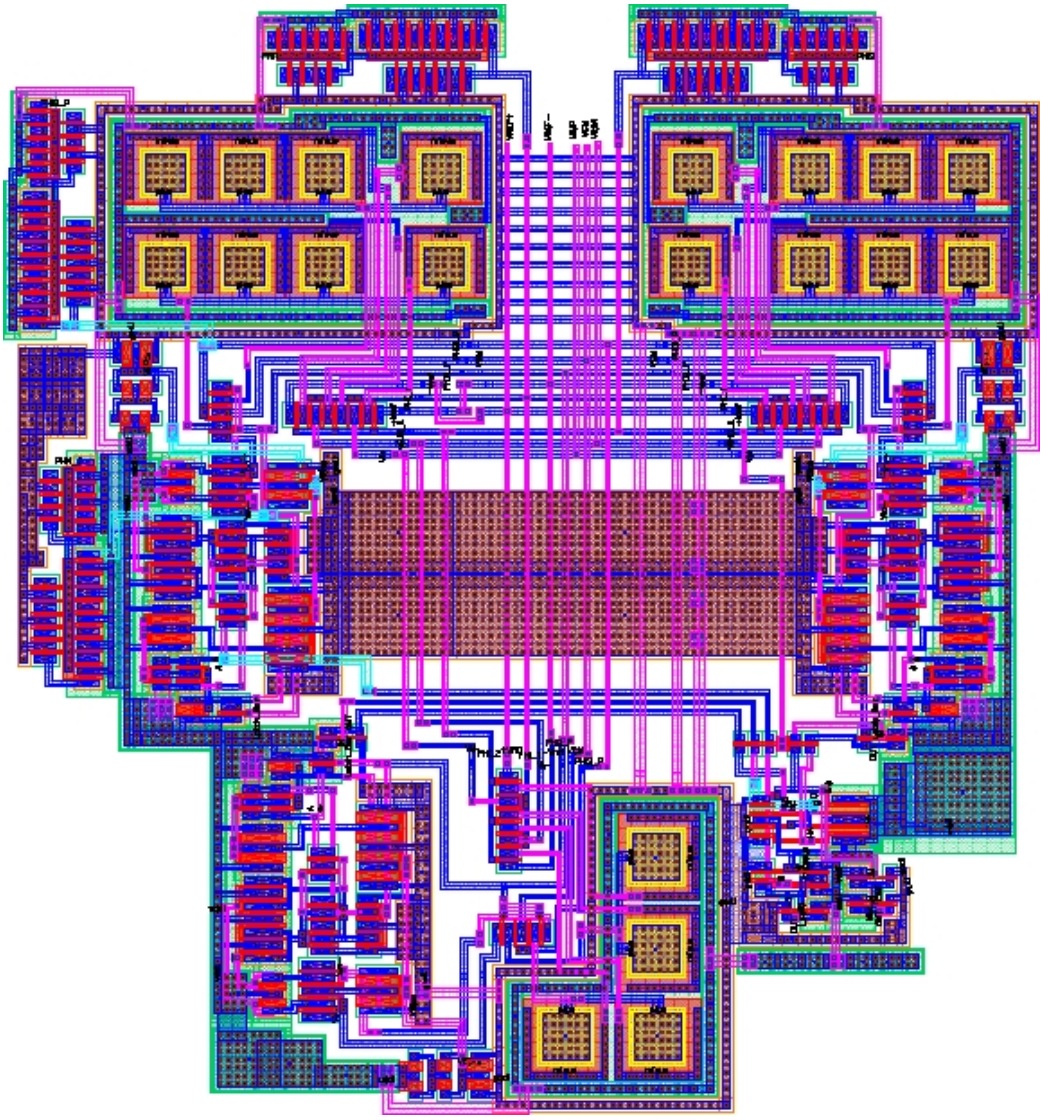

Figure B.6: Last stage layout.

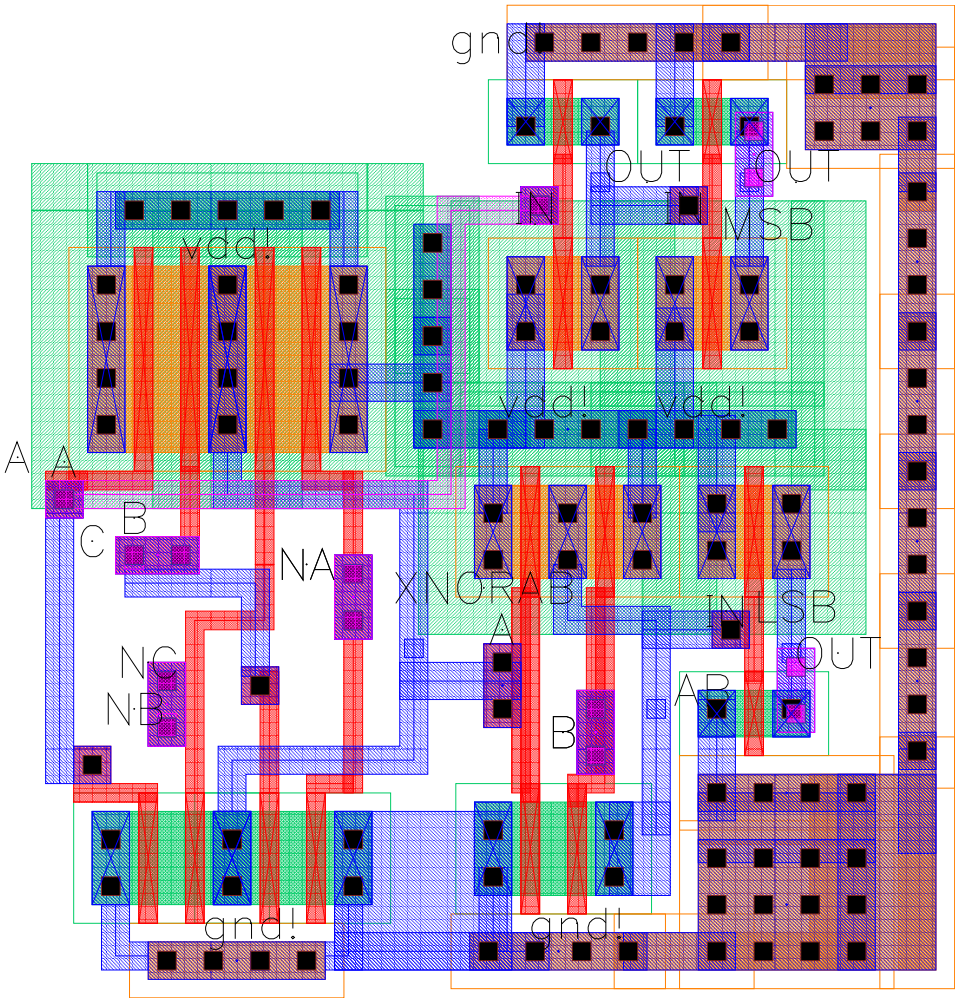

Figure B.7: Last stage logic layout.

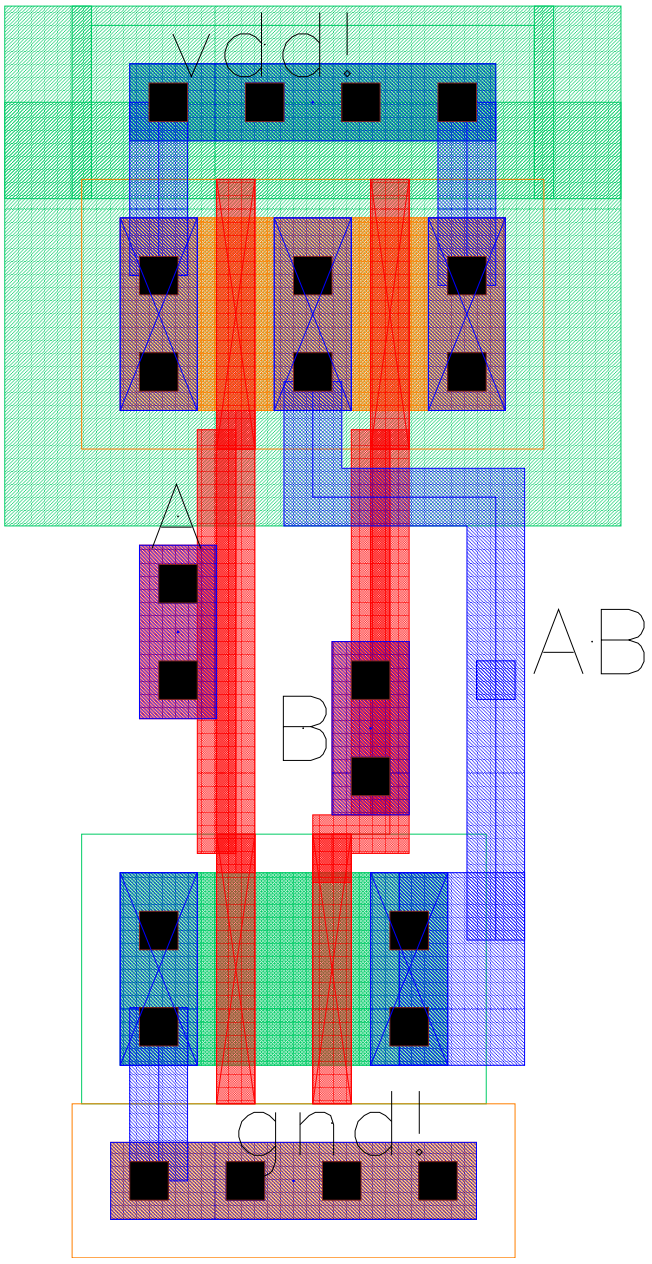

Figure B.8: 2-input NAND gate layout.

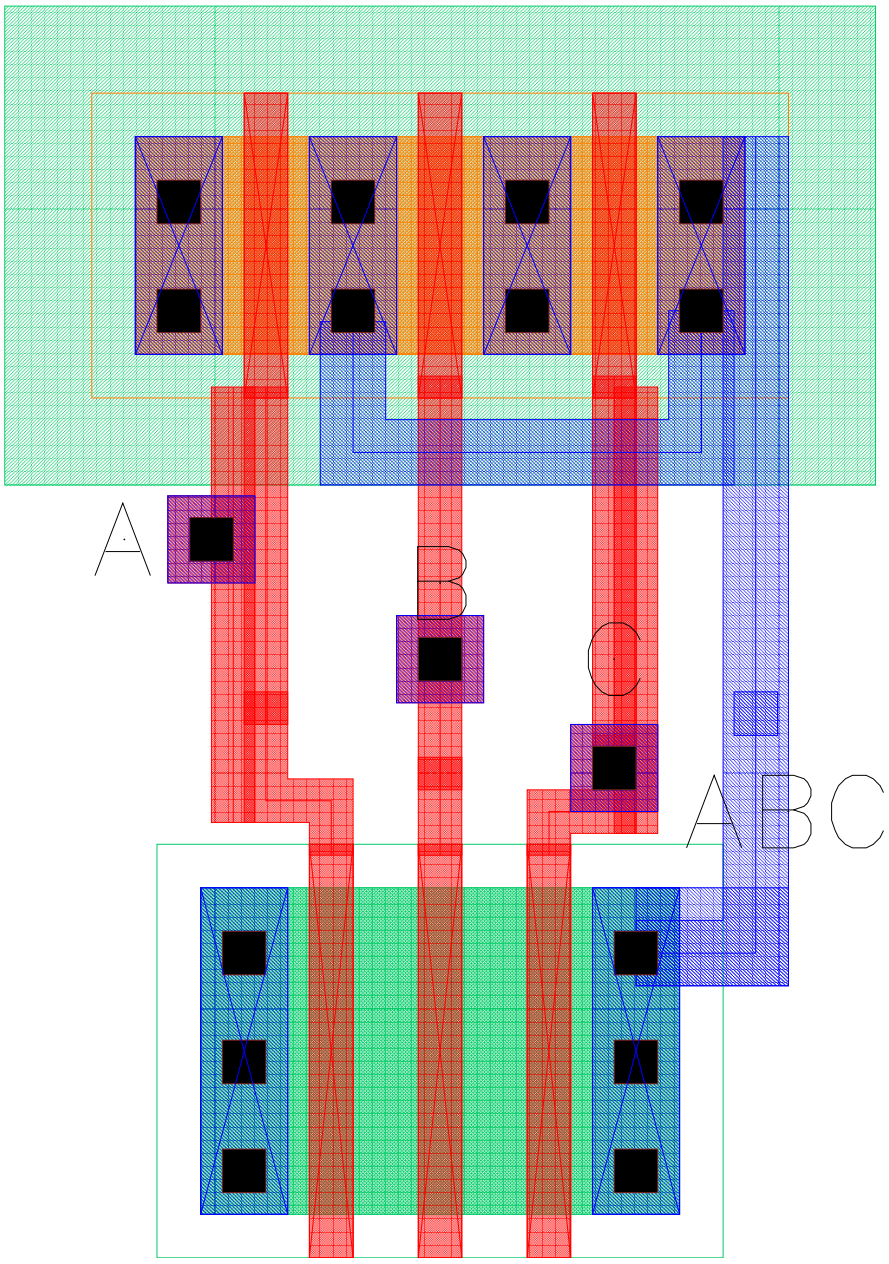

Figure B.9: 3-input NAND gate layout.

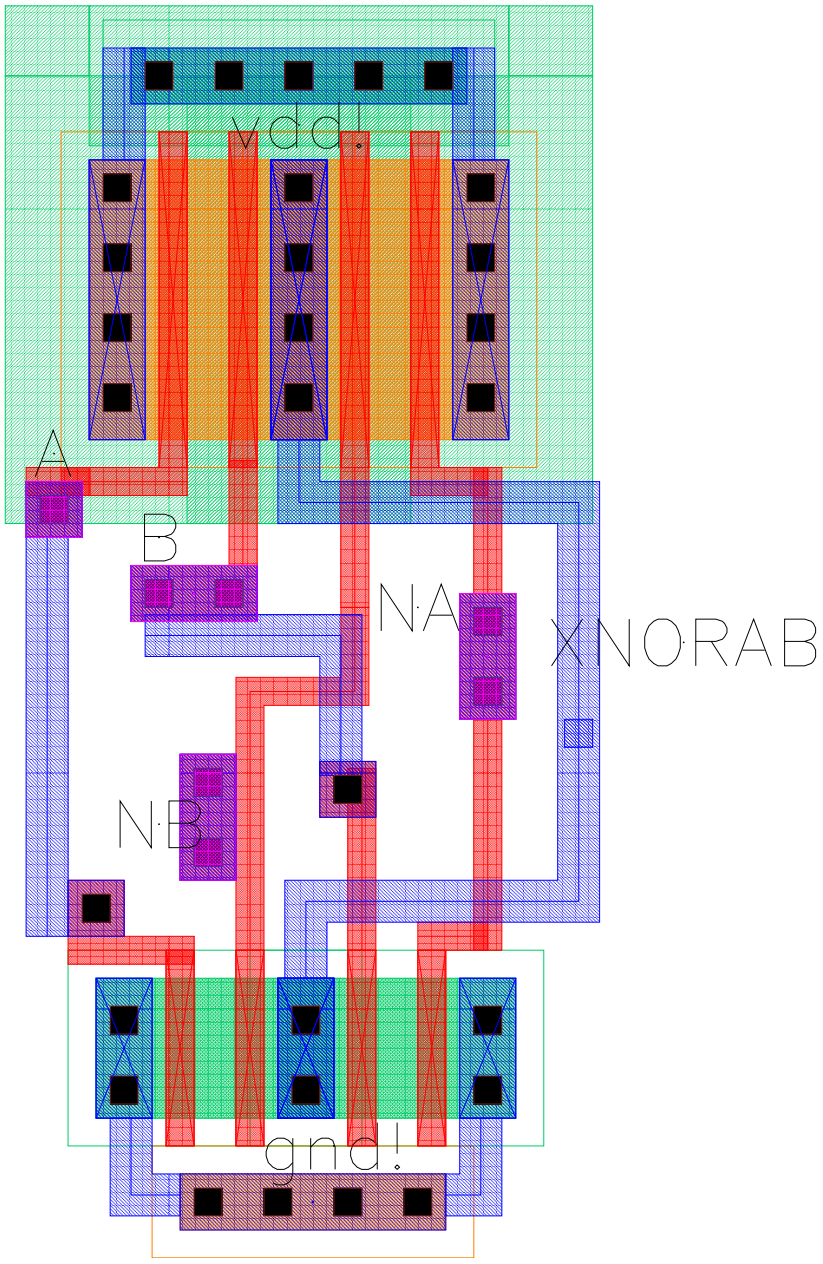

Figure B.10: Layout of the exclusive NOR.

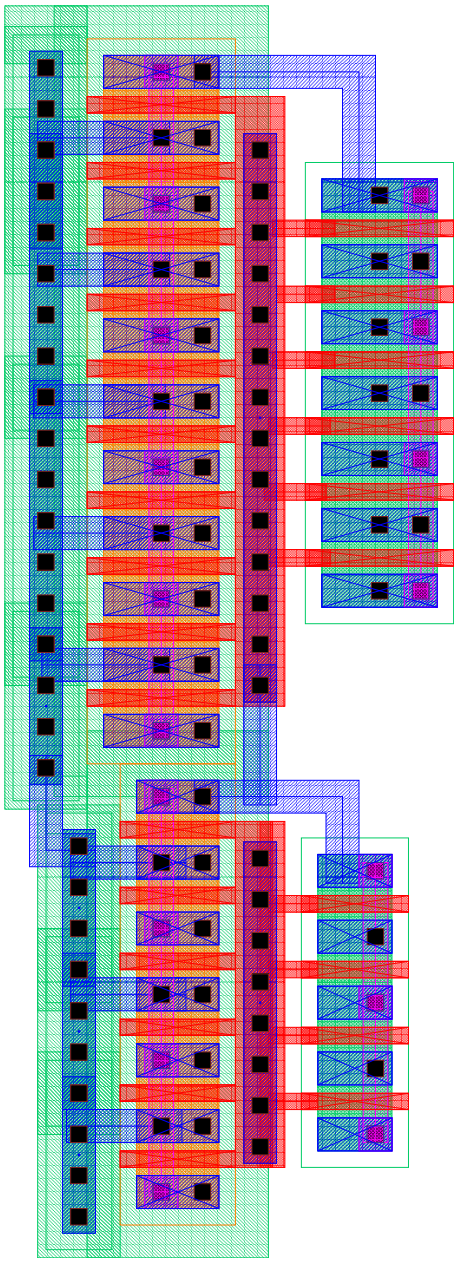

Figure B.11: 100fF buffer design layout.

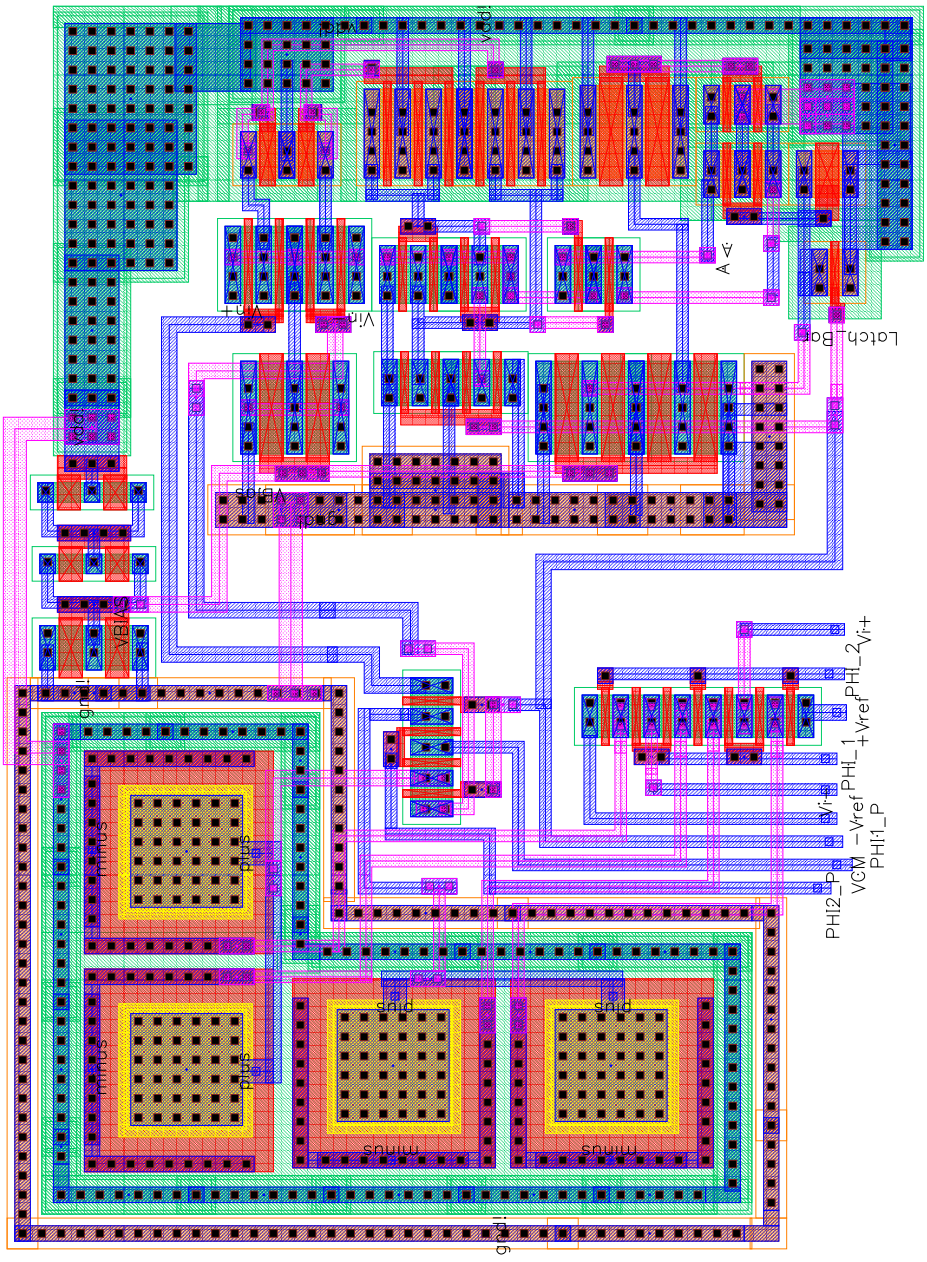

Figure B.12: Last stage differential comparator layout.

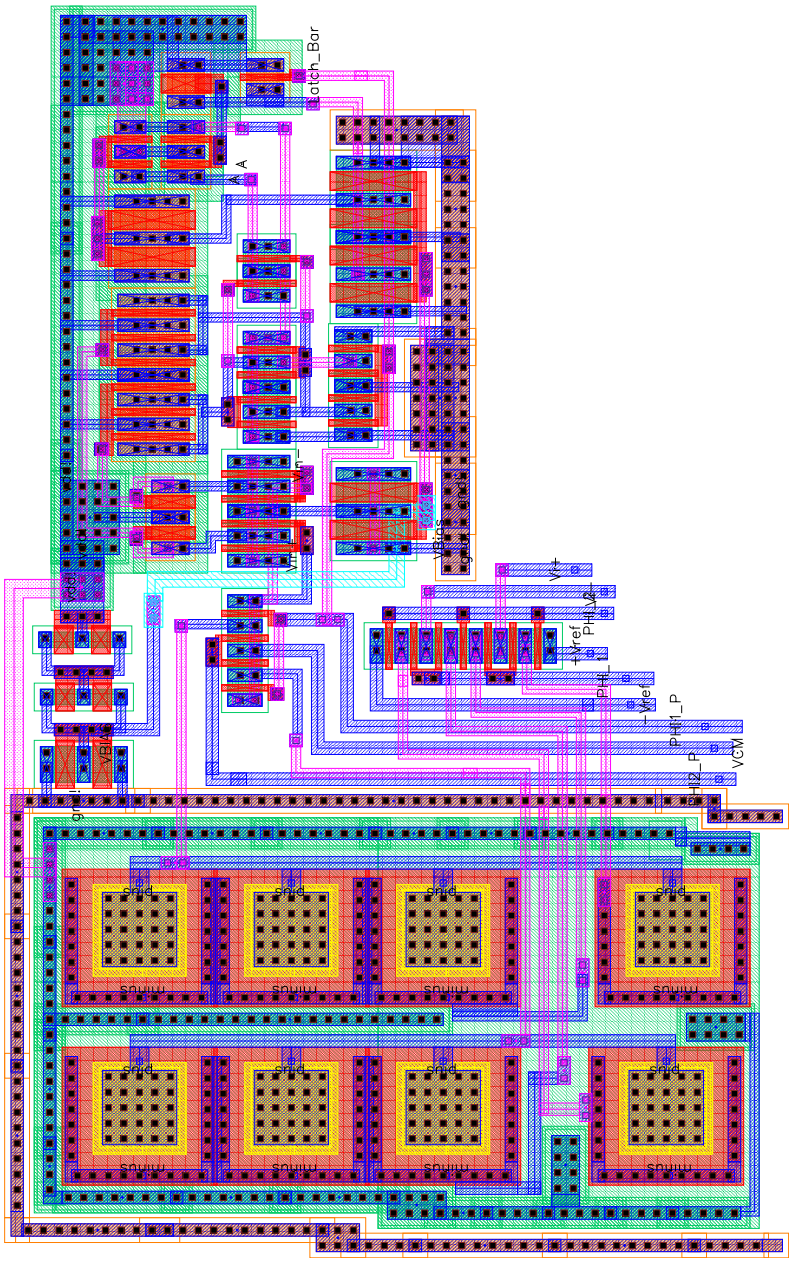

Figure B.13: Differential comparator layout (sub-ADC block).

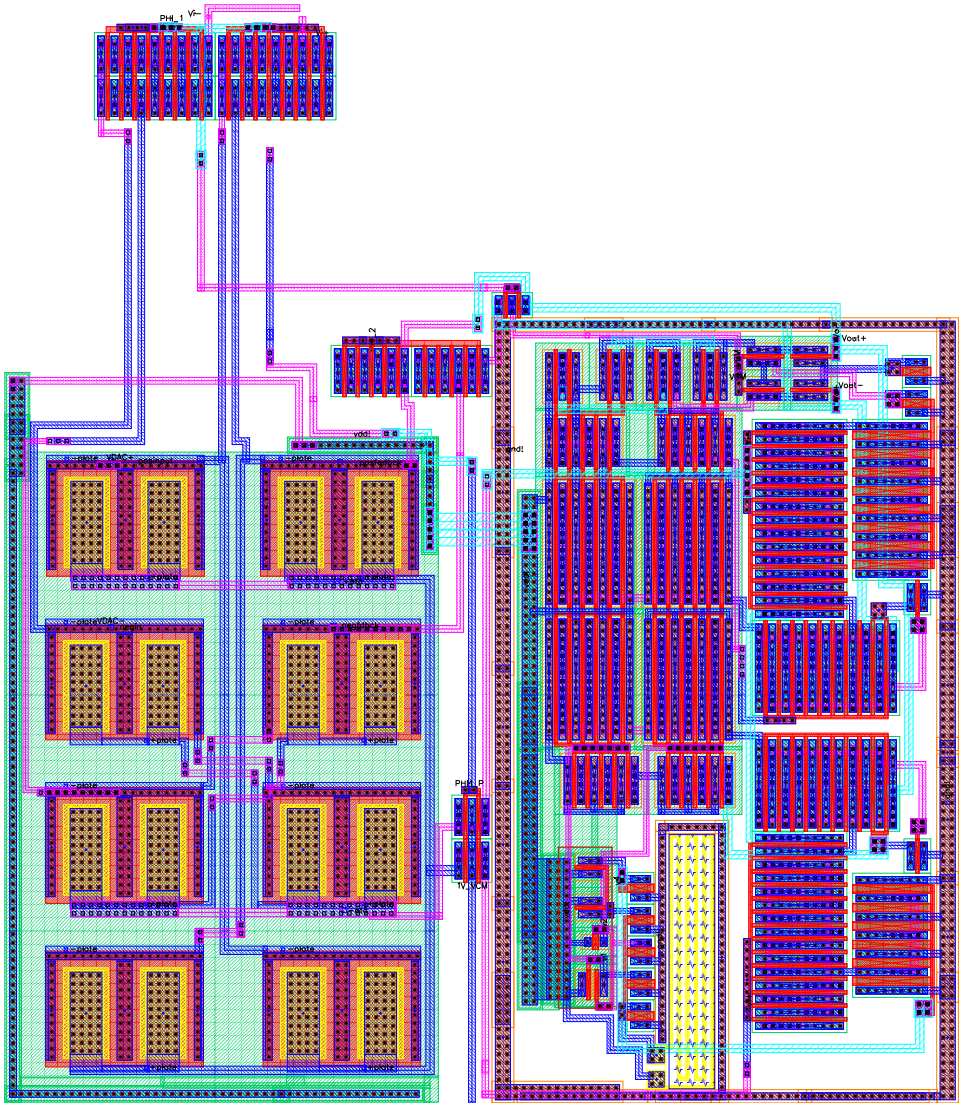

Figure B.14: Layout of gain stage block.

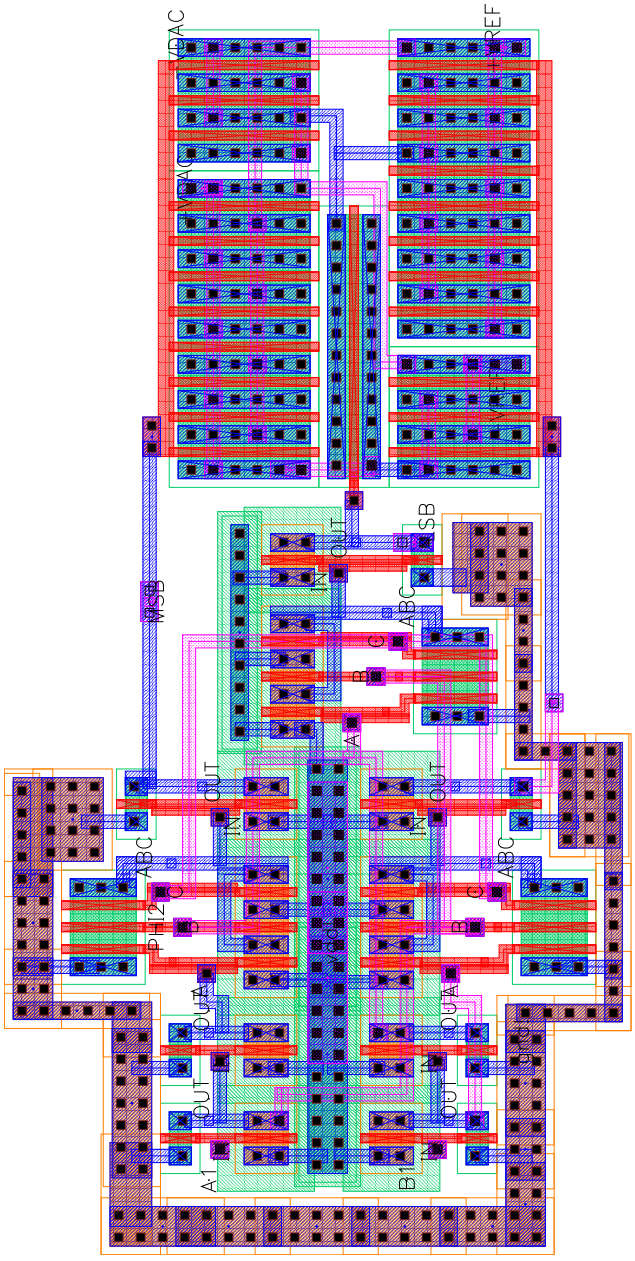

Figure B.15: Sub-DAC block layout.

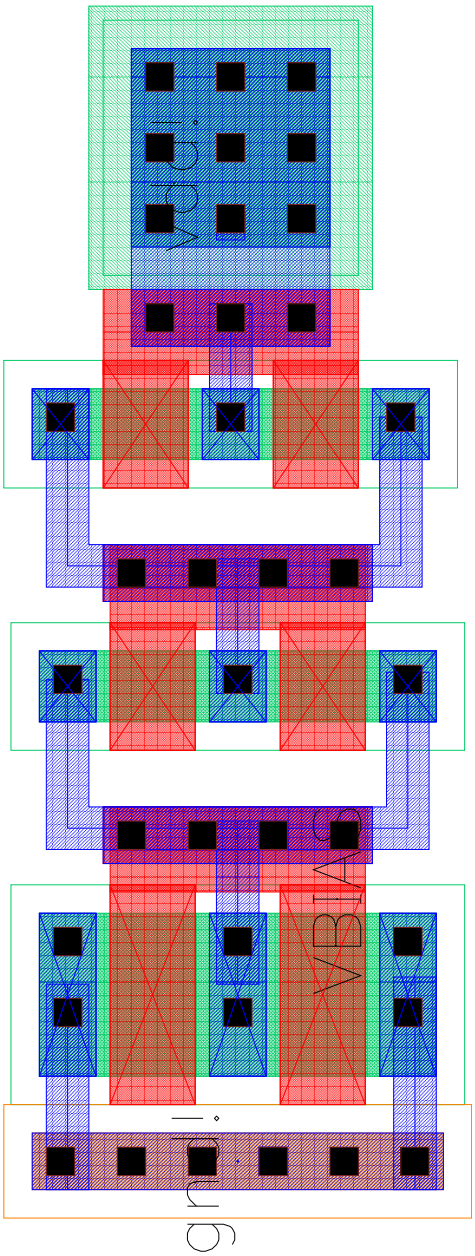

Figure B.16: Bias voltage circuit layout used in sub-ADC block.

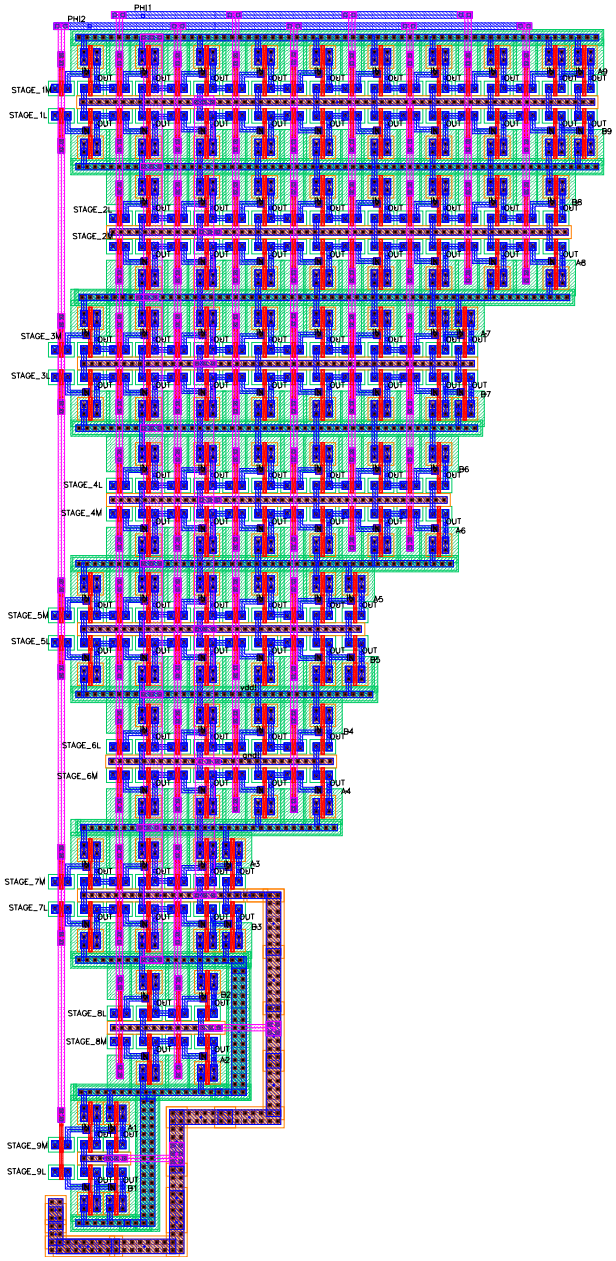

Figure B.17: Layout of the shift register.

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