Class-D Audio Power Amplifier with On-chip H-Bridge

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Abstract

There is always a push to create amplifiers that are more efficient. High efficiency translates to less power wasted, lower operating temperatures, and longer battery life in portable applications. For audio amplifiers, it is also imperative to have excellent sound quality by maintaining low distortion through the entire audio range.

This Class-D audio power amplifier achieves high efficiency while retaining exceptional sound quality, making it an outstanding audio power amplifier. It achieves high efficiency by using a pulse width modulation (PWM) scheme to convert the analog input into a stream of "pulses." These pulses control power transistors that allow current to flow through the load and turn the transistors either completely on or completely off keeping wasted energy to a minimum. There is very little audible distortion introduced by this Class-D audio power amplifier.

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Chapter 1
Introduction

1.1 Project Overview

Our VLSI design project is a Class-D audio amplifier that is used to convert small electrical signals into large ones while retaining a high efficiency.

The intended application of our amplifier is sound amplification. The Class-D audio amplifier receives an electrical signal from the output of a portable compact disc (CD) player or other audio device that would normally only be able drive a load such as headphones (150 Ω – 1000 Ω). Our project amplifies the electrical input signal so that it can drive smaller loads, such as an eight ohm speaker, with large currents to produce loud sounds. Throughout this text, we will assume the input to be an electrical audio signal.

Figure 1.1 below presents the overall block diagram of the Class-D audio amplifier.

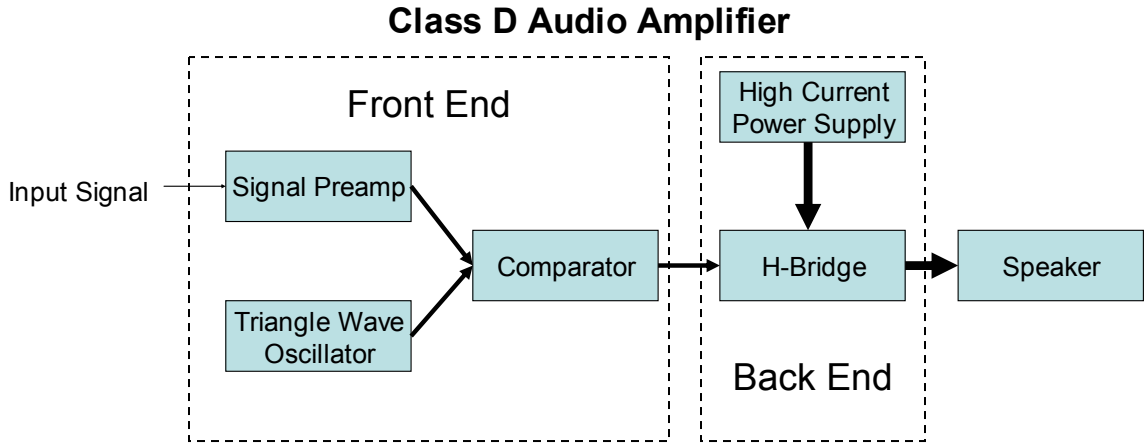

Figure 1.1 – Class-D Block Diagram

The input signal shown in Figure 1.1 is amplified by the signal preamplifier to control the volume of the output signal. The comparator compares the amplified input signal to a triangle wave oscillating at a constant frequency. The output of the comparator is either a "high" voltage or a "low" voltage. The "high" and "low" voltage levels at the output of the comparator control the power transistors in the H-bridge. When a "high" voltage level is sent from the comparator to the H-bridge, the high current power supply is directed by the H-bridge to drive the speaker with the current flowing in one direction. When a "low" voltage level is sent from the comparator to the H-bridge, the high current power supply is directed by the H-bridge to drive the speaker with the current flowing in the opposite direction. This constantly changing current through the load produces sound.

This text describes in detail the Class-D audio amplifier that we designed and built.

1.2 Project Specifications

Because this was the first VLSI design for both of the authors, specifications were relaxed. It was also beneficial for us to take up a Class-D Audio Amplifier because all components operate at relatively low frequencies (<200 kHz). Listed below are the specifications for our Class-D Audio Amplifier.

- Operates on ±2.5 V supply rails
- Utilizes a 5 bit volume control from 0 dB to -31 dB
- Operates on entire audio bandwidth (20 Hz – 20 kHz)
- Output will drive an 8 Ω speaker

1.3 Design Macros

A table listing all design macros used in our project appears below in Table 1.1.

Table 1.1 – Class-D Amplifier Design Macros

Macro Name	Macro Description
two_stage_diff_opamp	Wide swing differential input/output op-amp
OpAmp_Final OpAmp_Final_bias OpAmp_Final_amp	Wide swing single ended op-amp Bias circuit Amplifier circuit
Mux_2to1	2 to 1 Multiplexer
Mux_4to1 Mux_2 to 1	4 to 1 Multiplexer
Mux_8to1 Mux_2to1 Mux_4to1	8 to 1 Multiplexer
LineDriver Inv_2p7u_1p5u	ROM line driver circuit Standard inverter cell
VC_ROM Bit0 Bit1 S2G_1p12 S2G_1p25 S2G_1p4 S2G_1p58 S2G_1p77 S2G_1p99 S2G_1p23 S2G_1 S1G_p1 S1G_p2 S1G_p4 S1G_1	Volume control circuit Represents a zero bit Represents a one bit Bit pattern for stage 2 gain of 1.12 Bit pattern for stage 2 gain of 1.25 Bit pattern for stage 2 gain of 1.4 Bit pattern for stage 2 gain of 1.58 Bit pattern for stage 2 gain of 1.77 Bit pattern for stage 2 gain of 1.99 Bit pattern for stage 2 gain of 1.23 Bit pattern for stage 2 gain of 1 Bit pattern for stage 1 gain of 0.1 Bit pattern for stage 1 gain of 0.2 Bit pattern for stage 1 gain of 0.4 Bit pattern for stage 1 gain of 1
volctrl VC_ROM Line_Driver	Volume control circuit Volume control ROM circuit ROM line driver circuit
VC_preamp2 volctrl Mux_2to1 Mux_4to1 Mux_8to1 two_stage_diff_opamp OpAmp_Final	Volume control preamp circuit Volume control circuit 2 to 1 Multiplexer 4 to 1 Multiplexer 8 to 1 Multiplexer Wide swing differential input/output op-amp Wide swing single ended op-amp
Triangle_wave_2 OpAmp_FINAL	Triangle Wave Generator circuit Wide swing single ended op-amp
Comparator	Comparator circuit
Invertor	H-Bridge delay inverter
H_BRIDGE_DELAY Delay_buffer Inv_buffer4	H-Bridge delay circuit H-Bridge delay buffer H-Bridge final delay buffer
H_Bridge	H-Bridge circuit

1.3 Pin Out

A pin out table for our Class-D Audio amplifier appears on the next page in Table 1.2. Supply nets were assigned to pins with the highest parasitic capacitances. This allows for small bypass capacitors to squelch voltage transients. The critical signals were assigned to pins with the least amount of parasitics. For the ground signal, three pins were used. This puts the resistive and inductive parasitics in parallel which greatly reduces them. The capacitive parasitics are increased when in parallel, but this does not negatively affect our ground signal. Four pins were used for both the Vdd and Vss nets which supply the H-Bridge. This was done to provide adequate current to the H-Bridge. Lastly, four pins were used for each of the H-Bridge outputs. Again, this will reduce the current in each pin to a "safe" value.

It's important to note that we split the guard rings in order to have separate Vdd supplies for the front and back ends. In order to do this we couldn't use pins 1 and 20. Therefore there are no attachments to these pins.

Table 1.2 – Class-D Amplifier Pin Out

Pin	Pad Type	Pin Name	Description
1	-	-	No connect
2	padnc	-	No connect
3	padnc	-	No connect
4	padnc	-	No connect
5	padnc	-	No connect
6	padnc	-	No connect
7	padnc	-	No connect
8	padgnd	gnd!	Ground pin (1 of 3)
9	padgnd	gnd!	Ground pin (1 of 3)
10	padgnd	gnd!	Ground pin (1 of 3)
11	padaref	IN	Input Signal
12	padnc	-	No connect
13	padnc	-	No connect
14	padvdd	vdd!	Front end vdd
15	padio	A0	Volume bit 0
16	padio	A1	Volume bit 1
17	padio	A2	Volume bit 2
18	padio	A3	Volume bit 3
19	padio	A4	Volume bit 4
20	-	-	No connect
21	padvdd1	vdd1!	Back end vdd (1 of 4)
22	padvdd1	vdd1!	Back end vdd (1 of 4)
23	padnc	-	No connect
24	padvss1	vss!	Front/Back end vss (1 of 4)
25	padvss1	vss!	Front/Back end vss (1 of 4)
26	padnc	-	No connect
27	padio1	Out	+ H-Bridge Output (1 of 4)
28	padio1	Out	+ H-Bridge Output (1 of 4)
29	padio1	Out	+ H-Bridge Output (1 of 4)
30	padio1	Out	+ H-Bridge Output (1 of 4)
31	padio1	Out’	- H-Bridge Output (1 of 4)
32	padio1	Out’	- H-Bridge Output (1 of 4)
33	padio1	Out’	- H-Bridge Output (1 of 4)
34	padio1	Out’	- H-Bridge Output (1 of 4)
35	padnc	-	No connect
36	padvss1	vss!	Front/Back end vss (1 of 4)
37	padvss1	vss!	Front/Back end vss (1 of 4)
38	padnc	-	No connect
39	padvdd1	vdd1!	Back end vdd (1 of 4)
40	padvdd1	vdd1!	Back end vdd (1 of 4)

Chapter 2
Circuit Design

2.1 Fully Differential Operational Amplifier

In order to maximize the dynamic range of the Class-D amplifier, we utilize a fully differential wide swing op-amp taken from Banu, etc [1]. The chosen two-stage amplifier produces a large output swing, sufficient bandwidth, the capability of driving resistive loads, and relatively low power dissipation. Furthermore, the circuit can be operated on a ± 2.5 V power supply with a quiescent voltage of 0 V. All of these make this op-amp an ideal choice for our design.

The differential op-amp is separated into two components, the amplification stages and the bias stage. The amplification stage contains a differential-mode input stage, common-mode feedback circuitry, and an output stage. The sizing of the transistors was reduced so that the minimum length of the process was used. To do this, all transistors were reduced by 10/3 of their original size. The bias circuit was taken from Baker [2] page 657 with minor modifications. Its function is to establish a bias current of 10 μA that is mirrored throughout the op-amp. The schematic of the fully differential operational amplifier is shown in Figure 2.1.

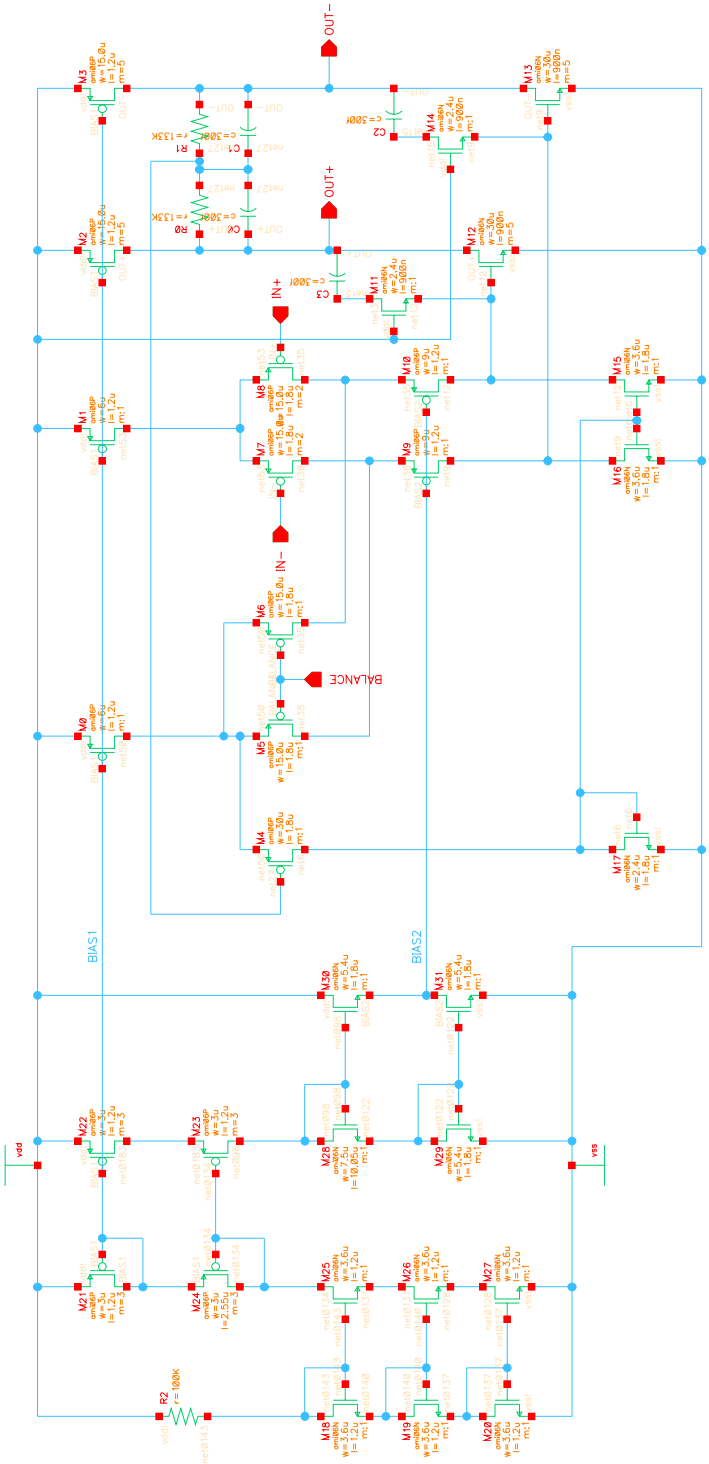

Figure 2.1 – Fully Differential Operational Amplifier Schematic

2.2 Multiplexers (Mux_2to1, Mux_4to1, Mux_8to1)

TX_Gate

This is a transmission gate designed to pass or reject analog signals depending on the logical value of the select line. It is a standard transmission gate using both P-type and N-type transistors. This gate can be seen in Figure 13.8 of Baker [2] on page 261; the schematic is shown below in Figure 2.2.

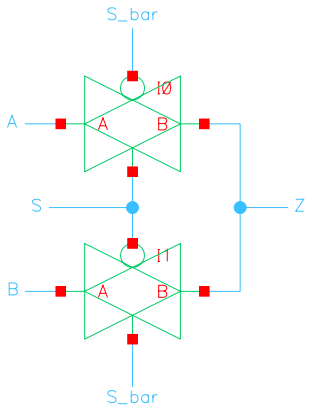

Figure 2.2 – Transmission Gate Schematic

Mux_2to1

The design for the multiplexers was taken from Baker [2] page 260. The 2 to 1 mux/demux is used for analog signals and is the standard TX_Gate cell. When the selector signal S is high, A is passed to the output. Likewise, when S is low, B is passed to the output.

Mux_4to1

This is an analog 4 to 1 mux/demux. It uses two 2 to 1 multiplexers fed into another 2 to 1 multiplexor. This configuration is shown in Figure 2.3. The logical values of the selection lines S[0] and S[1] determine which input is passed. For example if S[0]=*low* and S[1]=*low*, then IN[0] is passed. Also if S[0]=*low* and S[1]=*high*, then IN[1] is passed, if S[0]=*high* and S[1]=*low*, then IN[2] is passed, and if S[0]=*high* and S[1]=*high*, then IN[3] is passed.

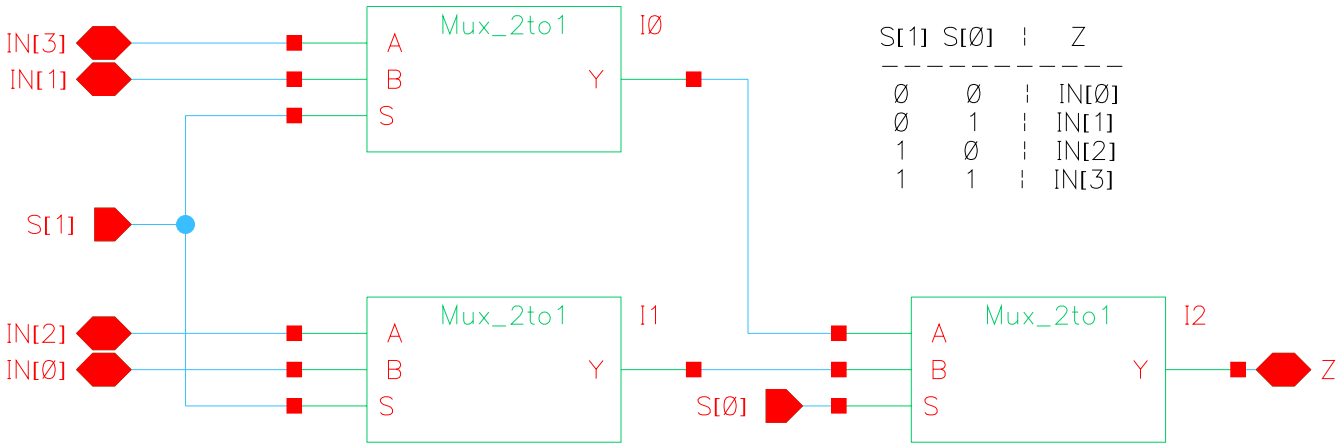

Figure 2.3 – 4 to 1 Multiplexer Schematic

Mux_8to1

This is an 8 to 1 analog mux/demux. It uses two 4 to 1 multiplexers fed into another 2 to 1 multiplexer. This configuration is shown below in Figure 2.4. The logical values of the selection lines S[0], S[1], and S[2] determine which of the eight input signals is passed. For example, if S[0]=*low*, S[1]=*low*, and S[2]=*low* then IN[0] is passed. The rest of the logic can be shown easily.

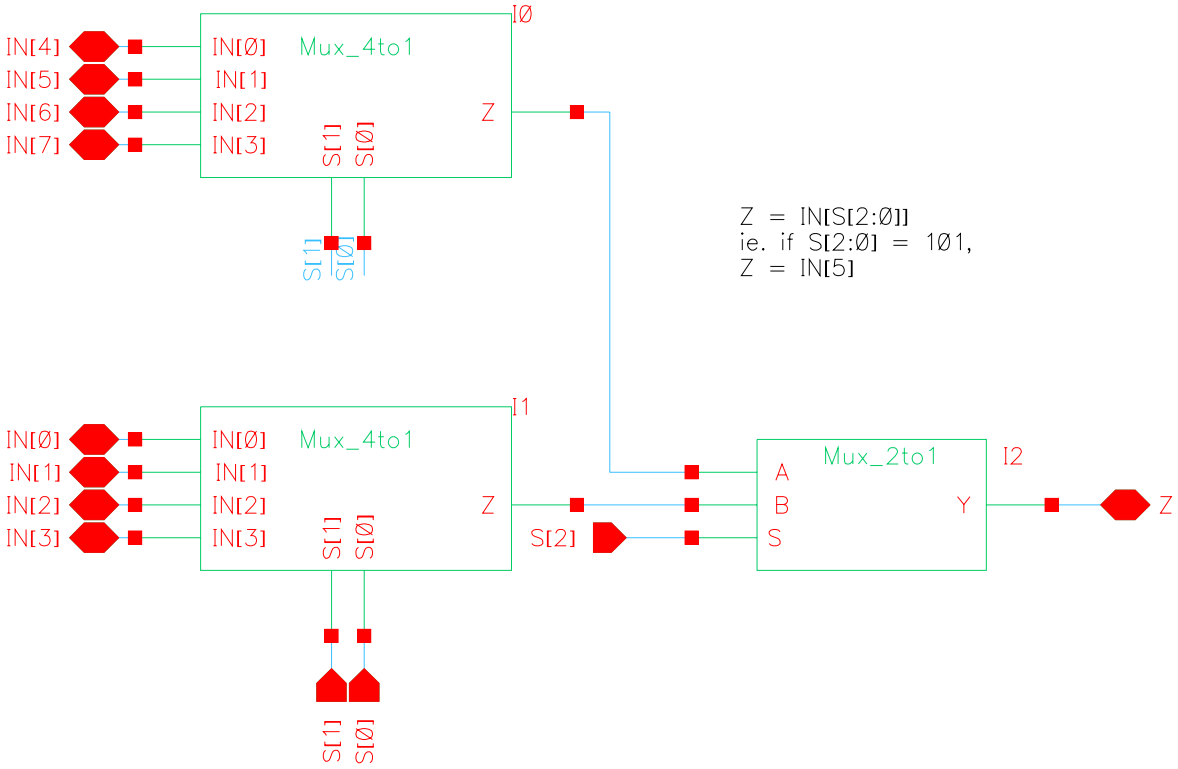

Figure 2.4 – 8 to 1 Multiplexer Schematic

2.3 Volume Control Logic

Volctrl

The volume control logic uses a ROM which was designed by Steven Turner and was used because of the easiness in changing the combinational logic. The volctrl circuit is shown in Figure 2.5, and its function is to drive the multiplexers in the preamp circuit. It accepts a five input digital volume control selection and outputs six multiplexer-driving signals. There are two components of the ROM, the Line_Driver and the VC_ROM. The Line_Driver accepts the five input digital volume control signal and selects and drives the appropriate line from the possible 32 ROM lines. The VC_ROM contains arrays of 1's and 0's that determine the appropriate logic levels for the multiplexer-driving outputs.

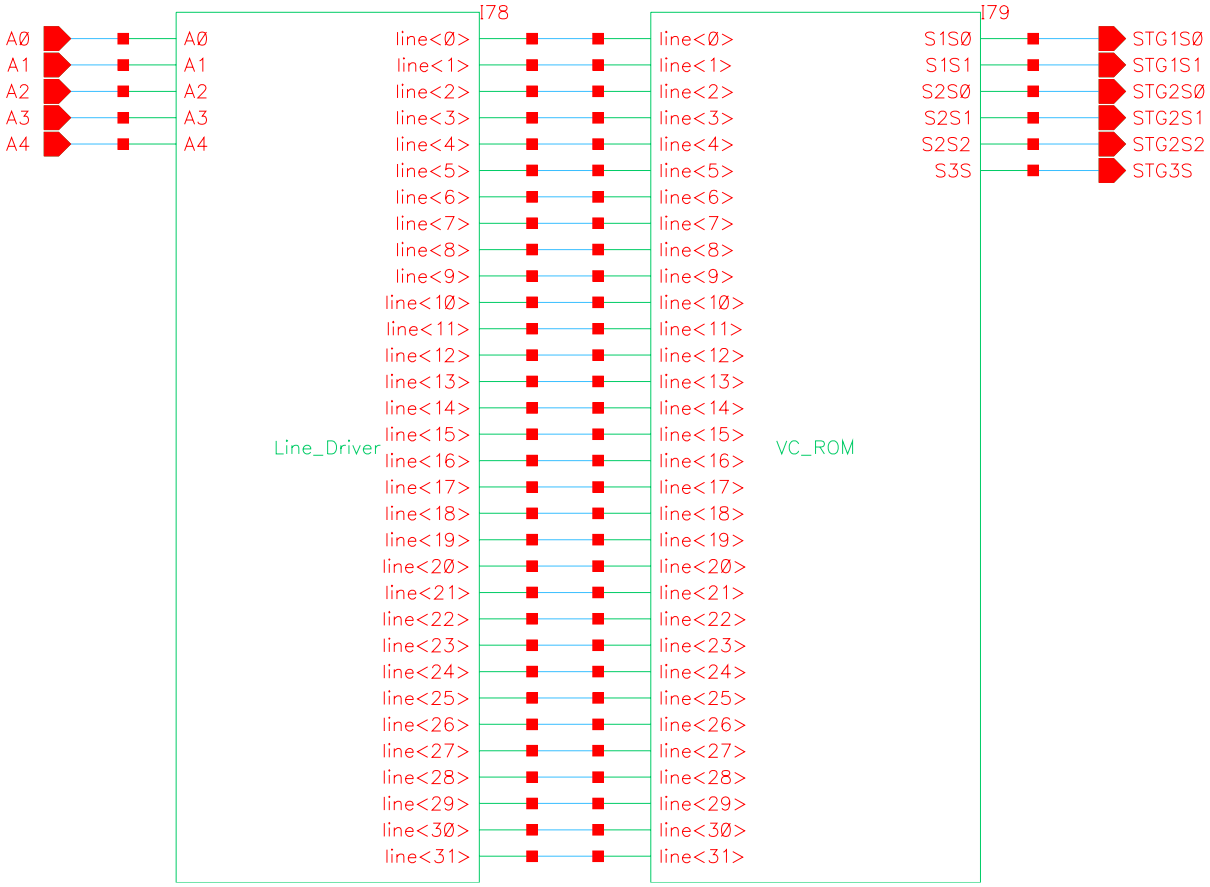

Figure 2.5 – Volume Control Schematic

Line_Driver

The Line_Driver selects and drives the appropriate line in the VC_ROM. It uses a tree decoder method described in Baker [2] page 341-343. A pull-down NMOS is used to pull the output of the VC_ROM low when that particular line is not selected. This ensures that all decoder outputs are low except for the line that is selected. Two inverters are then used to regenerate the signal and drive the line capacitances. The switching point voltage of the first inverter (-1 V) is set to compensate for the threshold drop across the pass transistor. The tree decoder consists of NMOS pass gates with the common row end tied to VDD. The configuration in Figure 2.6 is an expansion of Baker's tree on page 342 to allow for five inputs and 32 outputs.

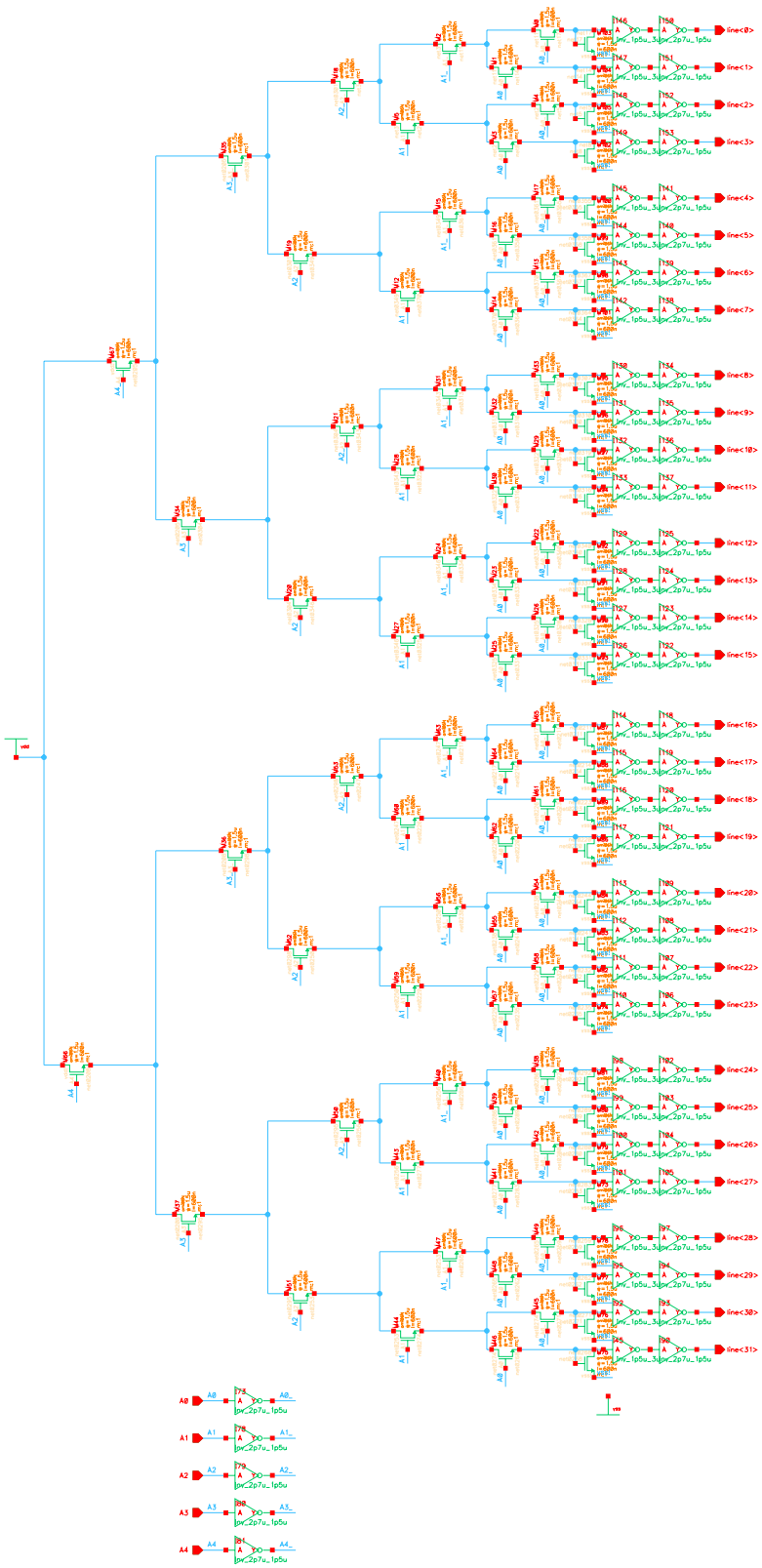

Figure 2.6 – Line Driver Schematic

VC_ROM

The VC_ROM circuit seen in Figure 2.7 is driven by the Line_Driver, and it drives the multiplexer select lines in the volume control preamp circuit. The output select lines consist of a PMOS tied to GND as a weak pull-up. The true output is buffered using two inverters in series. The switching point voltage of the first inverter is again set to -1 V. With this configuration, the line is high unless it is pulled low by the array combinational logic. To pull the line low, an NMOS is connected to the line which corresponds to an enabled Bit0 cell in the array path. It is important to note that the Line_Driver cell only allows one row to be driven at a time. Also the bits are either not connected for a Bit1, or have an enabled NMOS pull-down for a Bit0 *(see Bit0 and Bit1 sections)*.

Power dissipation was also a concern in this design. To minimize power, the weak pull-up was connected to GND instead of VDD. The VC_ROM bit pattern had to be slightly modified from Steven's configuration because we used a differential op-amp.

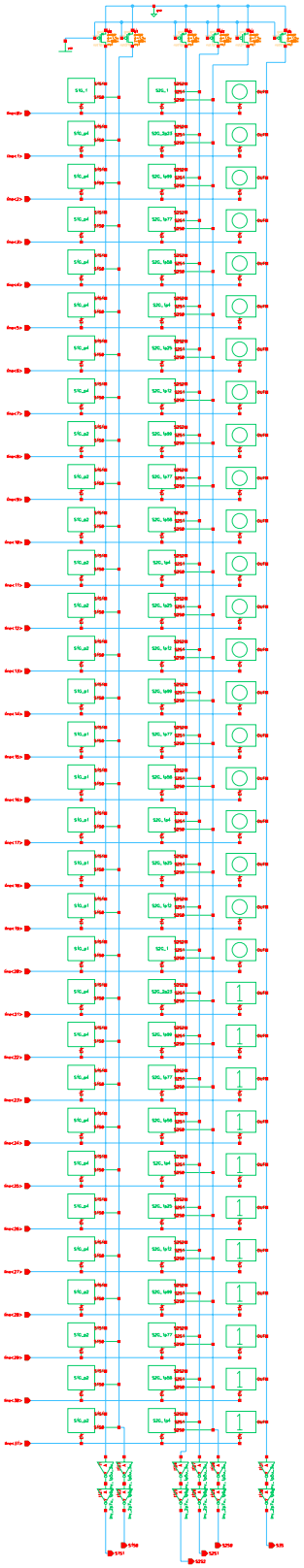

Figure 2.7 – Volume Control ROM Schematic

Bit0

The Bit0 cell represents a zero bit in the ROM. It is made up of an NMOS that pulls the line low when enabled. This is shown below in Figure 2.8.

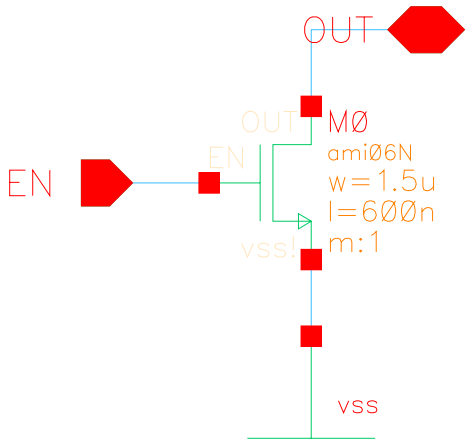

Figure 2.8 – Bit 0 Schematic

Bit1

The Bit1 cell represents a one bit in the ROM. It is made up of a simple open connection to ensure that the ROM line will be pulled high. This is shown below in Figure 2.9.

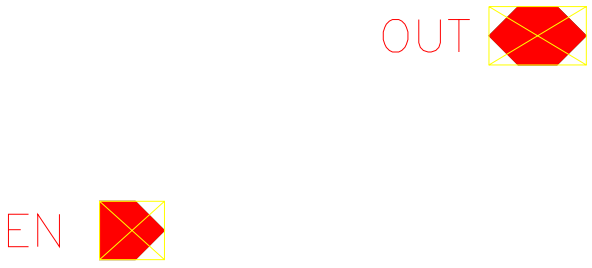

Figure 2.9 – Bit 1 Schematic

2.4 Volume Control Pre-Amplifier

The VC_preamp circuit shown in Figure 2.10 provides volume control for the Class-D Amplifier by adjusting the level of the input signal before it is fed into the comparator. It accepts an analog input signal and a five input digital volume control signal and outputs an analog amplified version of the input signal. The preamp circuit provides 32 levels of attenuation in 1 dB increments from 0 dB to -31 dB. In order to get these levels, a three gain stage configuration was used. Table 2.1 shows the scheme we used to obtain the desired gains.

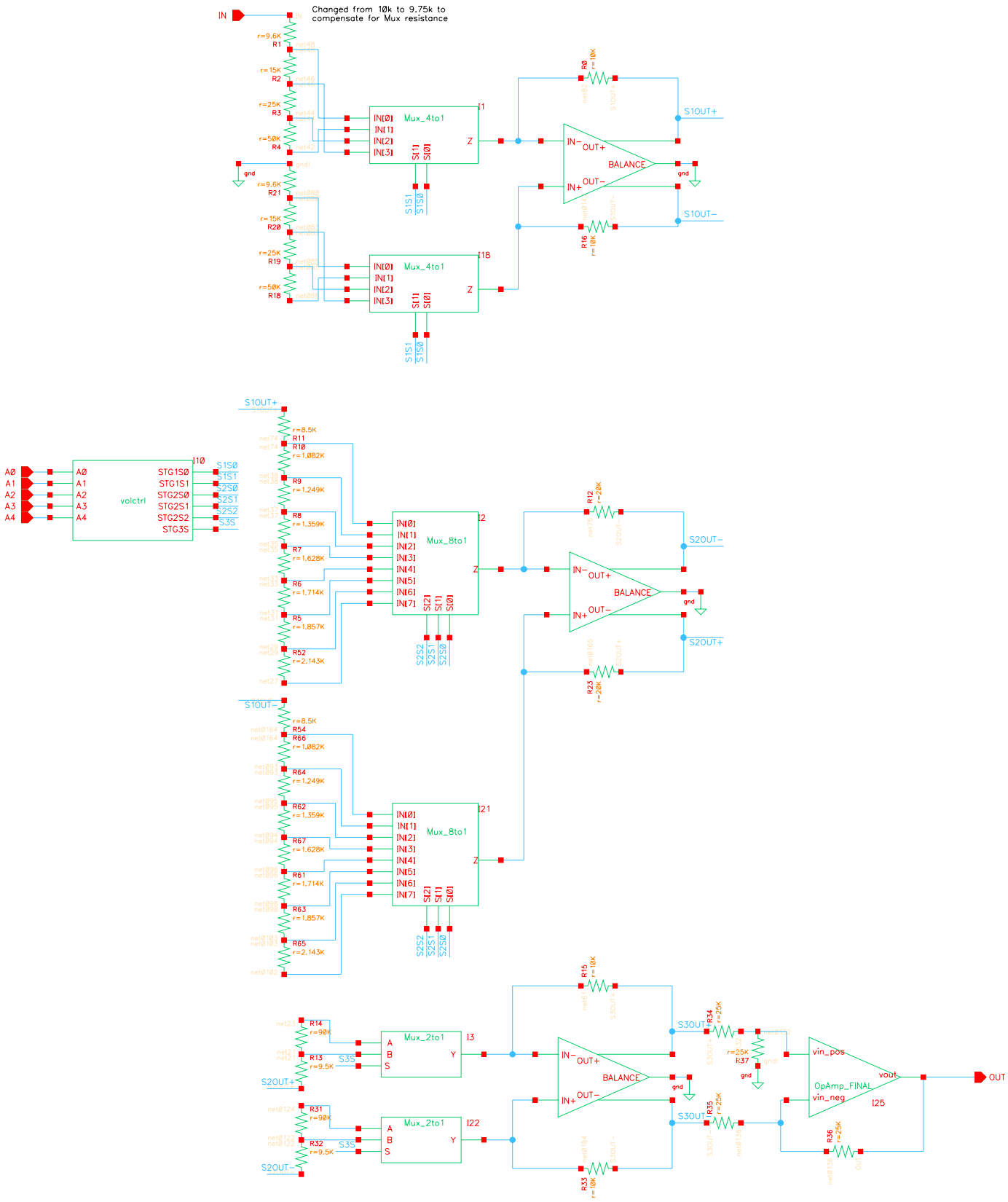

Figure 2.10 – Volume Control Preamplifier Schematic

Table 2.1 – Volume Control Preamplifier Gains

INPUT	DESIRED GAIN (dB)	STAGE 1 GAIN (V/V)	STAGE 2 GAIN (V/V)	STAGE 3 GAIN (V/V)	OBTAINED GAIN (dB)
00000	0	-1	1	-1	0
00001	-1	-0.4	2.25	-1	-0.91515
00010	-2	-0.4	2.00	-1	-1.9382
00011	-3	-0.4	1.78	-1	-2.9504
00100	-4	-0.4	1.59	-1	-3.93086
00101	-5	-0.4	1.41	-1	-4.97442
00110	-6	-0.4	1.26	-1	-5.95139
00111	-7	-0.4	1.12	-1	-6.97444
01000	-8	-0.2	2.00	-1	-7.9588
01001	-9	-0.2	1.78	-1	-8.971
01010	-10	-0.2	1.59	-1	-9.95146
01011	-11	-0.2	1.41	-1	-10.995
01100	-12	-0.2	1.26	-1	-11.972
01101	-13	-0.2	1.12	-1	-12.995
01110	-14	-0.1	2.00	-1	-13.9794
01111	-15	-0.1	1.78	-1	-14.9916
10000	-16	-0.1	1.59	-1	-15.9721
10001	-17	-0.1	1.41	-1	-17.0156
10010	-18	-0.1	1.26	-1	-17.9926
10011	-19	-0.1	1.12	-1	-19.0156
10100	-20	-0.1	1	-1	-20
10101	-21	-0.4	2.25	-0.1	-20.9151
10110	-22	-0.4	2.00	-0.1	-21.9382
10111	-23	-0.4	1.78	-0.1	-22.9504
11000	-24	-0.4	1.59	-0.1	-23.9309
11001	-25	-0.4	1.41	-0.1	-24.9744
11010	-26	-0.4	1.26	-0.1	-25.9514
11011	-27	-0.4	1.12	-0.1	-26.9744
11100	-28	-0.2	2.00	-0.1	-27.9588
11101	-29	-0.2	1.78	-0.1	-28.971
11110	-30	-0.2	1.59	-0.1	-29.9515
11111	-31	-0.2	1.41	-0.1	-30.995

In order to select the appropriate gain for each gain stage, a resistor ladder was used in conjunction with a multiplexer. This way the multiplexers could select the correct resistance corresponding to the gain needed. This can be seen in Figure 2.10. The first gain stage is wired as an inverting op-amp with four possible gains. A total of ten resistors are needed for stage 1. The second gain stage is wired in a non-inverting configuration with eight possible gains. Eighteen resistors are needed for stage 2. The last gain stage is wired as an inverting op-amp with two possible gains. It requires six resistors. A differential-to-single ended op-amp is used at the output of the gain stages to convert the differential signal to a single ended output signal. This additional conversion requires four resistors. The use of differential signals throughout the preamp reduces harmonic distortion while increasing the dynamic range of the op-amp. This was a large improvement over Steven Turner and Wayne Slade's design.

2.5 Triangle Wave Generator

Two op-amps are used to generate a triangle wave as shown in Figure 2.11 below. Using positive feedback, one op-amp (I7) is designed to act as a Schmitt-Trigger, generating a square wave with a 50% duty-cycle. The other op-amp (I6) then integrates the square wave to produce a triangle wave. This triangle wave is designed to oscillate at 150kHz, well above the Nyquist rate for the highest frequency of interest in this project (20kHz). See Sedra & Smith [3] page 1005 for more information.

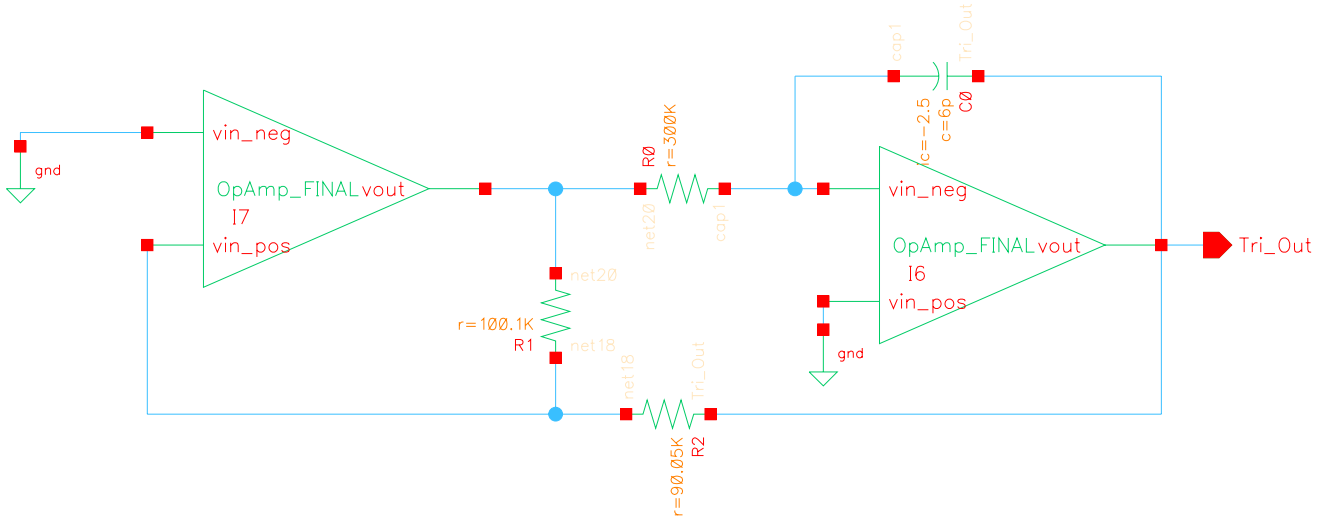

Figure 2.11 – Bi-Stable Oscillator Schematic

2.6 Comparator

The comparator generates a pulse-width modulated (PWM) signal by comparing the input signal to a triangle wave. The comparator design used in this project is found on page 693 of Baker [2]. It consists of three stages: the input pre-amplifier, the decision stage, and the output buffer. The input pre-amplifier improves the comparator's sensitivity so that a smaller difference in the input is needed to make a decision. The pre-amplifier also isolates the inputs from switching noise created by the decision stage. The decision stage determines which input signal is larger. Finally, the output buffer amplifies the information from the decision stage and outputs a logical signal. The comparator design is shown in Figure 2.12 below.

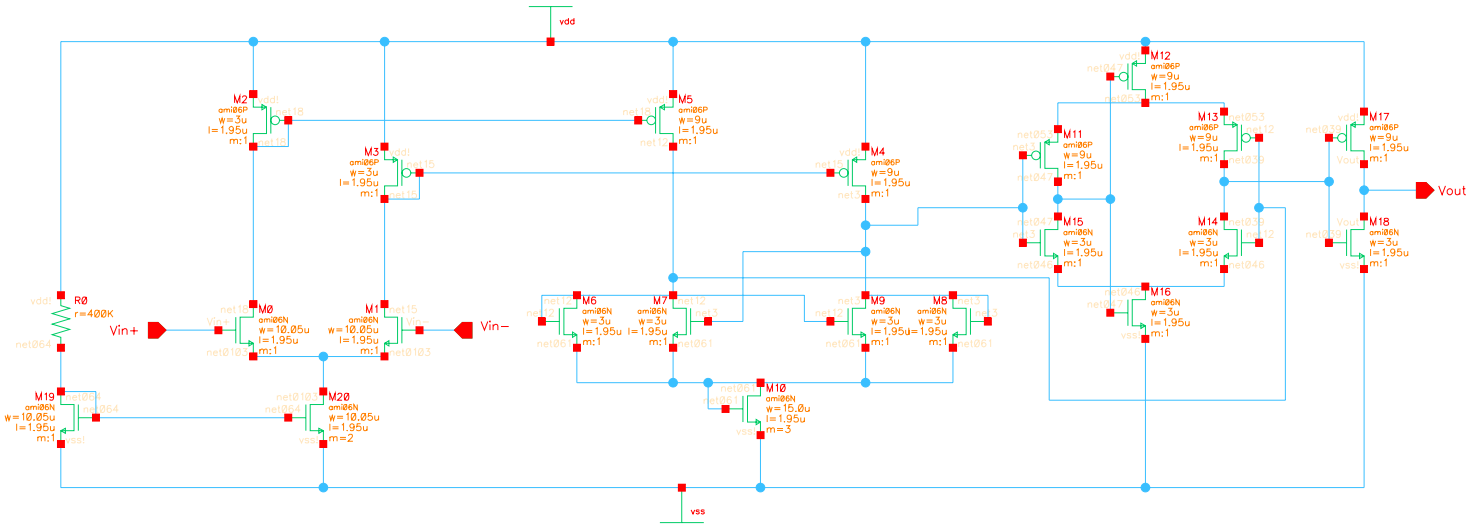

Figure 2.12 – Comparator Schematic

2.7 H-Bridge Driver

Since the transistors on the output stage of the comparator are much smaller than the transistors on the H-Bridge, a driver is needed so that the transistors on the H-Bridge can be turned on and off. As shown in Figure 2.13, the transistors in the driver are sized progressively larger until inverters large enough to drive the H-Bridge are reached.

Also, if both the PMOS and the NMOS transistors on the same leg of the H-Bridge (M0 and M1 or M2 and M3 in Figure 2.14) are on, current flows between the supply rails without flowing through the load. This "shoot-through" reduces efficiency of the Class-D amplifier because power is wasted. To ensure that shoot-through does not occur, a cross-coupled NAND gate (M0, M1, M4, and M5), as shown in Figure 2.13, is added so that one transistor turns off before the other one turns on.

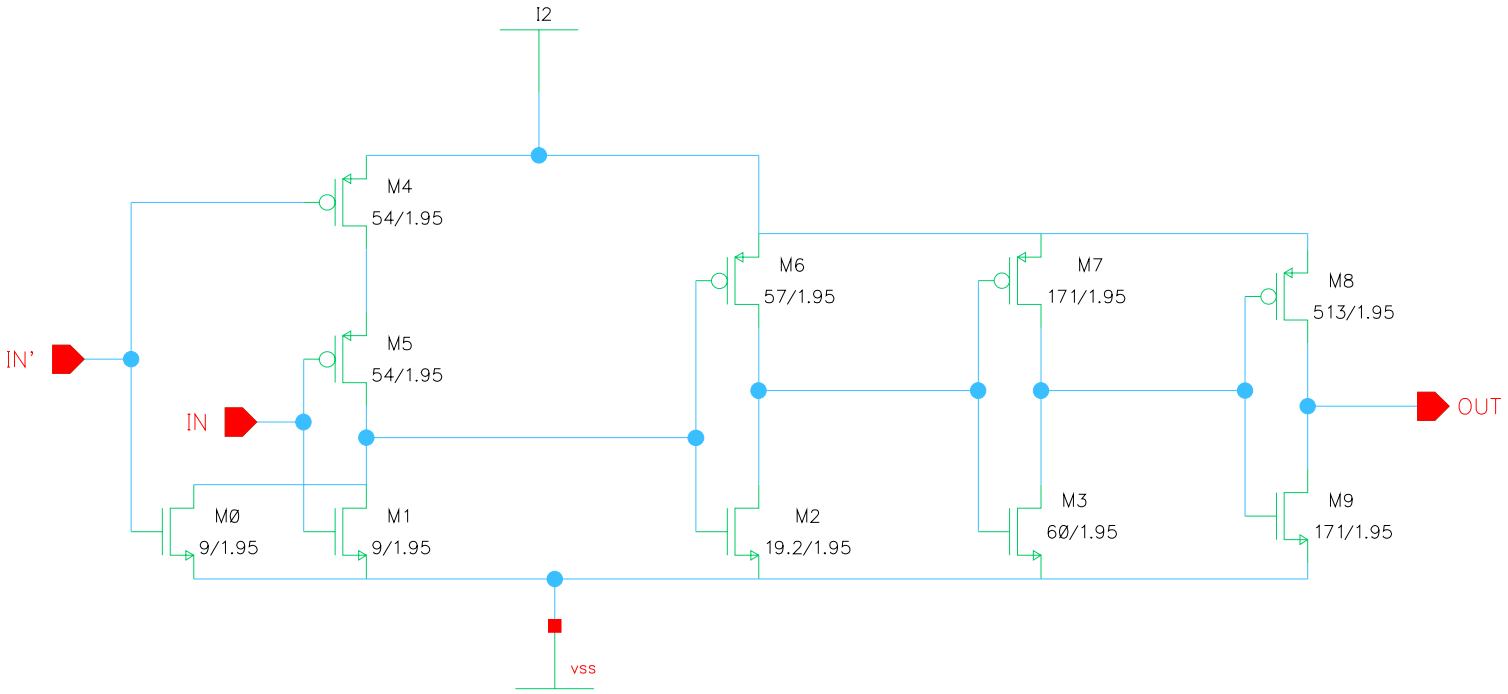

Figure 2.13 – H-Bridge Driver Schematic

2.8 H-Bridge

The digital voltage levels of the PWM signal control the transistors on the H-Bridge, shown in Figure 2.14 below, which in turn drives the audio speaker. When the PWM is high, current flows through the speaker in one direction by turning on transistors M0 and M3. Current flows through the speaker in the opposite direction when the PWM is low by turning transistors M1 and M2 on. The transistor sizes have been chosen to drive an 8 ohm load (speaker) with 400mA of current.

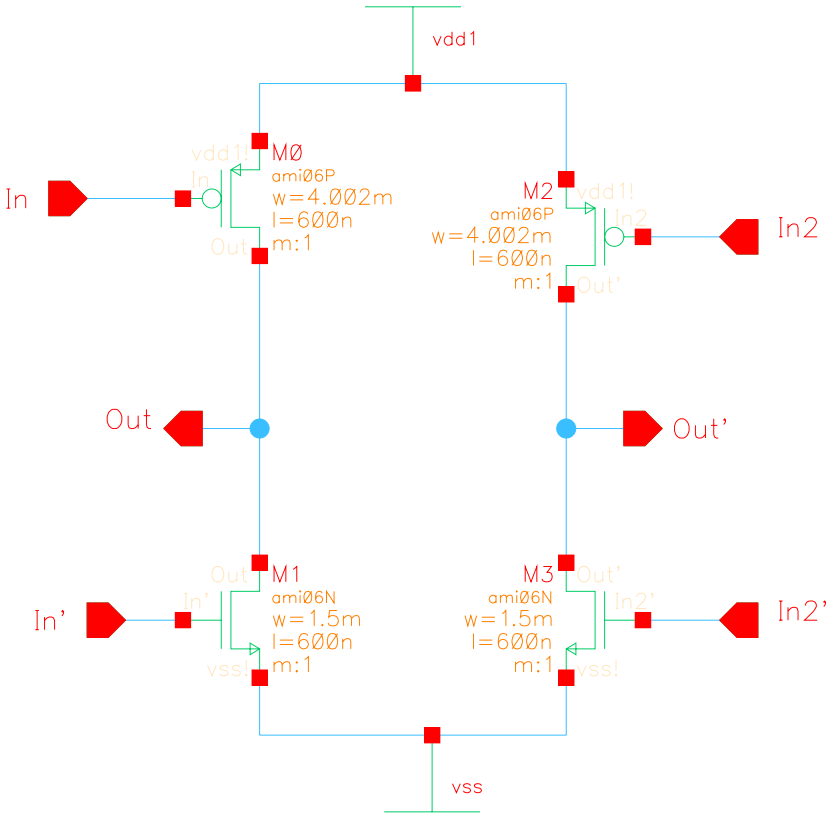

Figure 2.14 – H-Bridge Schematic

Chapter 3
Simulated Results

3.1 Fully Differential Operational Amplifier

Three tests were done to test the fully differential operational amplifier. These tests characterized the AC, DC, and transients responses. In order to test the AC response of our circuit, we used the configuration shown below.

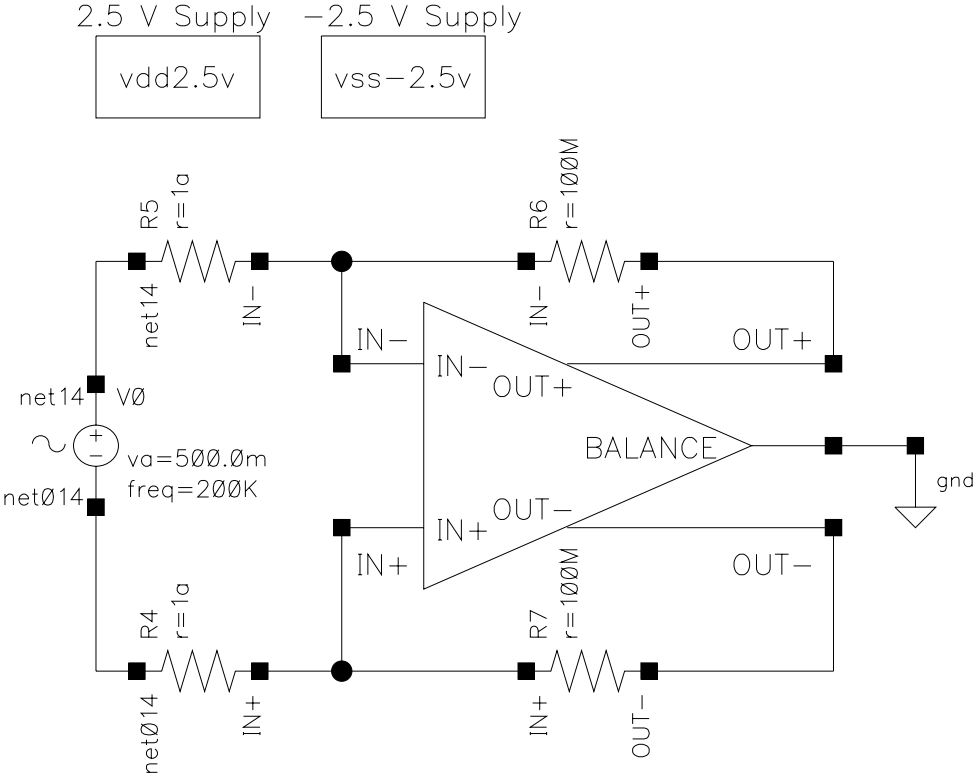

Figure 3.1 – Fully Differential Operational Amplifier AC Test Circuit

This is comparable to feeding a differential signal right between IN+ and IN- (note that R4 and R5 are 1 aΩ). Also note that R6 and R7 are 100 MΩ, so the feedback path is almost infinite resistance. This should provide us with an AC response of the designed fully differential op-amp without parasitics (for a discussion of parasitics see Section 5.2). The magnitude and phase response for this circuit can be seen on the next page in Figure 3.2.

These plots show that we have about 14.4 MHz of bandwidth and about 80° of phase margin. This is more than adequate for our purpose.

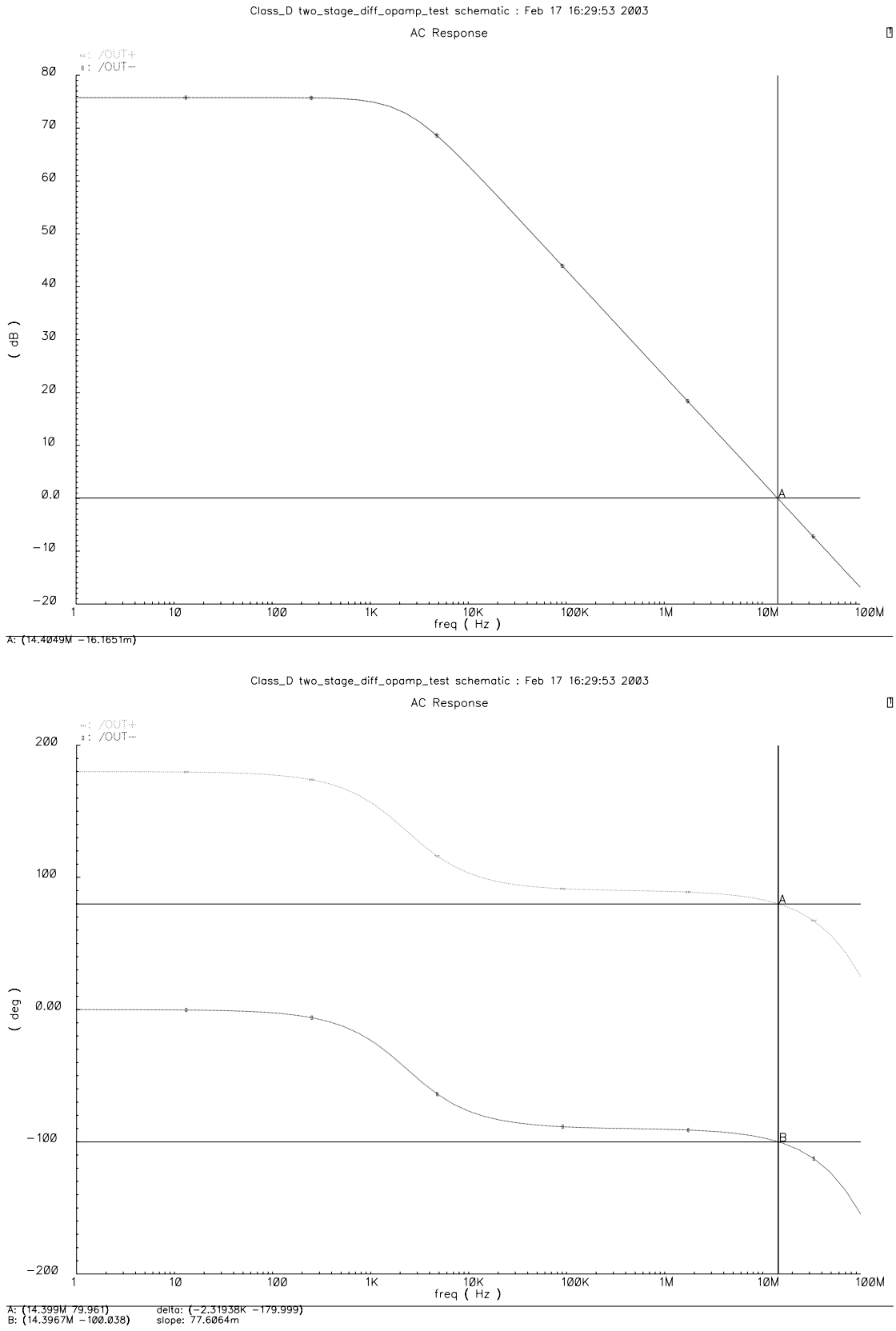

Figure 3.2 – Fully Differential Operational Amplifier AC Response

To test the DC response, we swept the input voltage from -6 V to 6 V for an amplifier in the unity gain configuration. The schematic for this test is shown below.

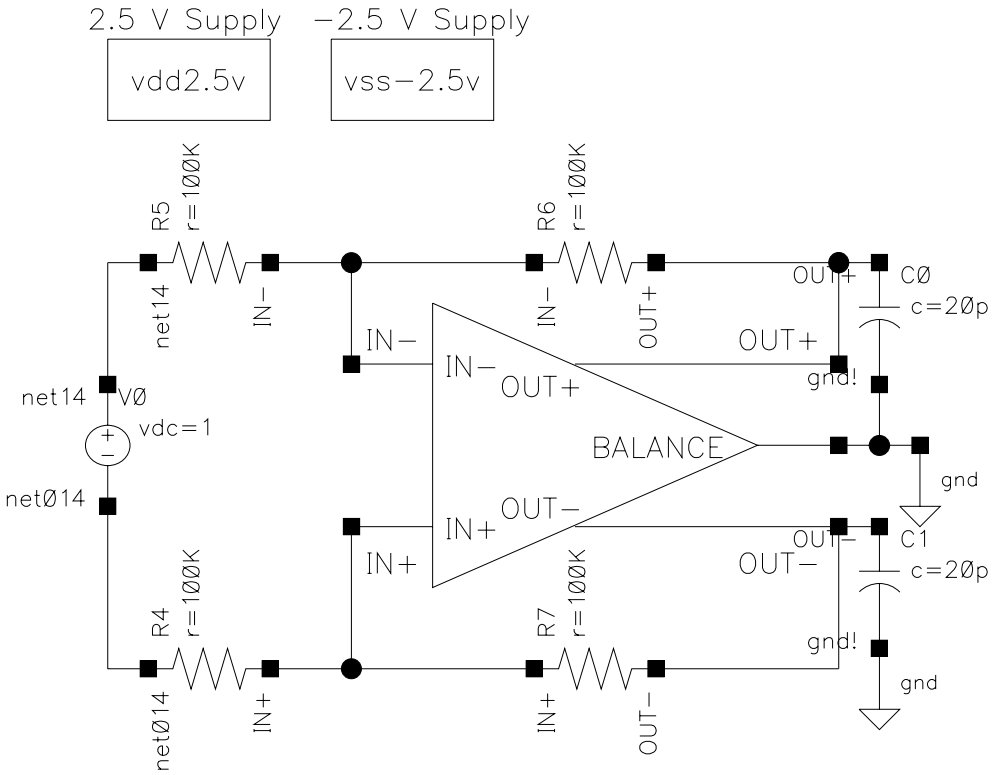

Figure 3.3 – Fully Differential Operational Amplifier DC Test Circuit

The differential input and differential output was taken from this and can be seen in Figure 3.4. As we would expect, the output exhibits good linearity between the voltage rails, +/-2.5 V. Since the voltage source is differential, however, the response exhibits good linearity between +/-5 V (differential).

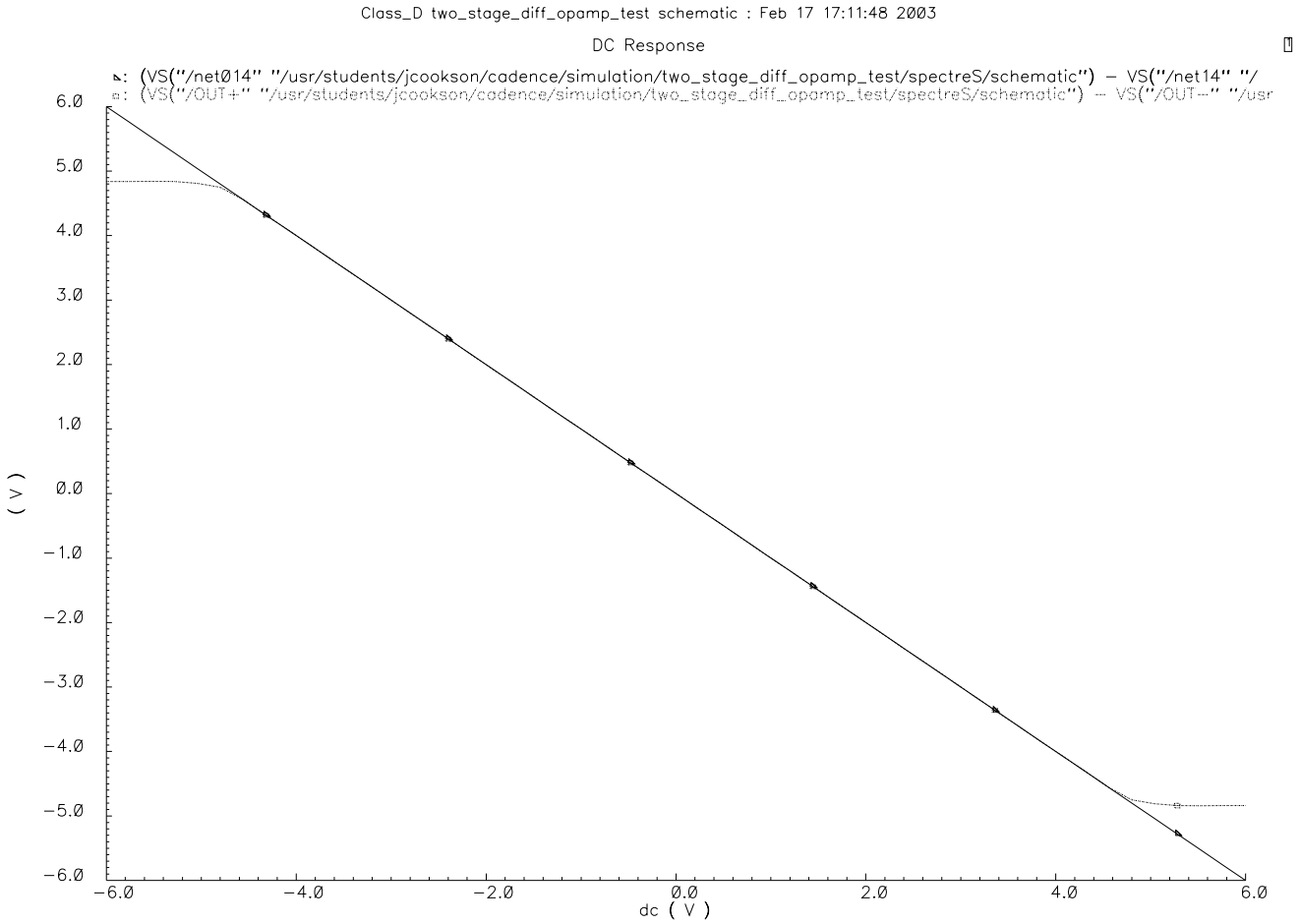

Figure 3.4 – Fully Differential Operational Amplifier DC Response

The last test for the fully differential op-amp was to characterize the transient behavior. To do this, the op-amp was operated in an inverting unity gain configuration with capacitive loads (20 pF) and a step function was applied to the input. This configuration, as well as the response, is shown in Figure 3.5 and Figure 3.6, respectively.

The transient response shown in Figure 3.6 is what we expect. As you can see, a non-ideal unit step function was applied at the input at 500ns with a 1ns rise time. The output, which is inverted, exhibits good linearity while transitioning and begins and ends at the appropriate voltage levels (2.5V and -2.5V).

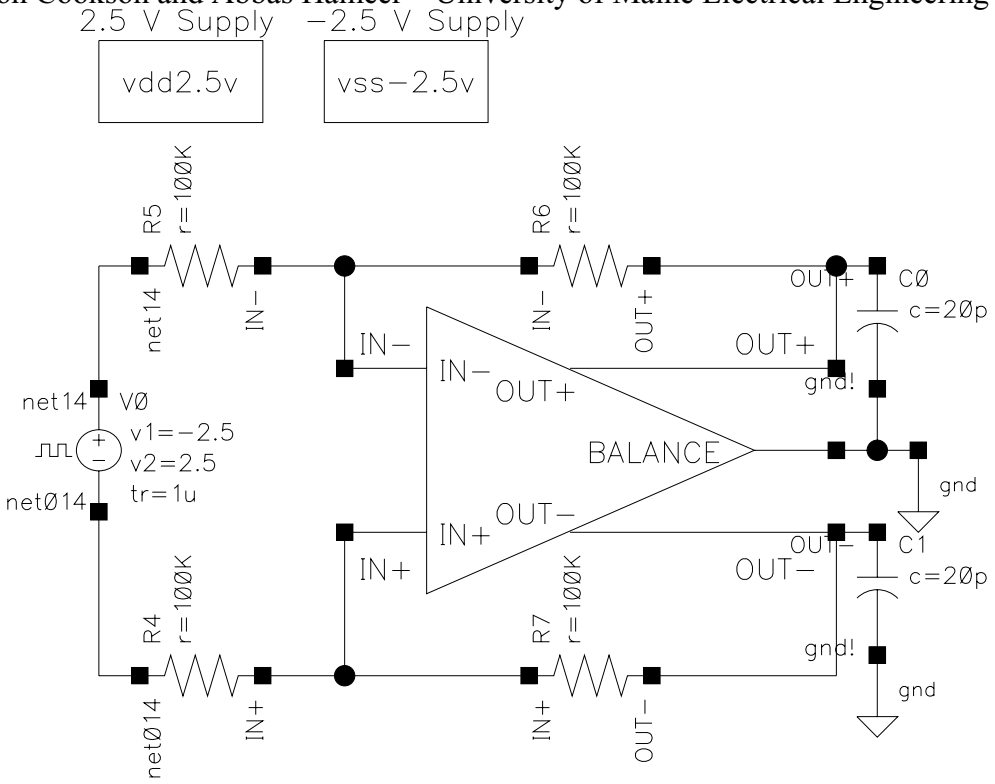

Figure 3.5 – Fully Differential Operational Amplifier Transient Test Circuit

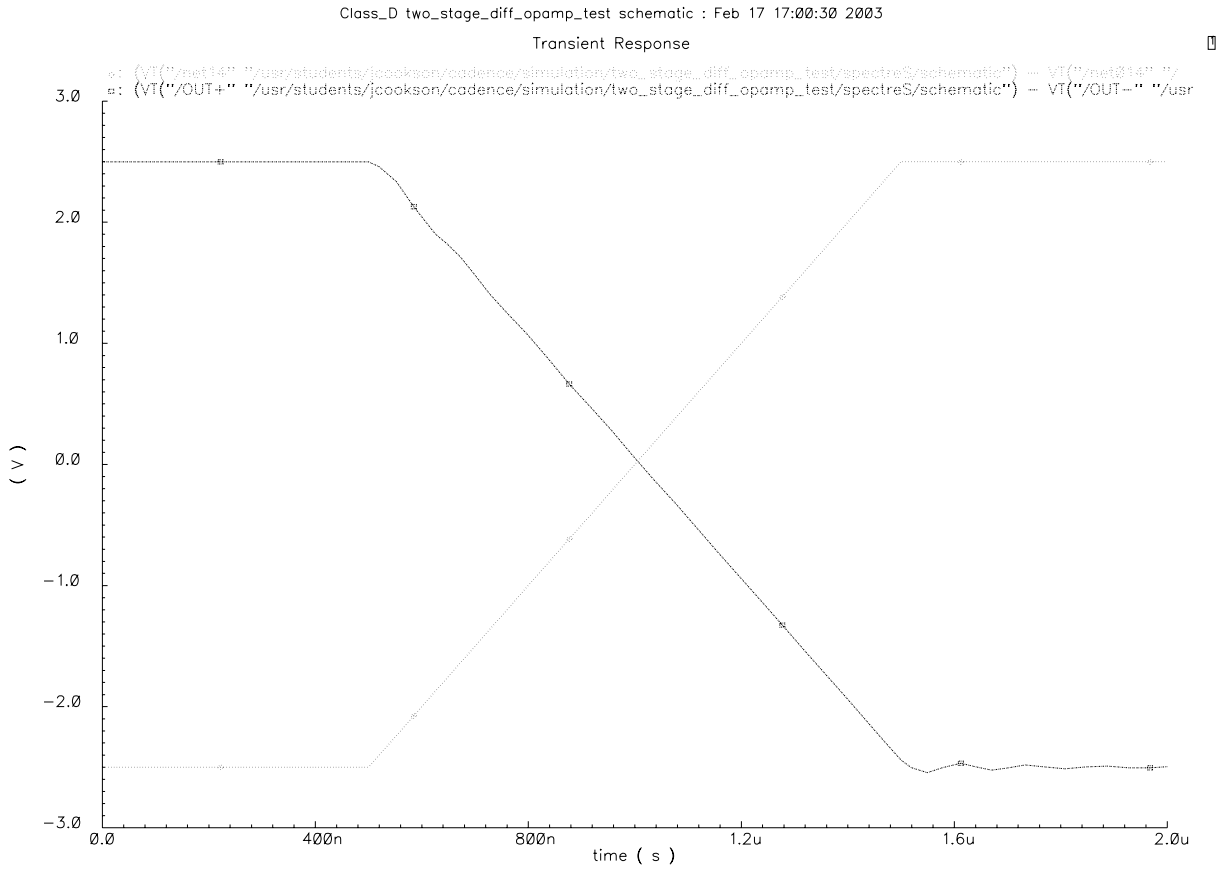

Figure 3.6 – Fully Differential Operational Amplifier Transient Response

3.2 Volume Control Preamplifier

Instead of showing the tests for each component in the volume control preamplifier, I will simply show two tests. The first will be our design of an 8 to 1 multiplexer that is used throughout our preamplifier. The other test will be of the complete preamplifier.

Multiplexers (Mux_8to1)

Since the 8 to 1 mux contains 4 to 1 and 2 to 1 muxes, we will only show that the larger one works. To test the multiplexer, input signals of 10kHz and 20kHz were applied to inputs IN[0] and IN[1] respectively. The input signal amplitudes were chosen to be different so the reader can more easily see the transition between states. Initially, the 10kHz signal is selected and output. After 1 ns, however, the select logic is changed to output the 20kHz signal. This schematic is shown below.

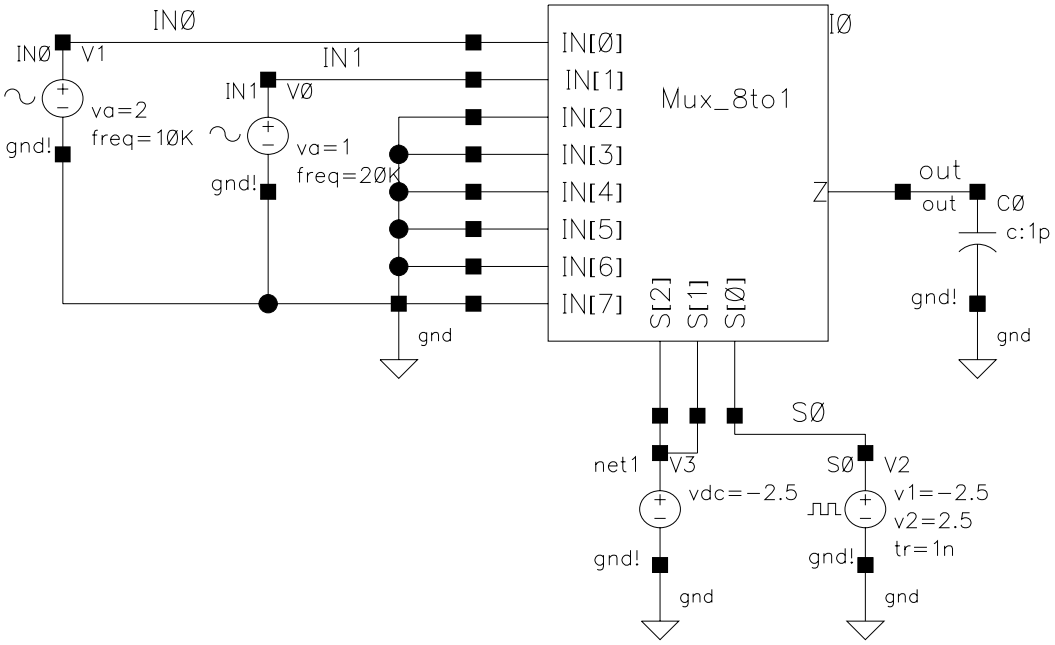

Figure 3.7 – 8 to 1 Multiplexer Test Circuit

The waveforms for this test are shown in Figure 3.8. The top plot shows the two input signals, the 10kHz signal and the 20kHz signal. The bottom plot shows the select signal changing, and the corresponding multiplexer output.

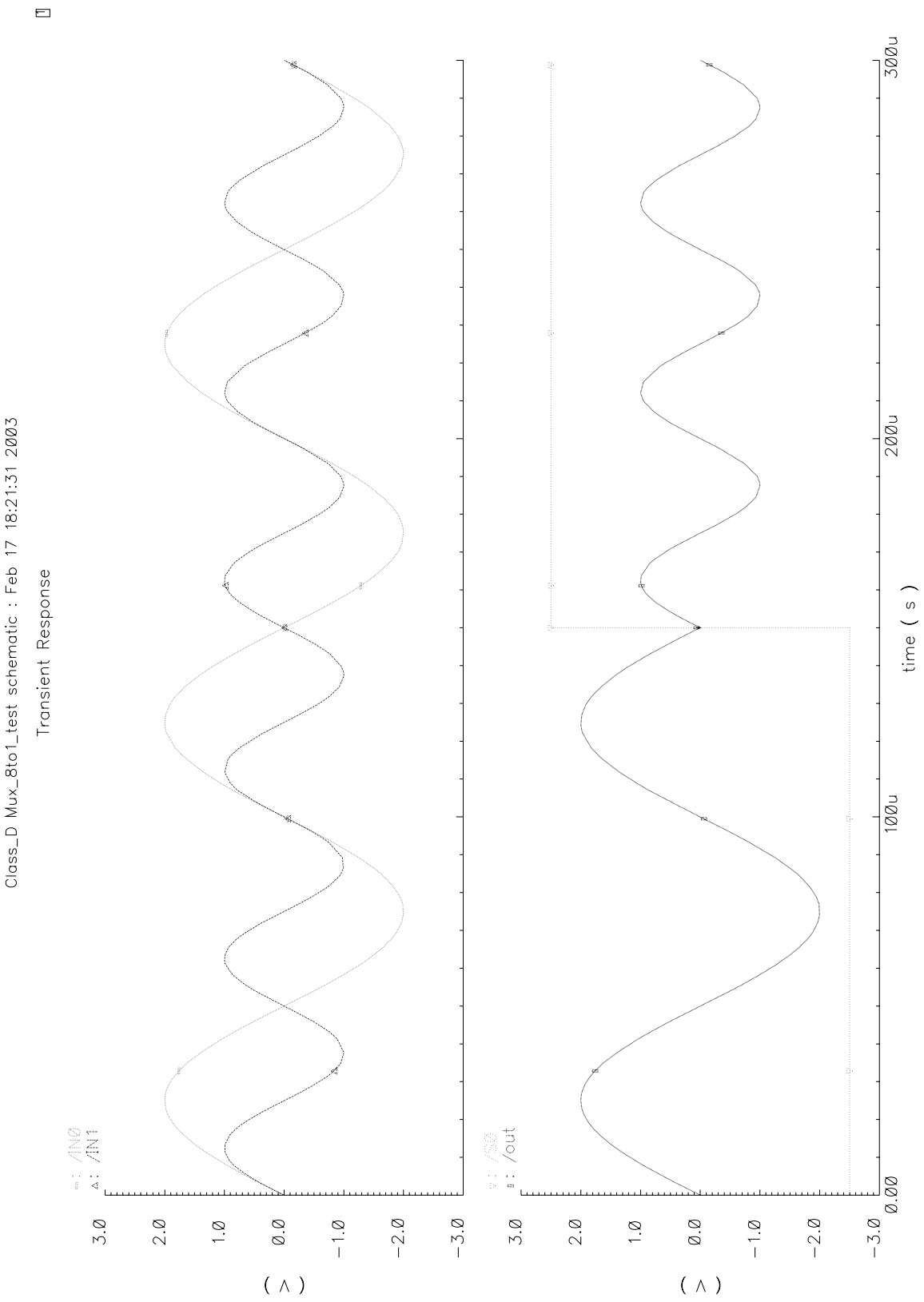

Figure 3.8 – 8 to 1 Multiplexer Test Waveform

Volume Control Preamplifier

In order to test all the possible inputs to the preamplifier a parametric simulation of all the possible inputs was performed. This should be sufficient to show that all cells in the preamplifier circuit perform correctly. The schematic for this test is shown below.

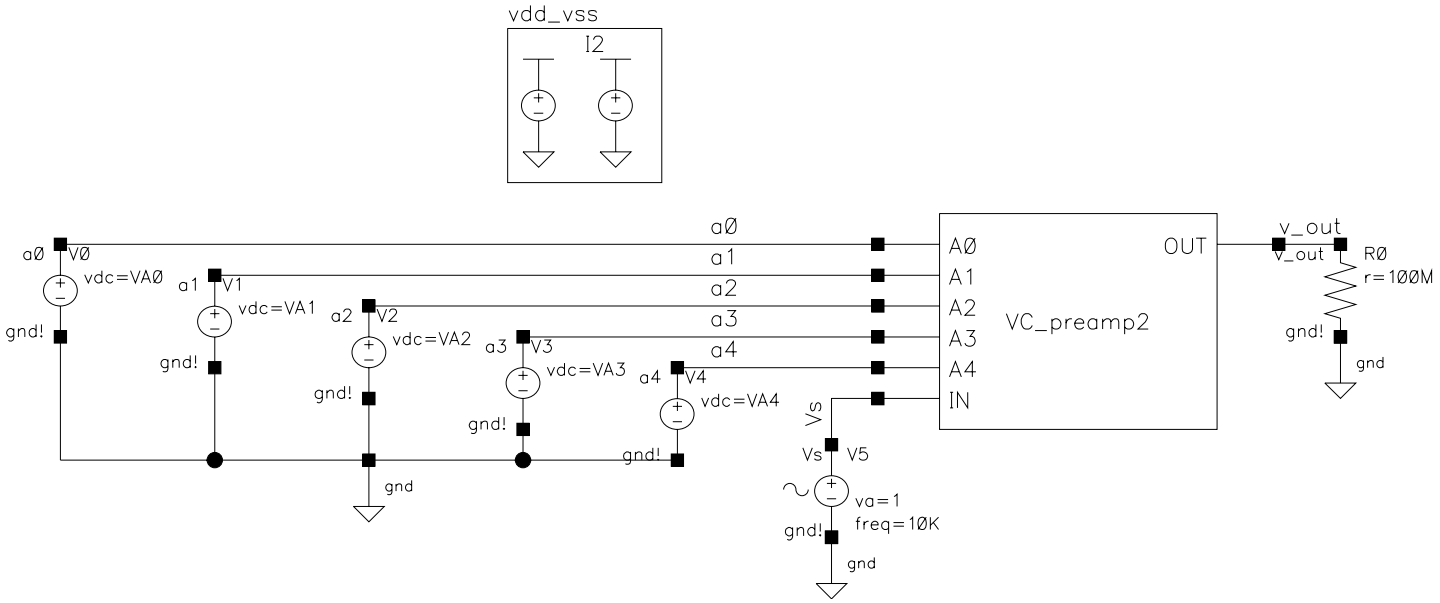

Figure 3.9 – Volume Control Preamplifier Test Circuit

In this circuit the digital volume control inputs VA0, VA1, VA2, VA3, and VA4 are changed between +/-2.5 V to generate all possible logic combinations. The waveform in Figure 3.10 shows the output of the volume control preamplifier. All attenuation levels between the range of 0 dB and -31 dB are achieved.

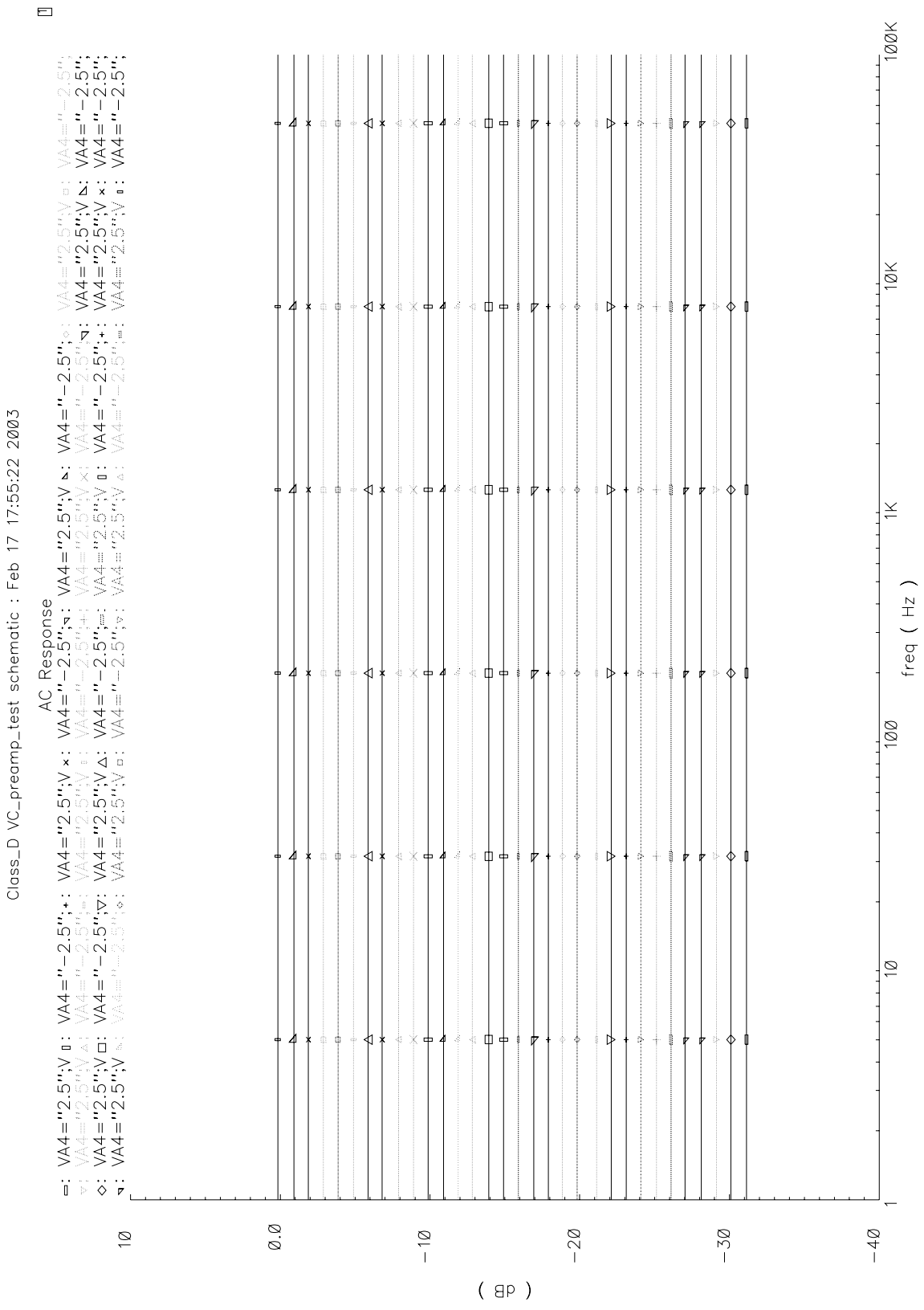

Figure 3.10 – Volume Control Preamplifier Test Waveform

3.3 Triangle Wave Generator

The simulation waveform shown in Figure 3.11 below is the triangle wave generated by the bistable oscillator. The frequency of the triangle wave is found to be 130.7kHz, which meets Nyquist's sampling criteria for our highest frequency (20kHz).

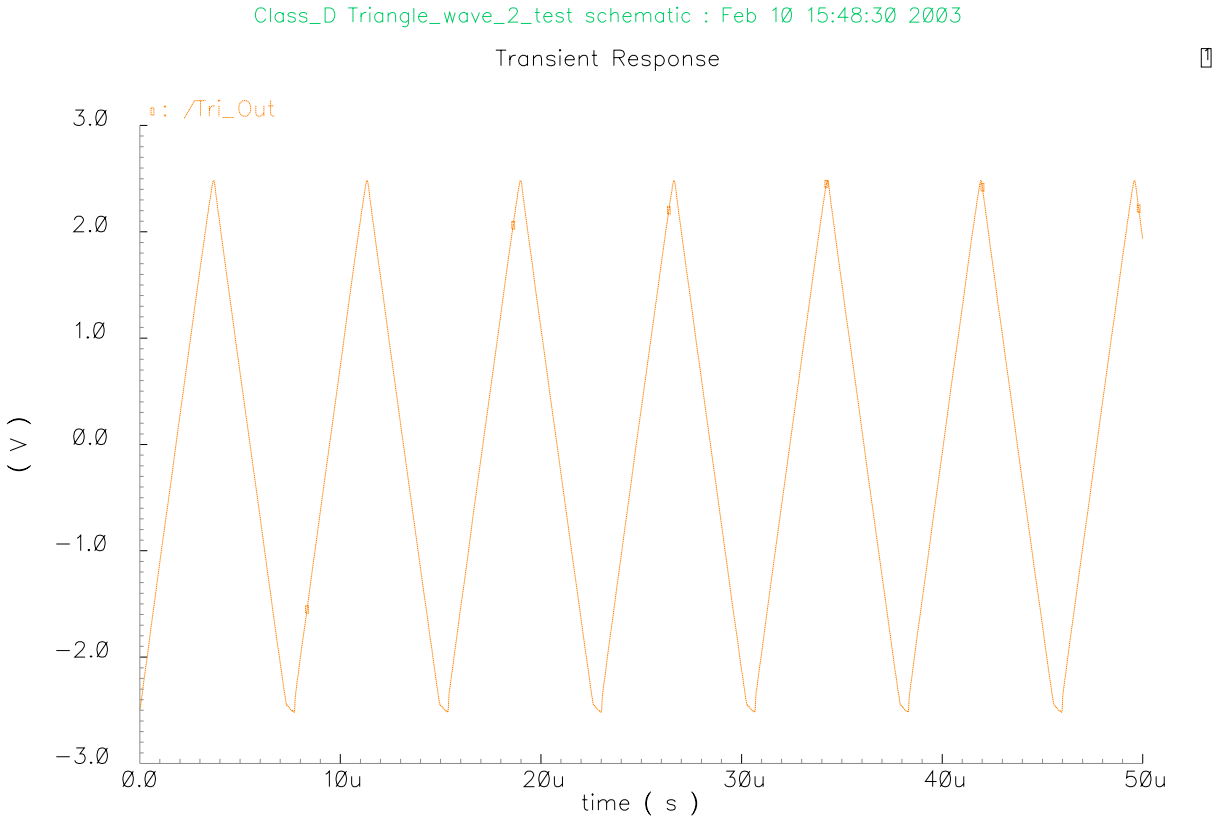

Figure 3.11 – Triangle Wave Generator Test Waveform

Although the bottom peak is slightly distorted, it will not affect the quality of the Class-D amplifier because we will never let our audio signal reach the distortion. By limiting our audio signal to between +/-1.5 V we ensure that the corresponding triangle wave has linear rising and falling edges.

3.4 Comparator

The comparator is simulated using a 20kHz sine wave and a 180kHz triangle wave as inputs. The triangle wave is connected to the Vin+ input terminal and the sine wave (representing an audio signal) is connected to the Vin- input terminal. The resulting output is a pulse width modulated (PWM) signal as shown in Figure 3.12 below.

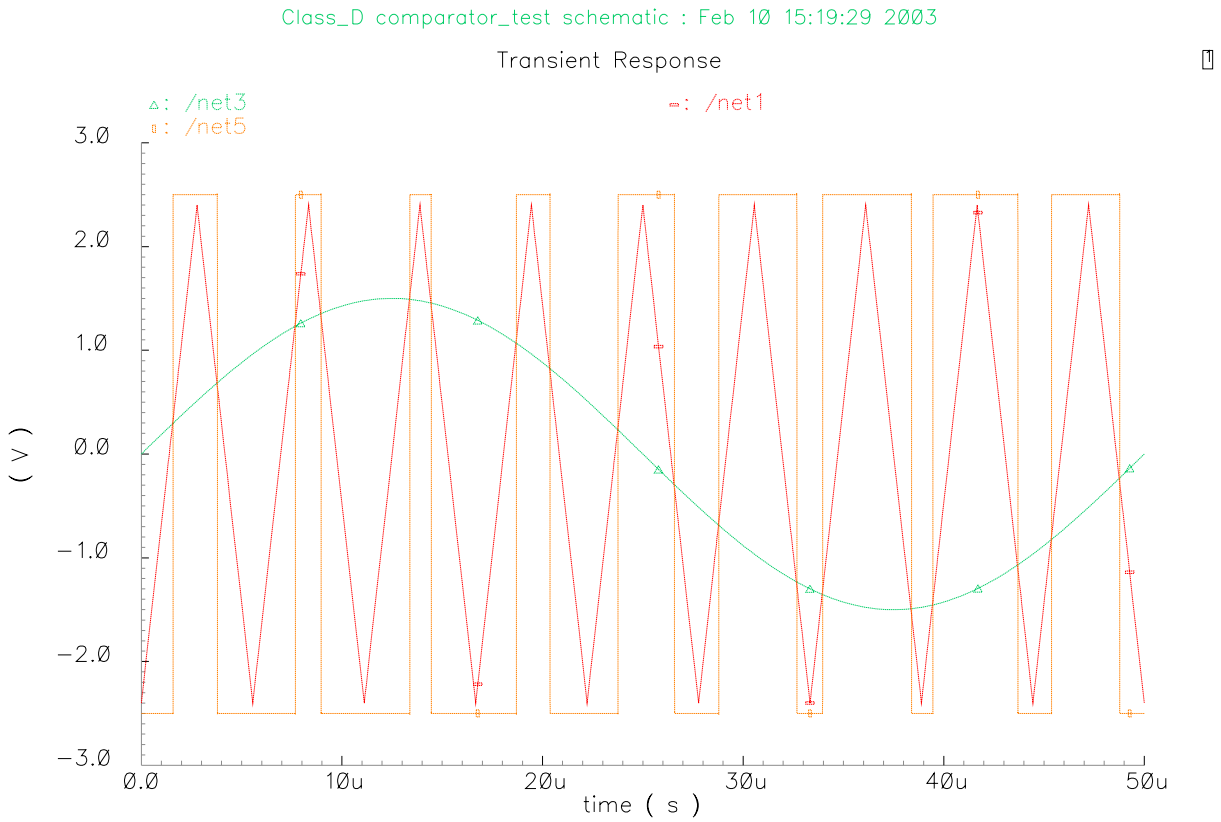

Figure 3.12 – Comparator (PWM) Test Waveform

3.5 H-Bridge Driver

The simulations shown in Figure 3.13 and Figure 3.14 show the delay caused by the driver to the PWM. The falling edge is delayed by 2ns where as the rising edge is delayed by 4ns. The rising edge has a greater delay due to the NAND gate in the driver. To obtain symmetry in the delays, a NOR gate can be added to the driver. This was not done, however, due to the space constraints of the chip.

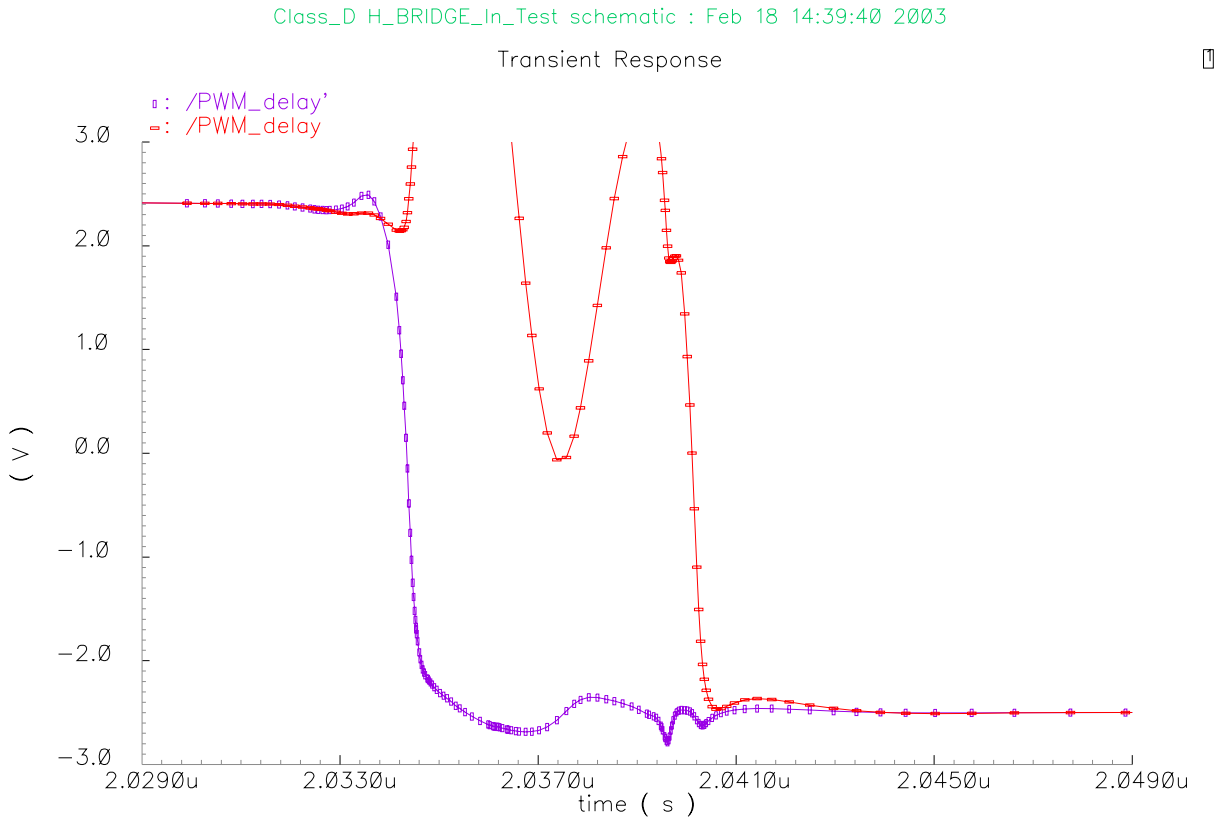

Figure 3.13 – H-Bridge Driver Falling Edge Delay Waveform

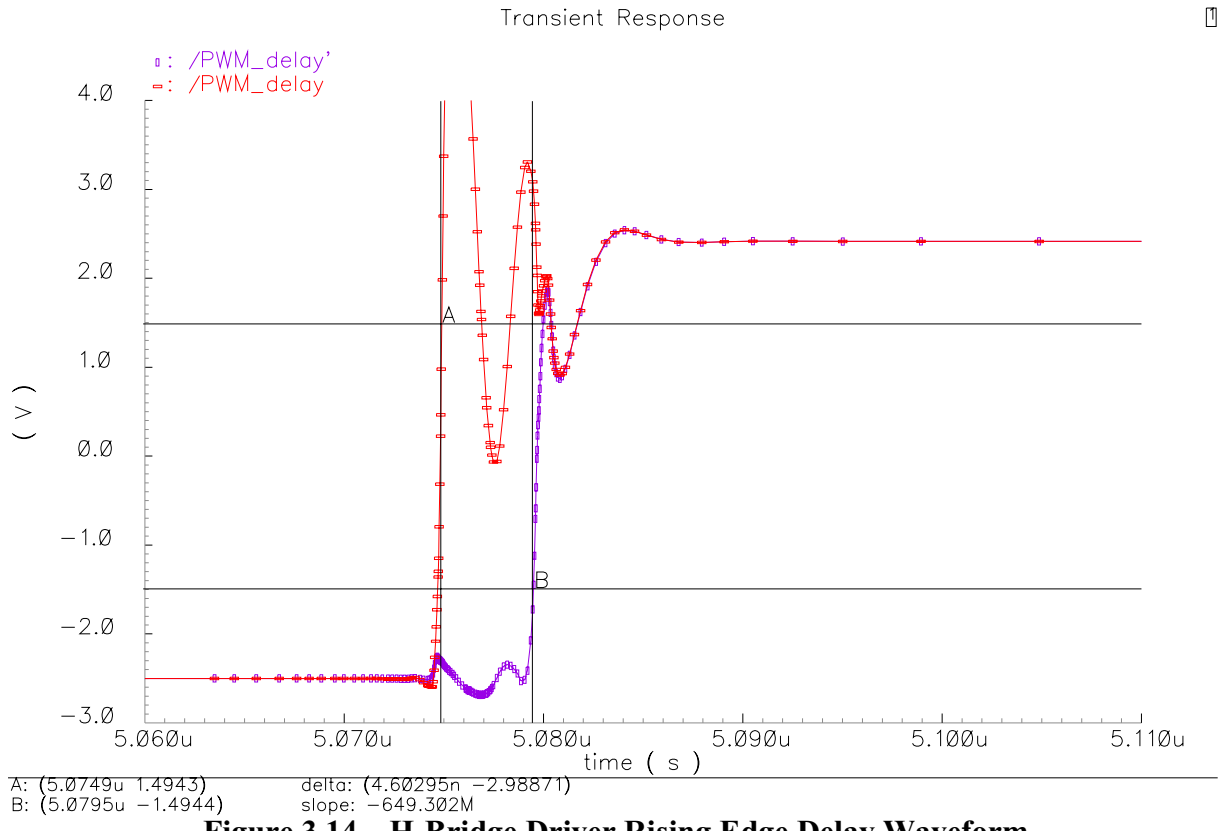

Figure 3.14 – H-Bridge Driver Rising Edge Delay Waveform

3.6 H-Bridge

The simulation shown in Figure 3.15 below shows the current (400mA) provided by the H-Bridge to a resistive 8 load. The transistors of the H-Bridge are driven by the PWM signal from the H-Bridge driver.

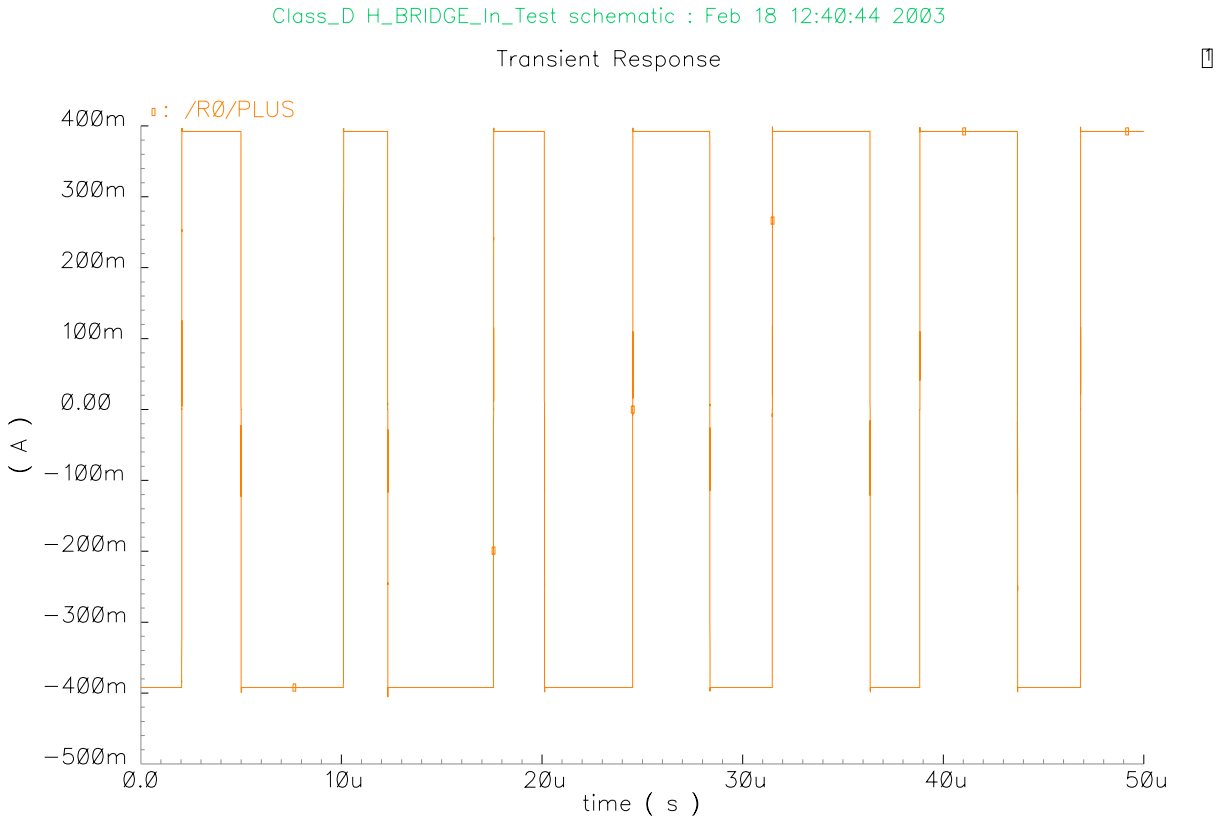

Figure 3.15 – H-Bridge Waveform

3.7 Entire Chip

The last part to simulate is the entire chip with no parasitic capacitances. This test was performed using a 20kHz sinusoidal input, the maximum frequency the chip will operate at. It will drive an 8 ohm purely resistive load, since again this is the largest load it will drive. The schematic for this test is shown below in Figure 3.16.

The results of this test are quite promising. You can see from the waveform in Figure 3.17 that the triangle wave is linear when transitioning between the voltage rails. The bottom of the triangle waveform is slightly non-linear, but this doesn't affect our project; notice that the sinusoidal signal is not allowed to reach this non-linearity. Also notice how fast the PWM signals rise and fall times are. Their almost instantaneous change (5ns) is ideal. Lastly, from the H-Bridge current plot (bottom pane) you can see that there is 400mA flowing through the H-Bridge in one direction or the other. This again is an ideal waveform.

Top-level performance has also been simulated using extracted parasitics. For details of this, see Chapter 5.

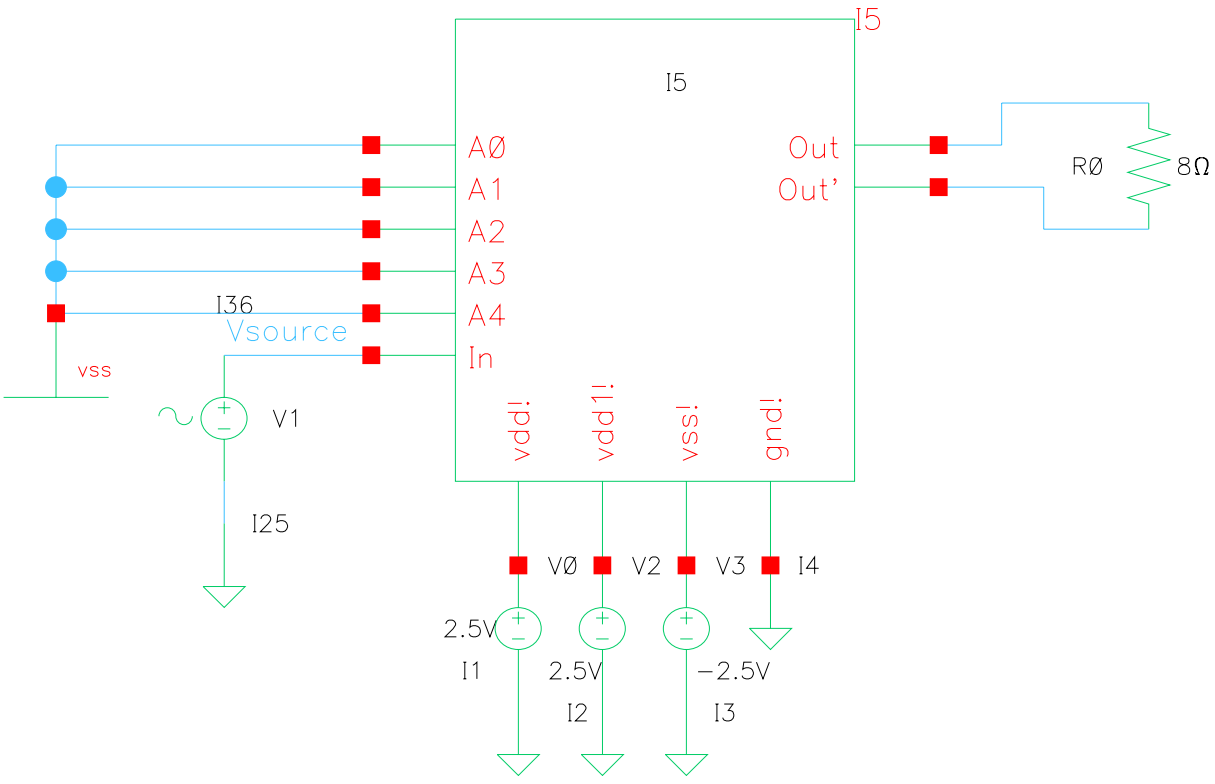

Figure 3.16 – Top Level Schematic

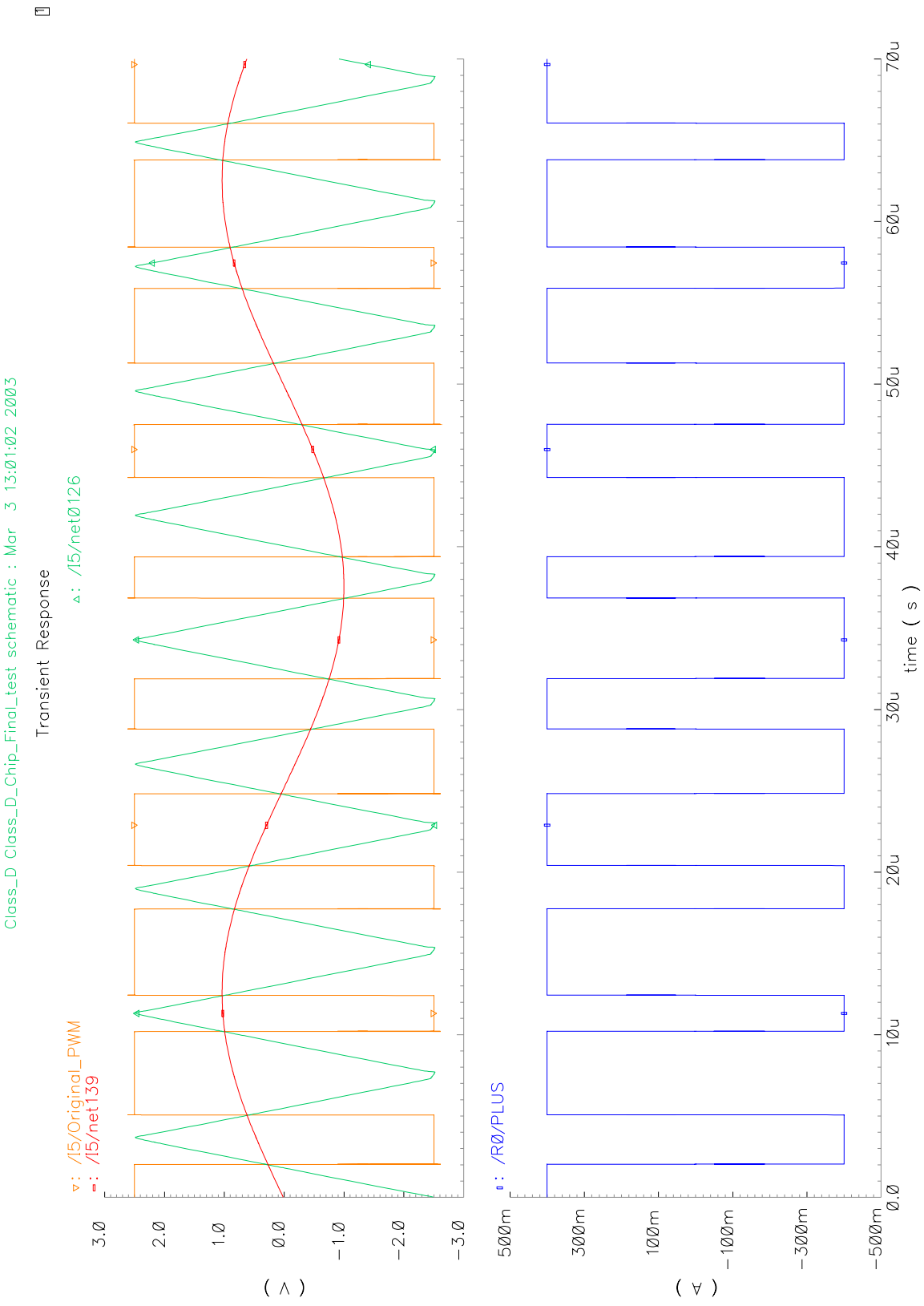

Figure 3.17 – Top Level Simulation Waveforms

Chapter 4
Layout Design

4.1 Components

The layout for all the components share the same general characteristics. Therefore, to ease redundancy a layout description for all components follows. First, Vss and Vdd guard rings are present wherever appropriate. This will hopefully reduce noise coupling between neighboring components. Drains are also shared wherever possible. This not only reduces parasitics by shortening the distance between transistors, but it also reduces the size of the particular cell. Vss and Vdd taps are also present in any empty spaces. By doing this, a "good" contact with both Vss and Vdd will be achieved. Lastly, routing with metal 3 was avoided when laying out each component. This way, it became very easy to wire all the components together on our final chip.

4.2 Outer Guard Ring

In order to use separate Vdd supplies for the front and back end of our project and to reduce substrate noise, we chose to break the outer guard ring and form two separate rings. This reduced the available on-chip area, but will hopefully greatly benefit the integrity of our signals.

Multiple pins were also used for critical signals. Three pins were used for our ground signal in order to reduce the parasitic resistance due to the pins. Also, four pins were used for both the Vdd and Vss supplies in the back end of our project. There will be a large amount of current flowing through our H-Bridge (400mA), so we have to make sure the limitations of our pins are not exceeded. This was accomplished by simply limiting the current through each pin. The same solution follows for our H-Bridge output pins. Since the 400mA flowing through our H-Bridge is output to a speaker we have to

ensure that the current can safely exit our chip. Therefore, four pins were used for both the positive and negative output terminals of our H-Bridge. This met the electromigration limits for our process. For our Class-D Amplifier chip pin out see Table 1.2 on page 5. For layout diagrams see Figure C.1 and Figure C.2 in Appendix C.

4.3 Physical Layout

Like the functionality of the Class-D Audio Amplifier, the layout of our chip is split into two areas, the front end and the back end. The front end, where the pulse width modulated signal is created, appears on the top half of our chip. This contains the preamp circuitry, the triangle wave generator, and the comparator. The back end of our chip, where the PWM signal is amplified to be delivered to a speaker, appears on the lower half of our chip. The back end consists of the H-Bridge delay buffers and the H-Bridge itself.

Our design was somewhat tightly packed. Although there were spare pins, there simply wasn't enough space on the chip to include test circuitry. The concern that some test circuitry such as a ring oscillator would degrade the integrity of our critical signals (such as the triangle wave oscillator) also led to our decision not to include any test circuits.

Chapter 5
Verification

5.1 Verification of Design

Before verifying the top-level functionality of the Class-D amplifier each component was first simulated and verified. Once all the cells were determined to be functionally correct the cells were tied together to form the top-level of the Class-D amplifier. This top-level cell was then simulated and verified. Similarly, during layout, *Design Rule Checks (DRC)* and *Layout versus Schematic (LVS)* checks were first performed on the individual cells and then on the complete circuit. The top-level layout passed DRC without any errors and LVS showed the layout to logically match the components in the original schematic.

5.2 Simulations with Parasitic Extractions

Once layout was complete and verified, the analog extracted schematic was simulated. The analog extracted schematic is obtained from the physical layout and contains certain parasitics that are not present in the original schematic. Therefore, the simulation of the extracted view will better depict how the fabricated chip will actually work.

Initial attempts to simulate the top-level extracted schematic failed because Cadence was unable to converge on a DC solution. This problem occurred because no initial condition could be specified for the bistable oscillator to start the oscillations. Therefore, for test reasons, a relatively small capacitor (1aF) was added in parallel with the 6pF capacitor and given an initial condition.

The circuit shown in Figure 5.1 was used to simulate the top-level functionality of the parasitic Class-D amplifier. The circuit is similar to the one used to simulate the non-parasitic top-level schematic, the only difference being the 1aF capacitor. The circuit was tested using a 20kHz sinusoidal input. The output had to drive an 8 ohm resistive load. The plot of the output is shown in Figure 5.2 below. Only a slight difference can be seen between the analog extracted output and the 'ideal' output, shown previously in Figure 3.12 on page 7.

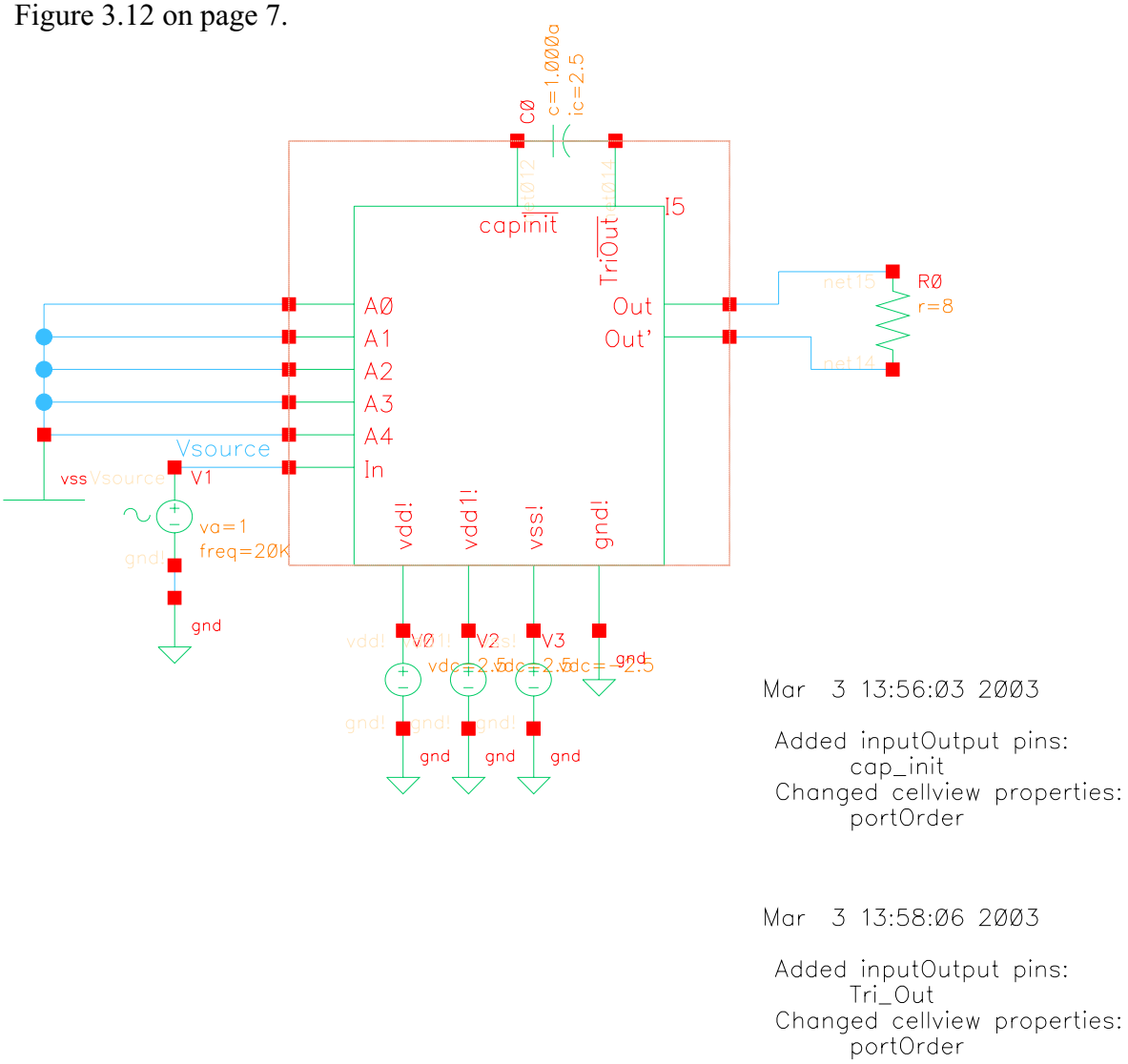

Figure 5.1 – Top-Level Simulation Circuit with Parasitics

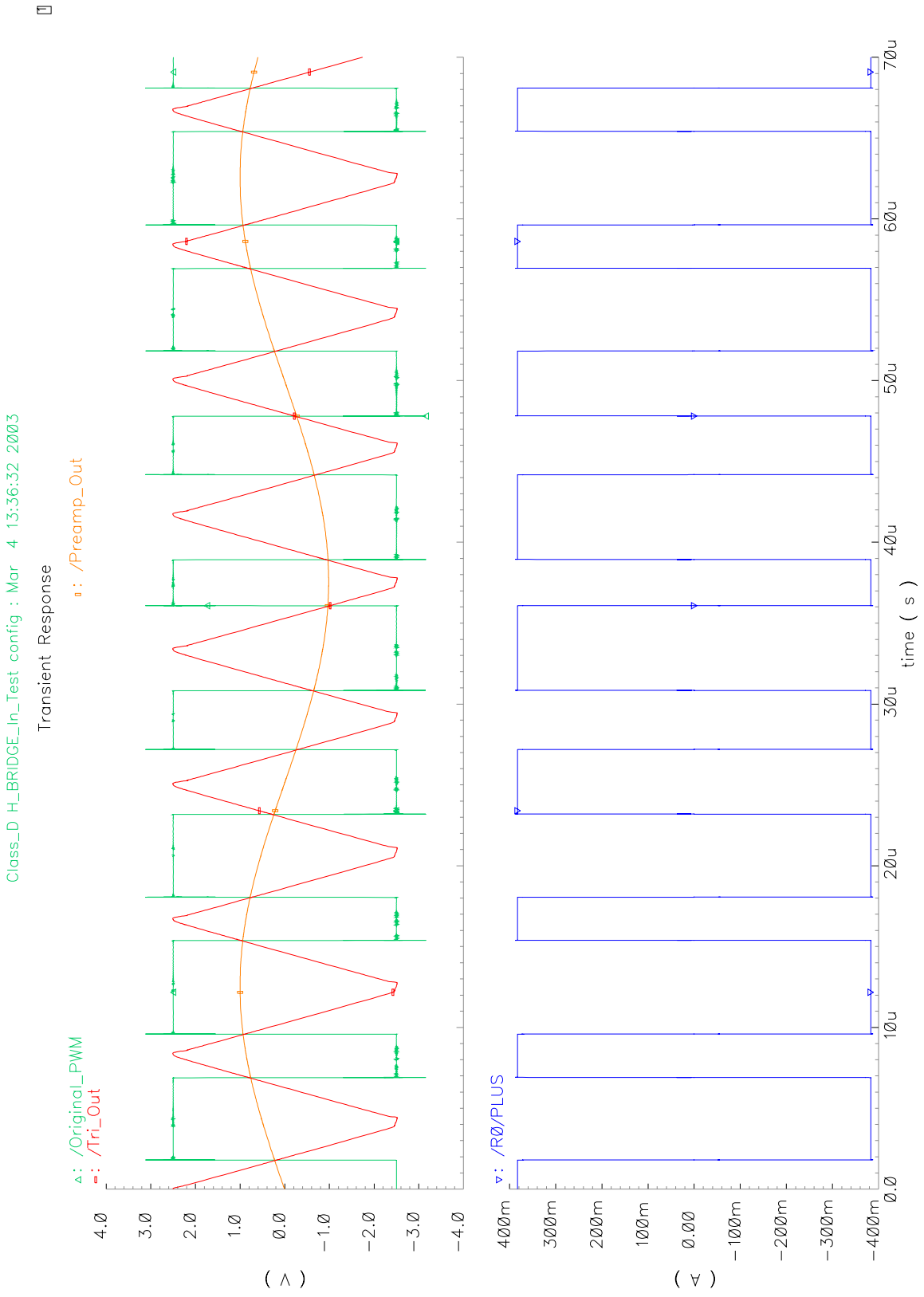

Figure 5.2 – Top-Level Simulation Waveform with Parasitics

Chapter 6
Experimental Tests

Five tests are described in the following chapter that outline how we characterized our Class-D Audio Amplifier. These tests were conducted in April 2003.

6.1 Test 1 – Static Power Dissipation

This is the simplest characterization test, which determines if there are any Vdd or Vss shorts to ground. It will also give us a rough idea if the fabricated chip will match our simulated results.

Equipment:

- (2) Agilent E3642A DC Power Supplies

Procedure:

- Ground all inputs.
- Ramp power supplies to Vdd=2.5V and Vss=-2.5V slowly, observing how much current is drawn from the power supplies.
- If the current drawn is not excessive, compare to simulated values.
- If the current drawn is excessive, suspect shorts in the fabricated chip.

Results:

- This test passed. When I ramped Vdd and Vss towards +/-2.5V there was not an excessive amount of current drawn from the power supplies. In fact, when the voltage supplies were at +/-2.5V there was only 3 – 4 mA drawn from each power supply which agrees with our simulated results.

6.2 Test 2 – Dynamic Power Dissipation

This is fairly simple characterization test, which determines if there is excessive power dissipation with an audio input. It will also give us a better idea if the fabricated chip will match our simulated results, because it will generate a pulse width modulated signal that we can compare with our simulations.

Equipment:

- (2) Agilent E3642A DC Power Supplies
- (1) Agilent 33250A 80MHz Function Generator
- (1) Yokogawa Dl7100 Digital Oscilloscope

Procedure:

- Wire all five digital volume control inputs to Vss to achieve a gain of 0 dB. Attach a 5kHz sinusoidal input to the audio input pin. Leave the output with no load attached.
- Ramp power supplies to Vdd=2.5V and Vss=-2.5V slowly, observing how much current is drawn from the power supplies.
- If the current drawn is not excessive, compare to simulated values.
- If the current drawn is excessive, suspect problems in the fabricated chip.

Results:

- This test passed. When I ramped Vdd and Vss towards +/-2.5V there was not an excessive amount of current drawn from the power supplies. For a 5kHz, 2Vpp sinusoidal input, and with the power supplies at +/-2.5V there was only 3 – 4 mA drawn from each supply which agrees with our simulated results. The simulation of the sinusoidal input and resulting PWM output is shown below in Figure 6.1. It appears that the PWM signal is correct, since it has a longer high time when the sinusoidal input is high, and a shorter high time when the sinusoidal input is low.

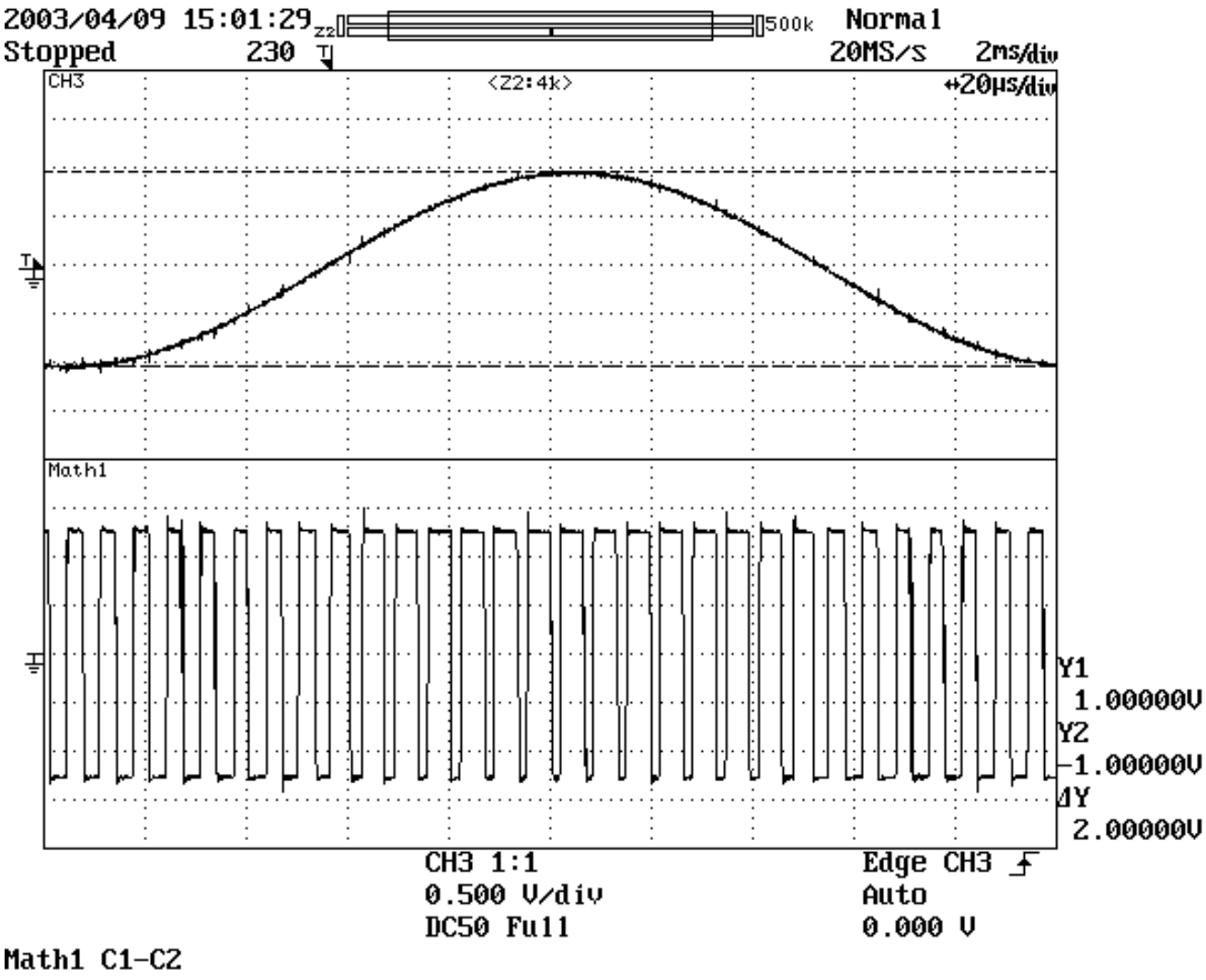

Figure 6.1 – PWM Test Waveform

6.3 Test 3 – PWM 50% Duty Cycle and Frequency

This is an important characterization test because it gives us an idea of how much distortion is introduced to our Class-D amplifier. With a grounded input signal, the PWM waveform should be 50% duty cycle at the appropriate frequency (150kHz). If the duty cycle is off, distortion will be added to our amplifier.

Equipment:

- (2) Agilent E3642A DC Power Supplies
- (1) Yokogawa Dl7100 Digital Oscilloscope

Procedure:

- Ground all inputs with no load attached at the output.
- Turn on power supplies (+/-2.5V).
- Measure the frequency and duty cycle of the PWM signal. It should be 150kHz and 50% duty cycle.

Results:

- This test passed but not perfectly. First we made sure that the PWM signal range is +/-5V. This is shown below in Figure 6.2. From the waveform, it is clear that the PWM signal range is +/-5V. There is also significant ringing, but this is expected because of the extremely high frequencies.

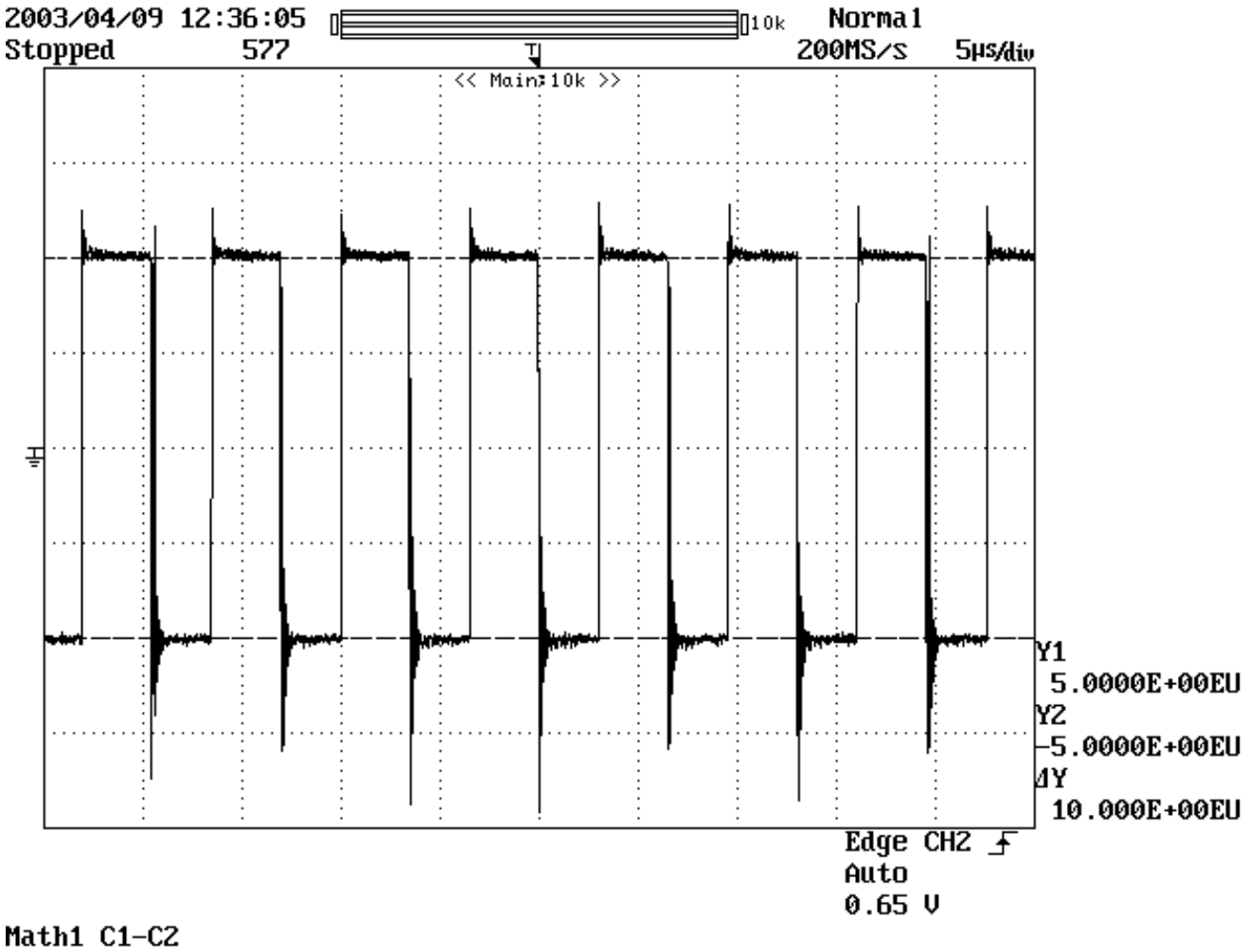

Figure 6.2 – PWM Voltage Range Test Waveform

Next we wish to determine the frequency of the PWM signal. This is shown below in Figure 6.3. From the figure, we see that the PWM frequency is 152.44kHz. This is extremely close to the 150kHz desired frequency. This difference will not affect our Class-D amplifier since any frequency that satisfies Nyquist's sampling criteria should be equally good.

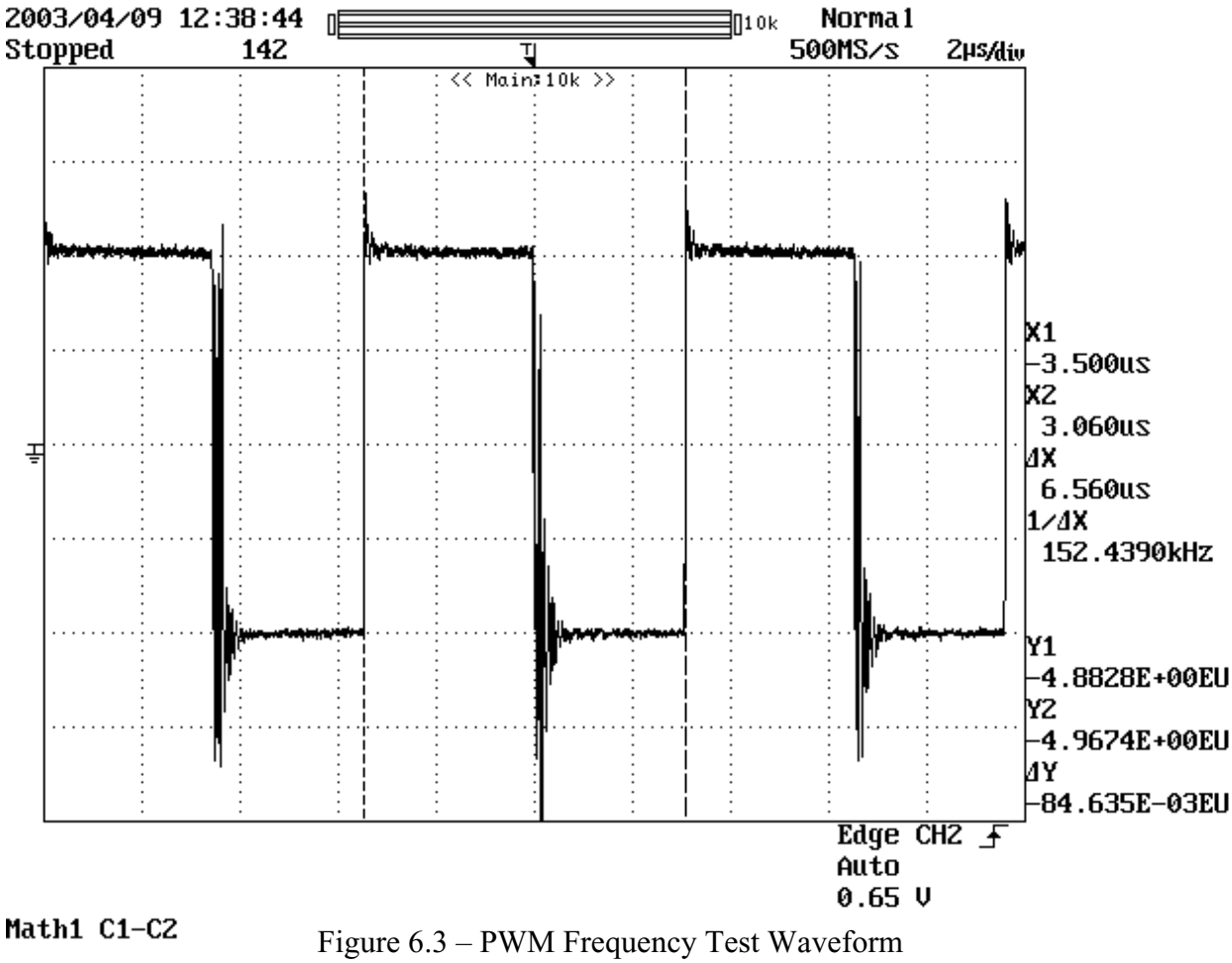

Figure 6.3 – PWM Frequency Test Waveform

Lastly, we wish to determine the duty cycle of the PWM waveform. This can be seen below in Figures Figure **6.4** and Figure **6.5**. From Figure 6.4 the time high is 3.43us, and from Figure 6.5 the time low is 3.06us. Therefore the duty cycle is:

$$\frac{T_H}{T_H - T_L} \quad \frac{3.43\,us}{3.43\,us \quad 3.06\,us} = 0.5285$$

Because the duty cycle is 52.85% there will be some slight distortion introduced to the amplifier. This should be minimal however because of the small difference in duty cycles (50% and 52.85%).

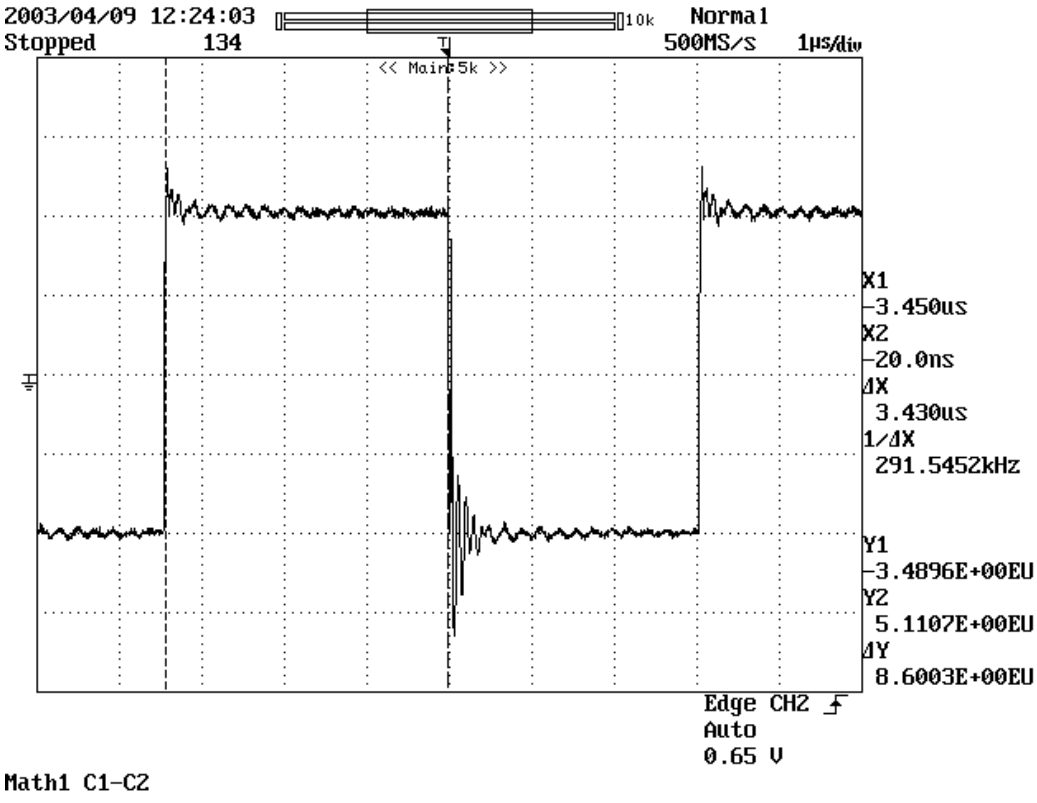

Figure 6.4 – PWM Time High Test Waveform

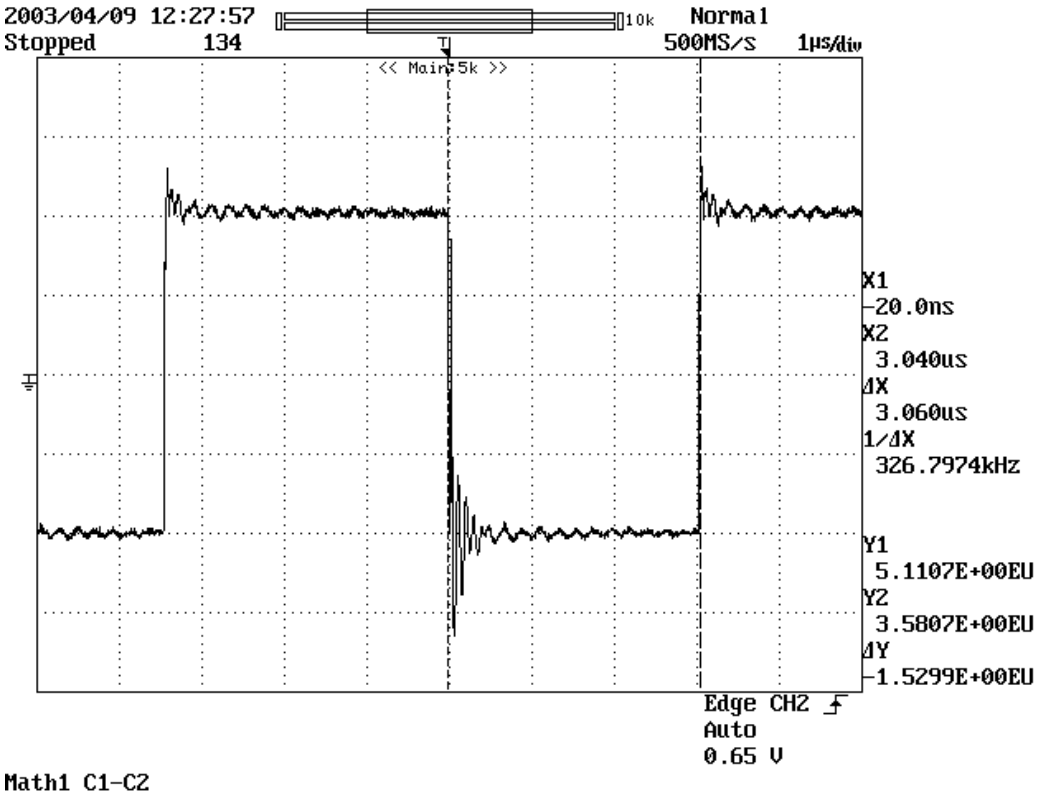

Figure 6.5 – PWM Time Low Test Waveform

6.4 Test 4 – Speaker Power Test

This is fairly simple characterization test, which measures the current delivered to the load when the Class-D amplifier is connected to an 8 ohm speaker.

Equipment:

- (2) Agilent E3642A DC Power Supplies
- (1) Agilent 33250A 80MHz Function Generator
- (1) 8 ohm speaker

Procedure:

- Wire all five digital volume control inputs to Vss to achieve a gain of 0 dB. Attach a 1kHz, 1Vpp sinusoidal input to the audio input pin. Attach an 8 ohm speaker to the output of the H-Bridge.
- Connect power supplies to +/-2.5V, observing how much current is drawn from the power supplies.
- If the current drawn is not excessive, compare to simulated values.
- If the current drawn is excessive, suspect problems in the fabricated chip with driving a load.

Results:

- This test passed. With a 1kHz, 1Vpp sinusoidal input and an 8 ohm speaker attached, we observed the current drawn by the speaker. This current was measured to be 128mA, which was lower than the 400mA for an 8 ohm load from simulation. This difference is caused by the fact that we are using an 8 ohm speaker which has inductive properties to reject high frequency components. Our simulations were based on a purely resistive load that accepts all frequencies. The 128mA is therefore acceptable.

6.5 Test 5 – Sound Test

This is the most important characterization test because we are actually producing sound which is what the amplifier is designed to do. From the output of the speaker, we will listen for distortion.

Equipment:

- (2) Agilent E3642A DC Power Supplies
- (1) Agilent 33250A 80MHz Function Generator
- (1) 8 ohm speaker

Procedure:

- Wire all five digital volume control inputs to Vss to achieve a gain of 0 dB. Attach a 1kHz, 1Vpp sinusoidal input to the audio input pin. Attach an 8 ohm speaker to the output of the H-Bridge.
- Connect power supplies to +/-2.5V.
- Listen and determine if it sounds like 1kHz and if there is any audible distortion.

Results:

- This test passed but not perfectly. With a 1kHz, 1Vpp sinusoidal input and an 8 ohm speaker attached, we listened to the sound generated by the speaker. Again we observed that the current drawn from the power supplies was 128mA. We also determined that there was 60mV of offset in the PWM waveform which creates slight distortion.
- Interestingly, when we changed the input to a square wave or pulse, there was less distortion. In fact, the speaker sounded very good with no audible distortion when driven by a square wave. This may be caused by a non-linearity in the triangle wave. If the triangle wave is non-linear and noisy, the PWM signal may be incorrect because the sinusoidal wave rises and falls slowly. But if a square wave is used, with sharp rise and fall times, the non-linearity and noise on the triangle wave shouldn't affect the PWM signal. It

would therefore be extremely beneficial if we could look at the triangle wave, but unfortunately we didn't have room to create a pin for this signal.

Chapter 7
Summary and Conclusions

7.1 Comparison of Simulated and Experimental Results

Our Class-D audio amplifier passed all tests that we performed on it. Simulated and experimental results also matched. The only difference that was found was the slight distortion introduced to the amplifier. This was most likely caused by a non-linear triangle waveform. Some improvements that would benefit the amplifier are noted below.

7.2 Future Improvements

After fabricating our chip, we found out that there was no size limitation. This would have greatly benefited us as we weren't able to output some of our signals that we would have wanted to (e.g. triangle waveform, pre-amplified signal). It would also have been beneficial to enhance this project by making it stereo. To do this, we would put the H-Bridge Delays and H-Bridges on a separate chip. This would allow us to completely separate the power supplies which we had hoped we could do.

The triangle wave generator can be improved by using a different design. An initial design that produced an extremely clean triangle waveform had to be replaced because of size limitations. The design we used however, appears to be non-linear and sensitive to noise. Therefore, a better design should be investigated.

The comparator in the design can be improved by adding (cascading) more gain and preamp stages. This would improve the sensitivity and reduce delay in the comparator.

A cross-coupled NOR gate can also be added to the H-Bridge driver to obtain symmetry between the falling-edge delays and the rising-edge delays. Since the driver in

this design only has cross-coupled NAND gates, the rising-edge delays are longer due to the stacked PMOS transistors (versus the parallel NMOS transistors).

7.3 Estimate of Time Spent on Project

Table 7.1 lists the estimated time spent on our Class-D Audio Amplifier.

Table 7.1 – Estimate of Time Spent on Project

	Estimated Time (in hours)	
Task	**Jason**	**Abbas**
Circuit Design	90	100
Class Time	45	45
Layout	80	75
DRC	5	5
LVS	10	10
Top-Level Simulation	10	15
Extracted Simulation	10	10
Documentation	60	25
Total	**310**	**285**

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[4] S. E. Turner and W. H. Slade, "Class-D Audio Amplifier Front-End Circuit," 18 April 2003 <http://www.eece.maine.edu/vlsi/Class_D/classd_paper.pdf>.

Biography of the Authors

Jason Cookson grew up in Glenburn, Maine and attended John Bapst Memorial High School. He will graduate from the University of Maine in May 2003 with a B.S. degree in Electrical Engineering and a minor in Mathematics and Statistics. After graduation, he plans to work at M.I.T. Lincoln Laboratory in the Missile Defense Elements Group. Jason is a member of Eta Kappa Nu, Tau Beta Pi, and Pi Mu Epsilon.

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Abbas Hameer was born in Nakuru, Kenya, on August 9th of 1980. He completed his O-level education in 1996 at Al-Muntazir in Dar-es-Salaam, Tanzania. After completing a year of his A-levels, he came to the US in 1998 to pursue his bachelor's degree. In December of 2002 he graduated with a BS in Computer Engineering, from the University of Maine. He has worked as a Physics tutor, and a teacher's assistant for Sequential logic systems and Electronics I & II. He has also completed co-operative (co-op) work at Tundra Semiconductor Corporation in Portland, ME, and GE Power Systems, in Bangor, ME. He is currently waiting to begin work for his M.S. degree in the fall of 2003.

abbas.hameer@umit.maine.edu

Appendix A
Schematics

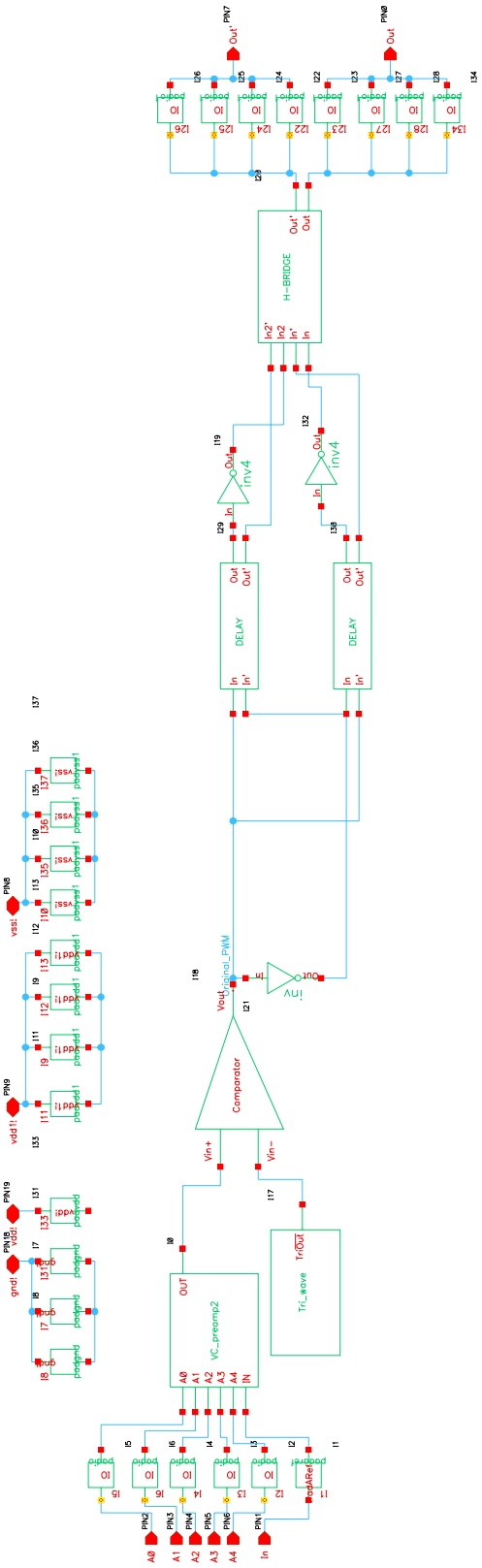


Figure A.1 – Top Level Schematic

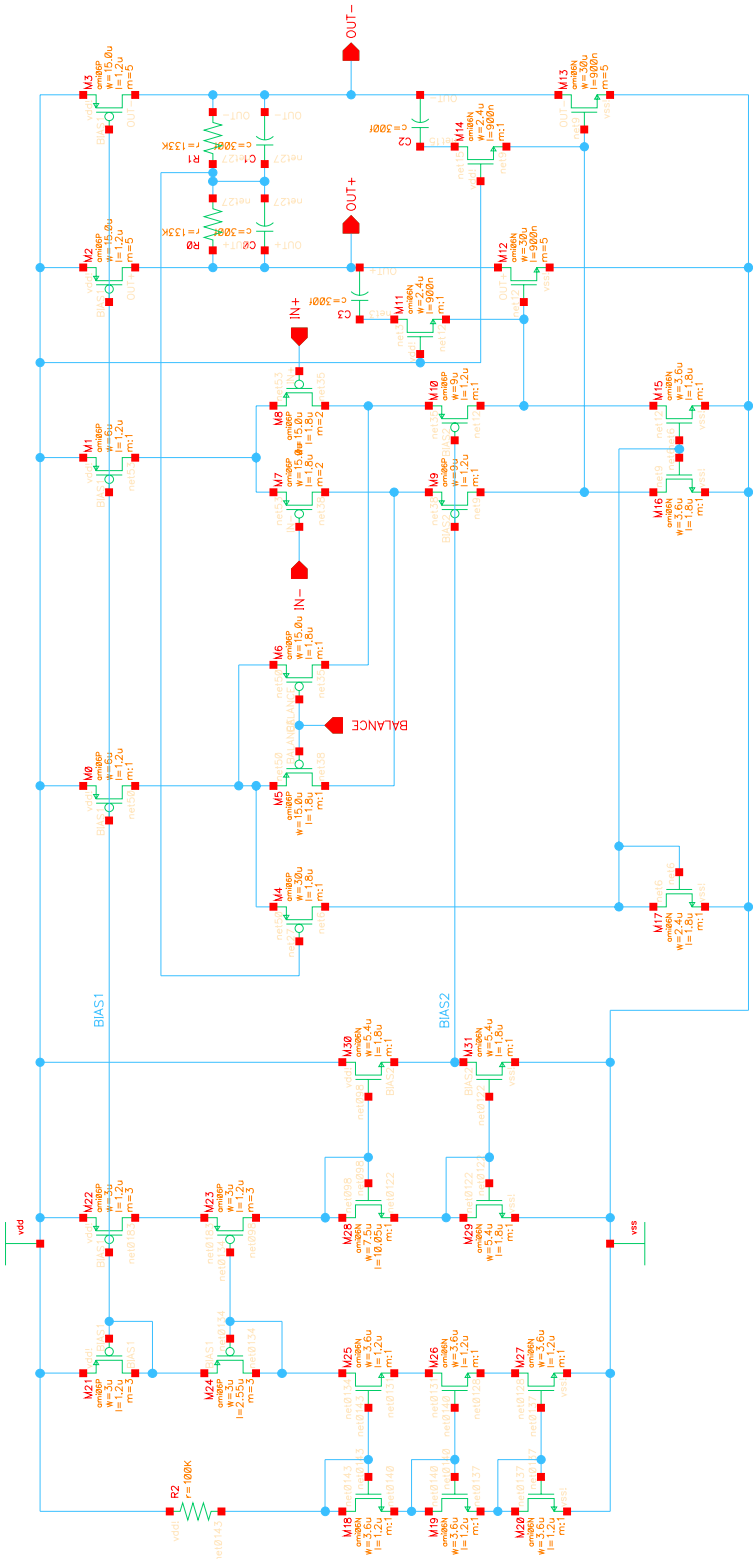


Figure A.2 – Two Stage Differential Op-amp Schematic

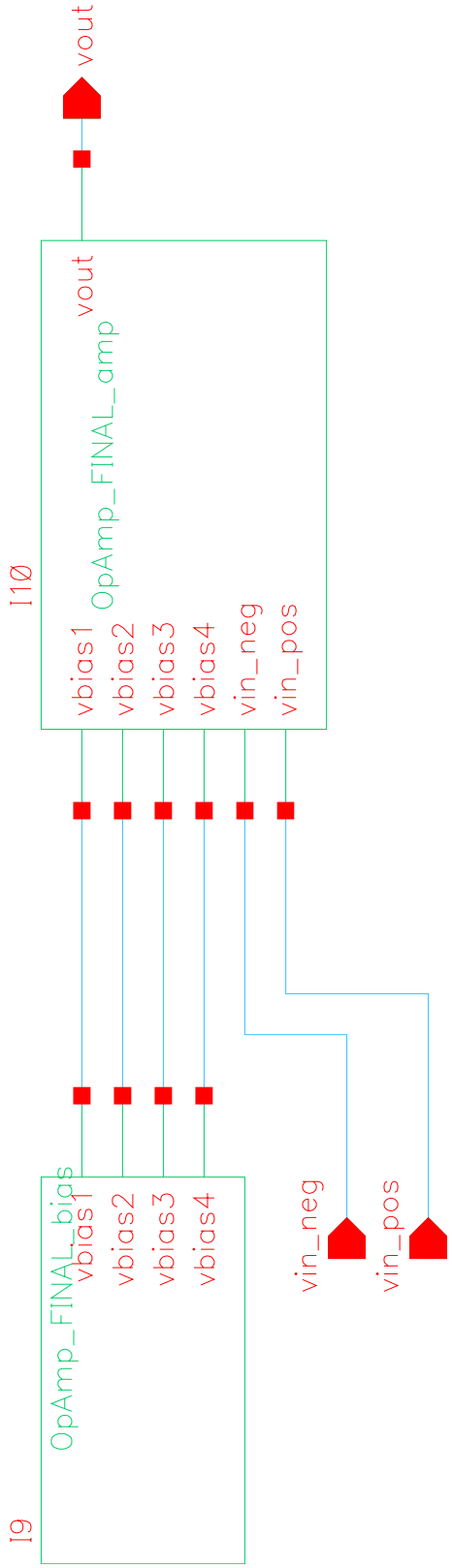


Figure A.3 – Wide Swing Op-Amp Schematic

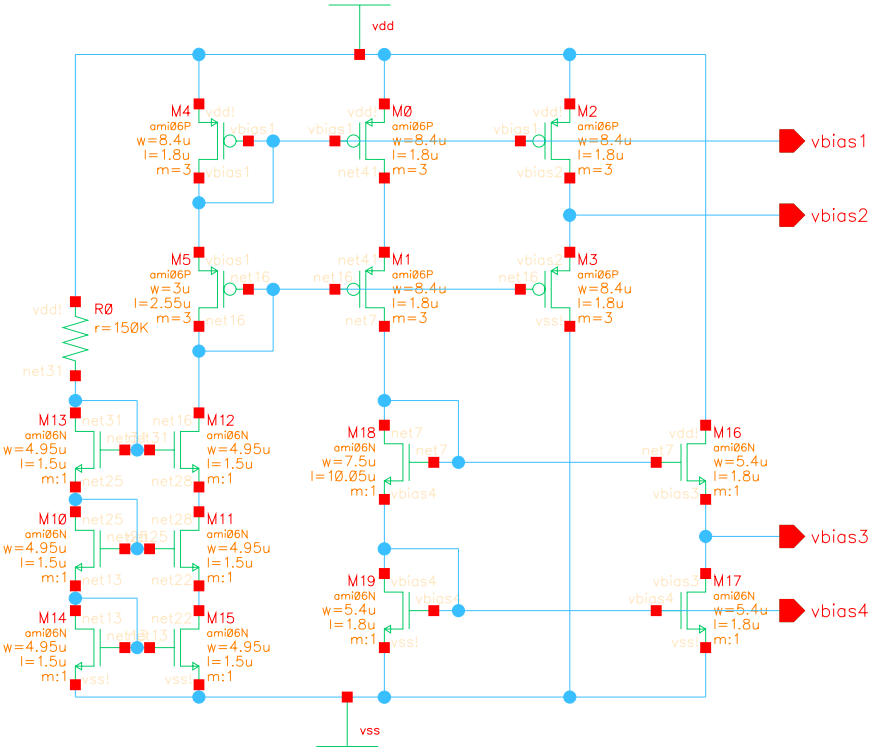


Figure A.4 – Wide Swing Op-Amp Bias Stage Schematic

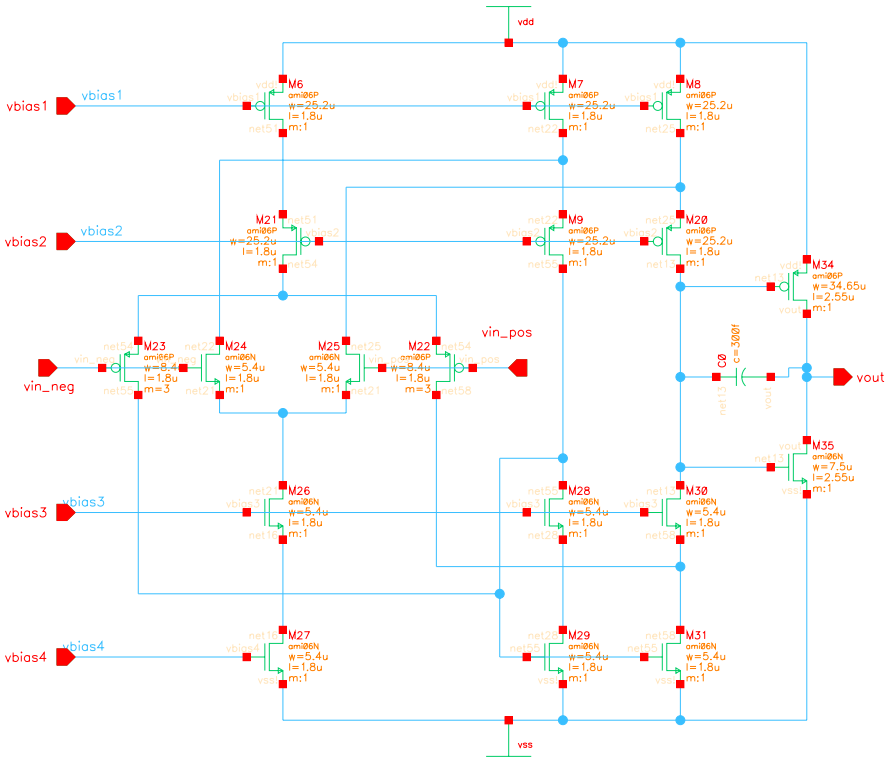


Figure A.5 – Wide Swing Op-Amp Gain Stage Schematic

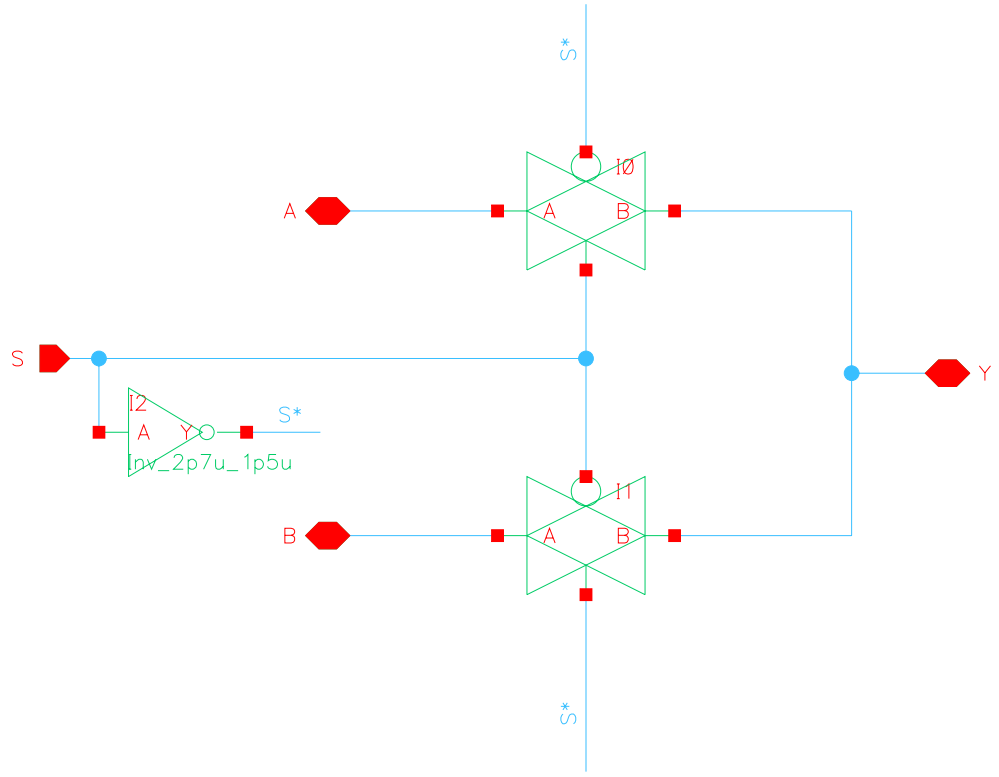


Figure A.6 – 2 to 1 Multiplexer Schematic

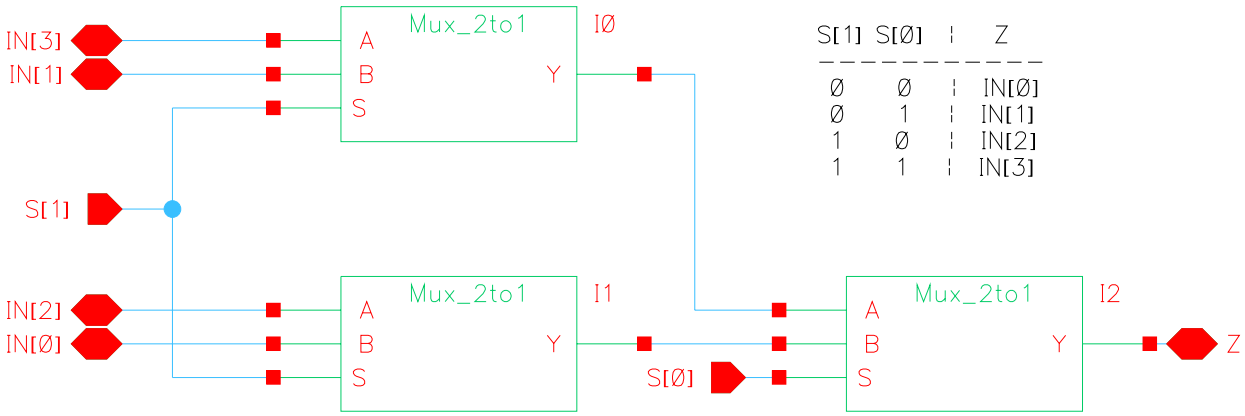


Figure A.7 – 4 to 1 Multiplexer Schematic

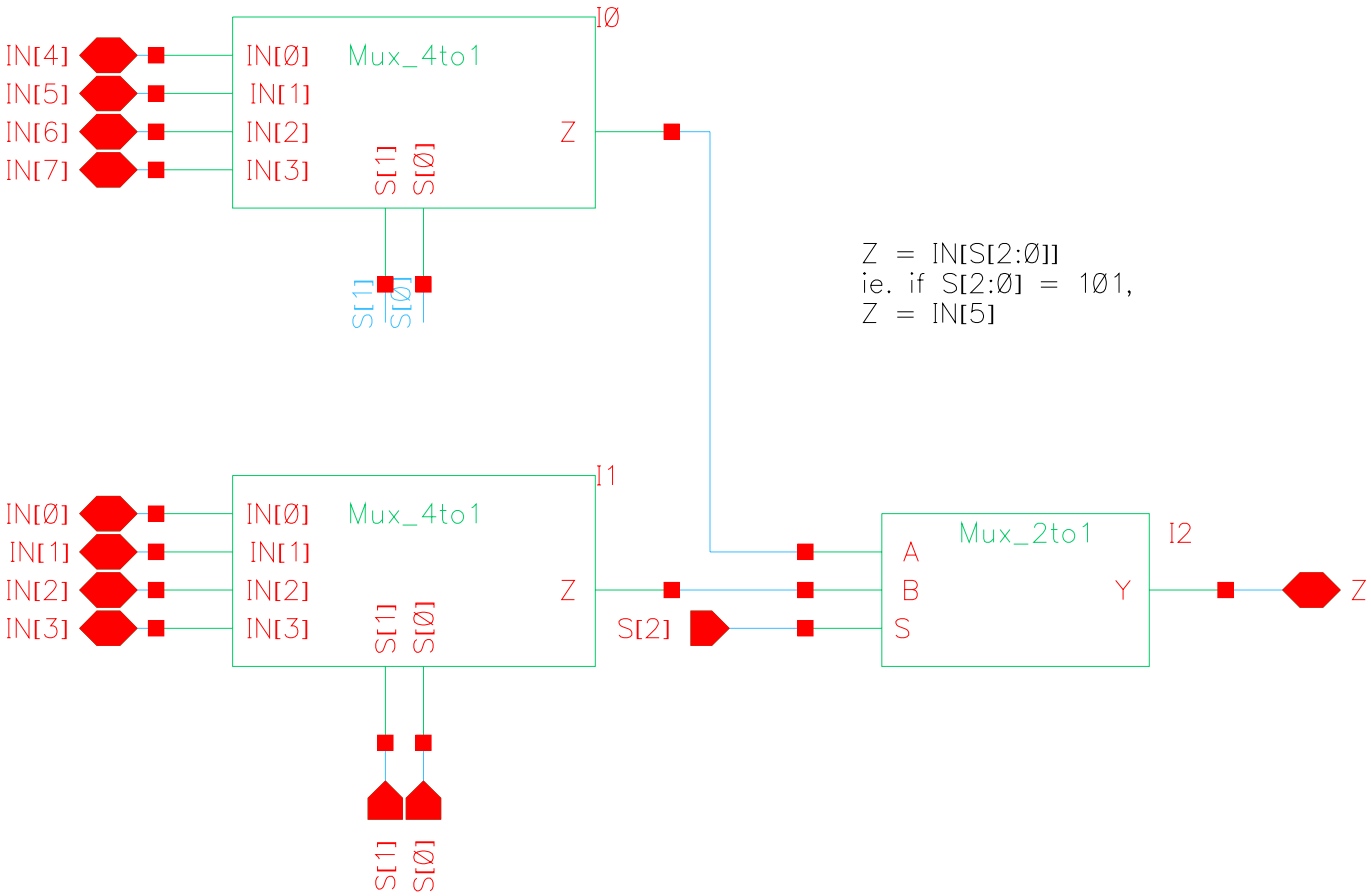


Figure A.8 – 8 to 1 Multiplexer Schematic

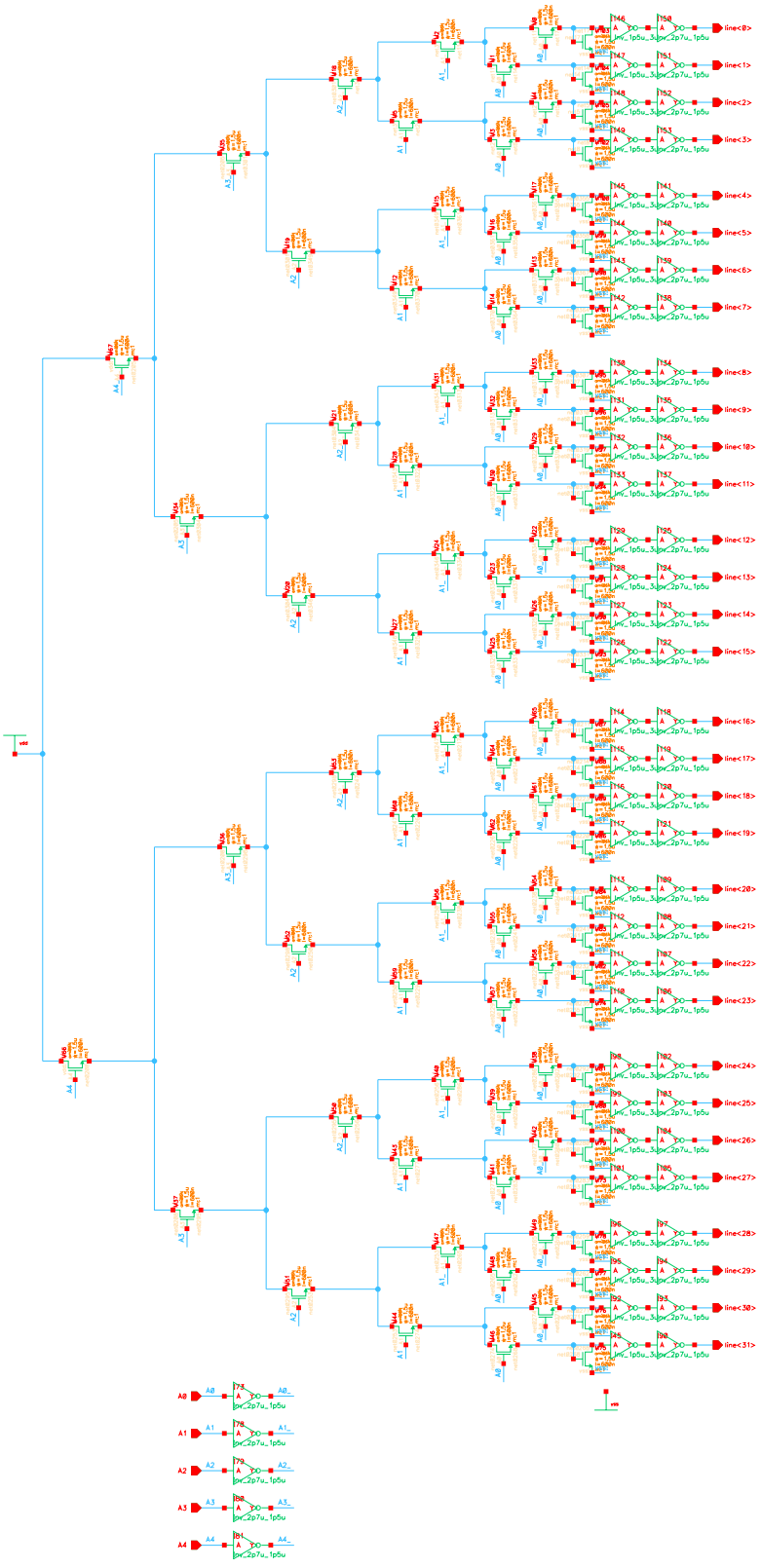


Figure A.9 – Line Driver Schematic

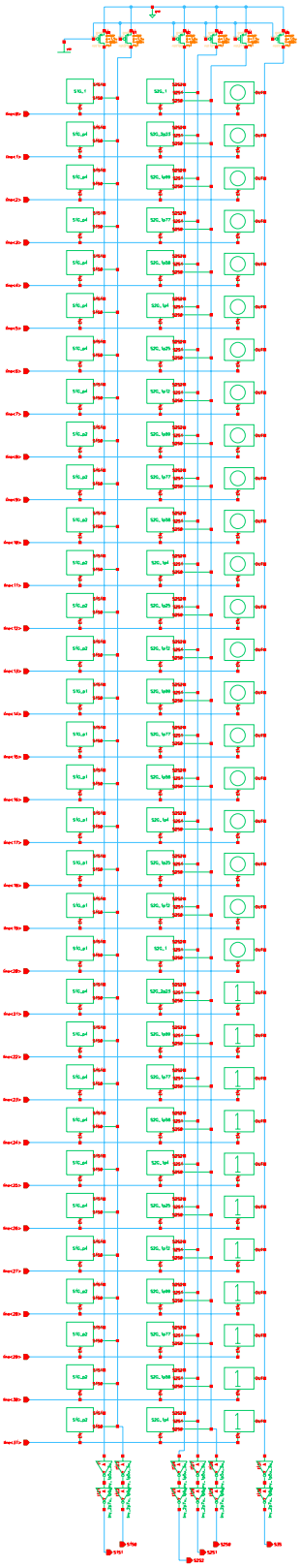


Figure A.10 – Volume Control ROM Schematic

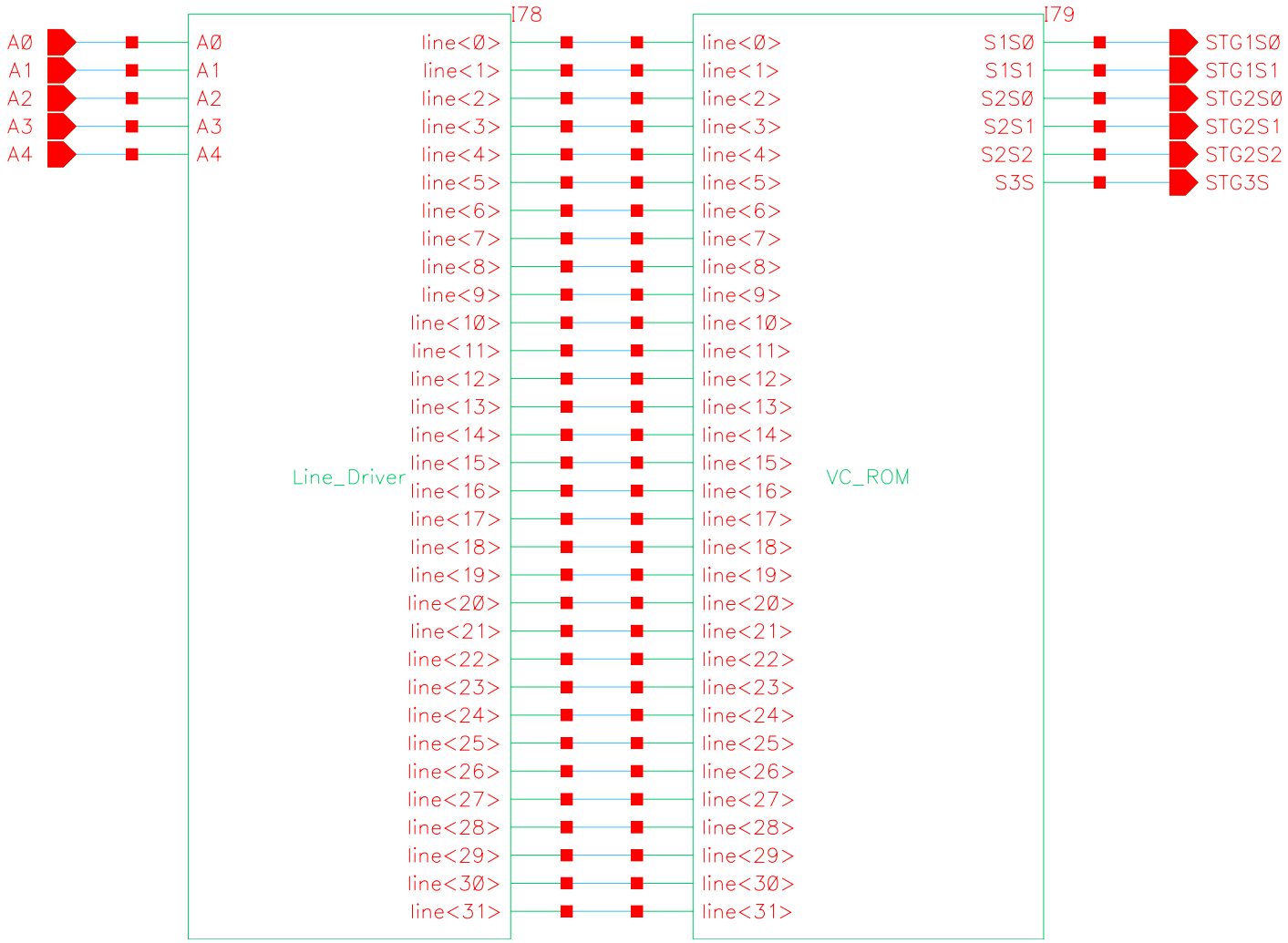


Figure A.11 – Volume Control Schematic

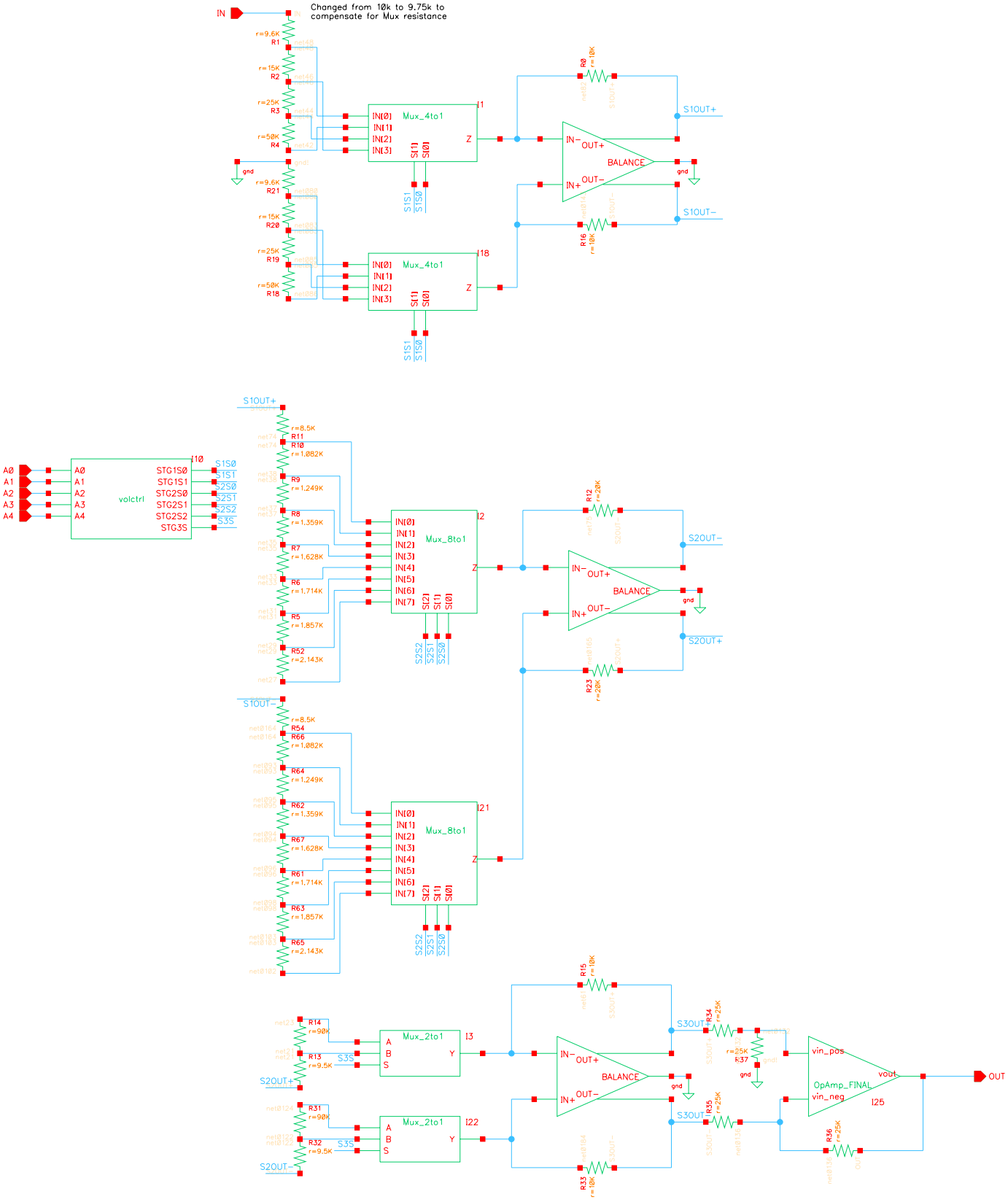


Figure A.12 – Volume Control Preamp Schematic

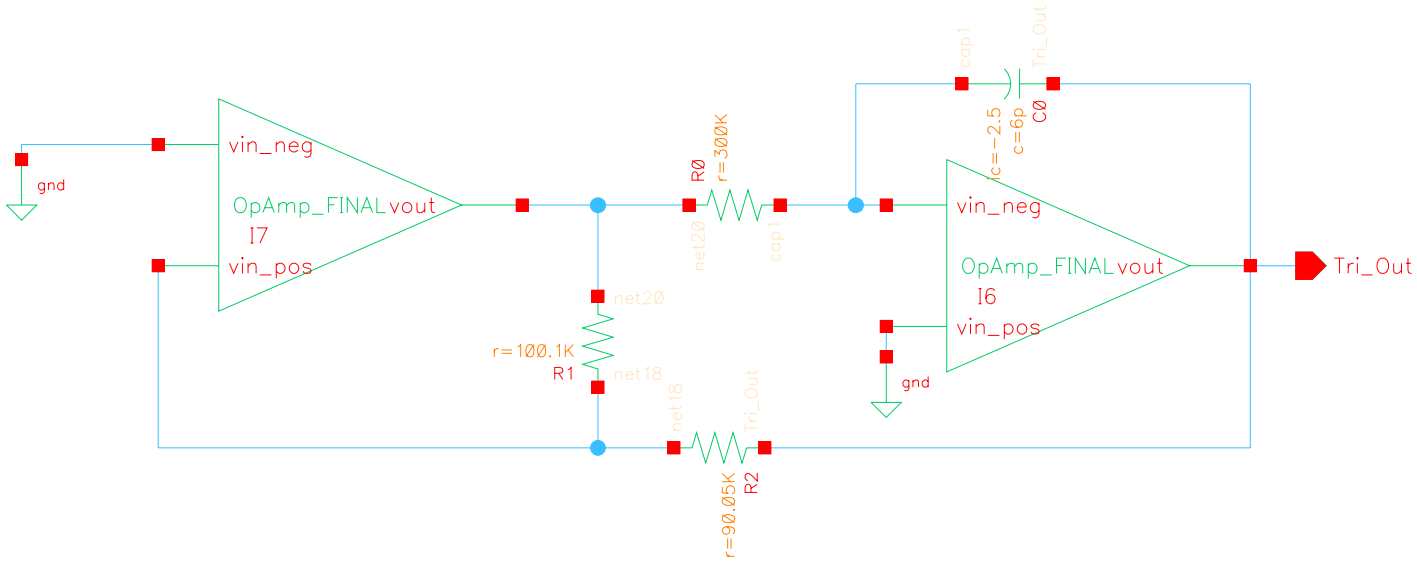


Figure A.13 –Triangle Wave Generator Schematic

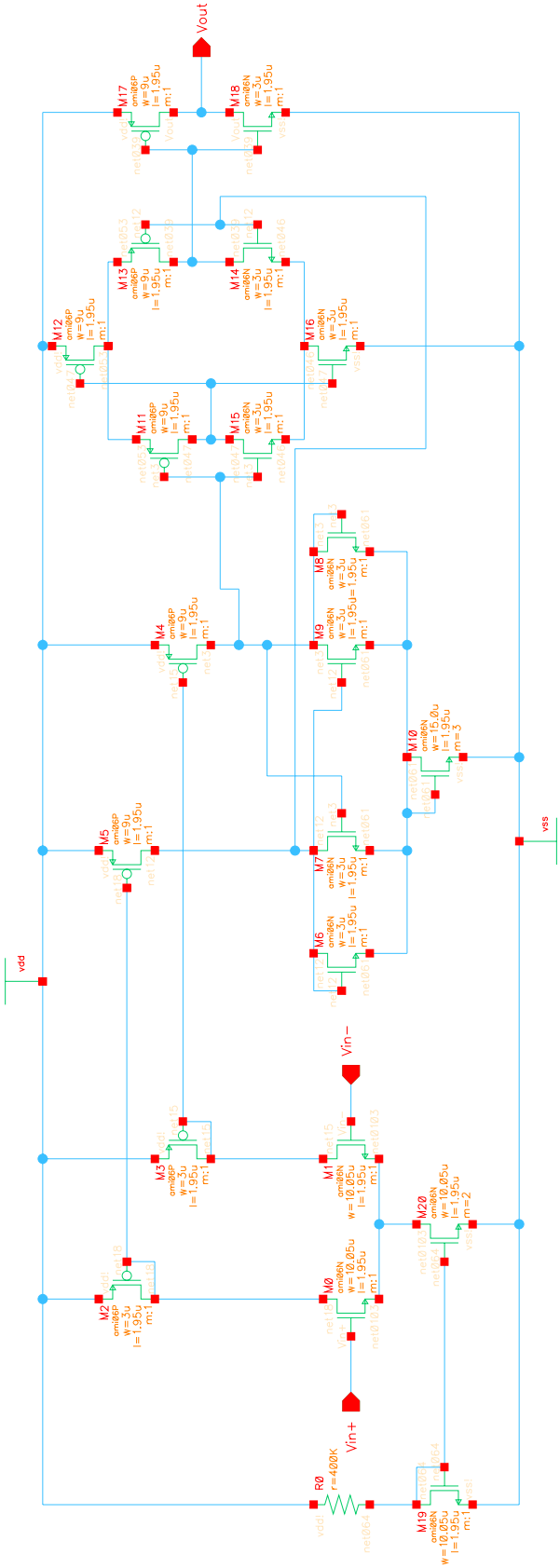


Figure A.14 – Comparator Schematic

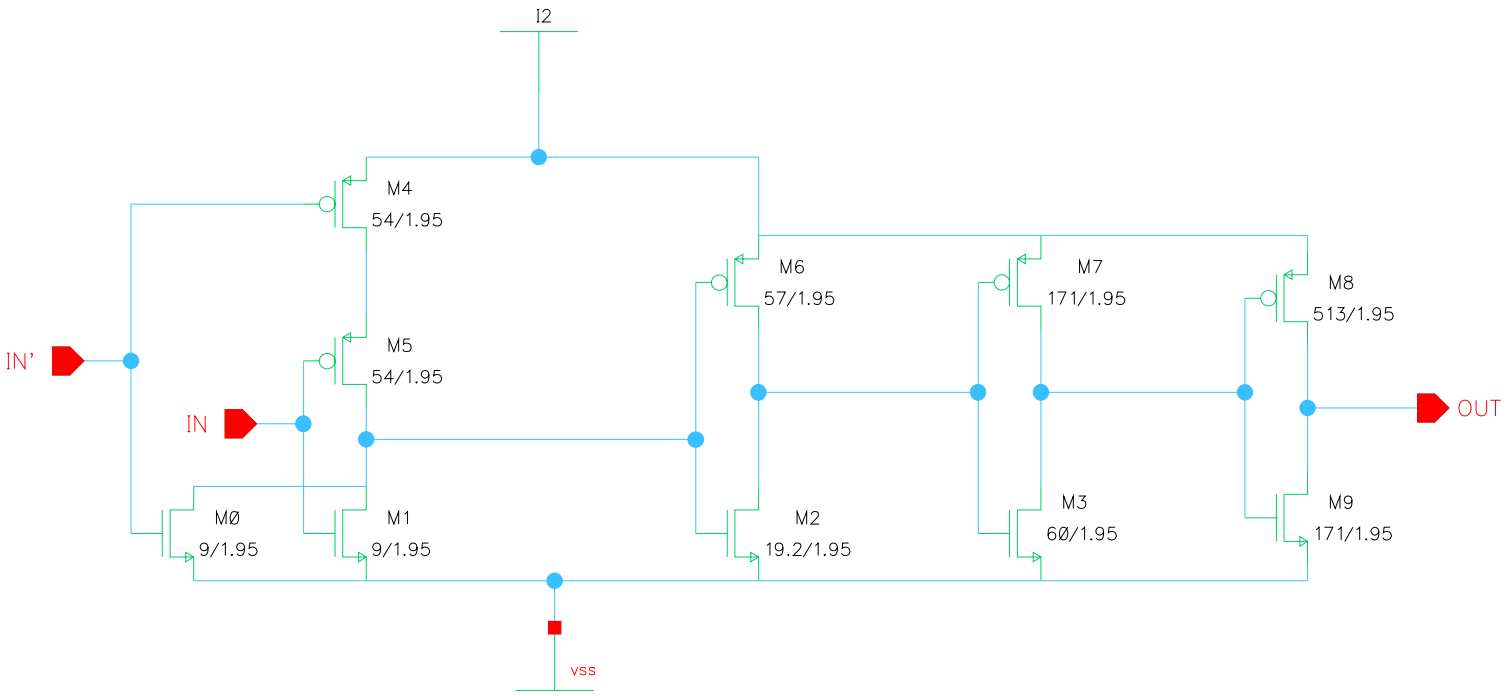


Figure A.15 – H-Bridge Delay Schematic

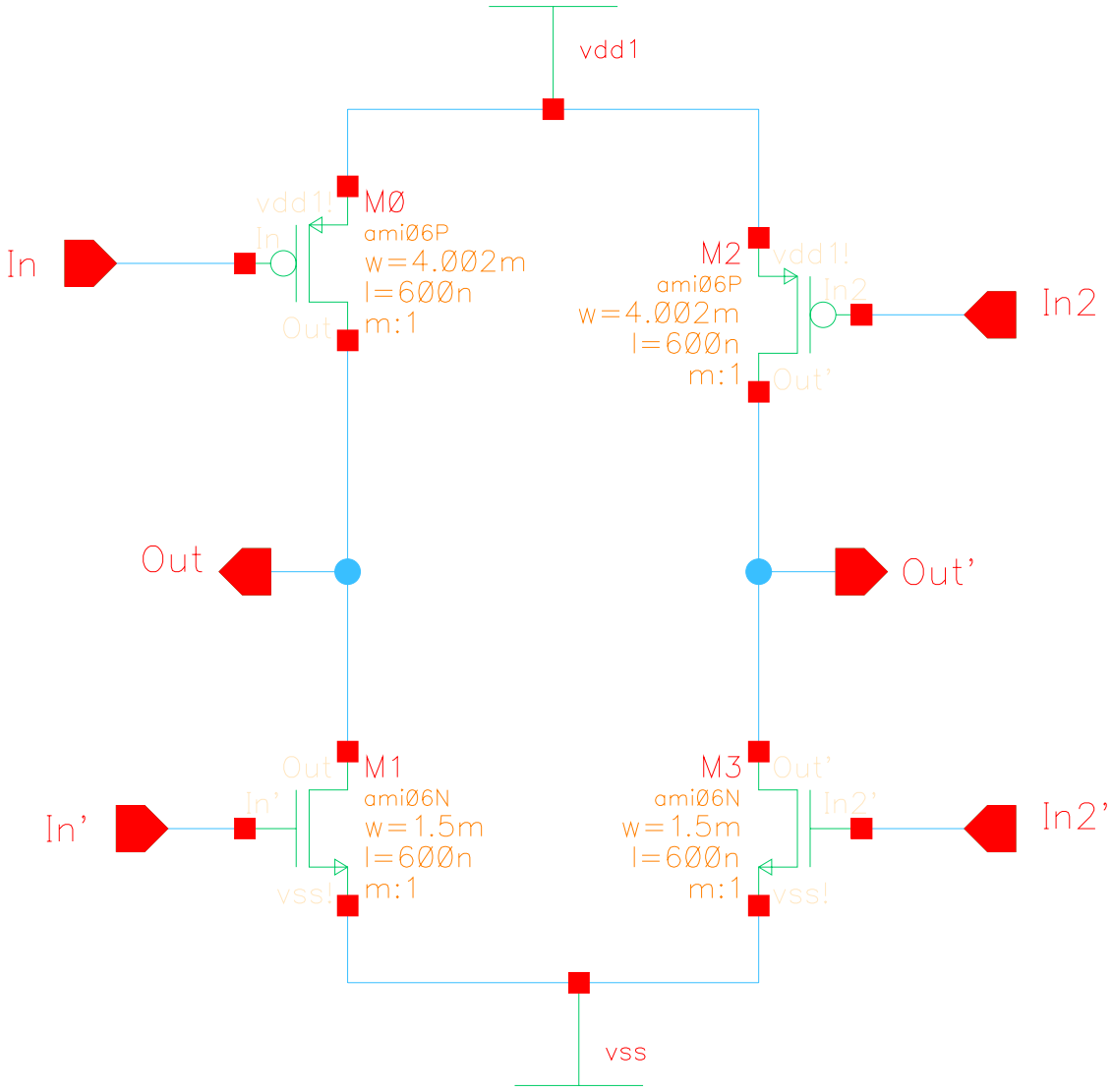


Figure A.16 – H-Bridge Schematic

Appendix B
Layout

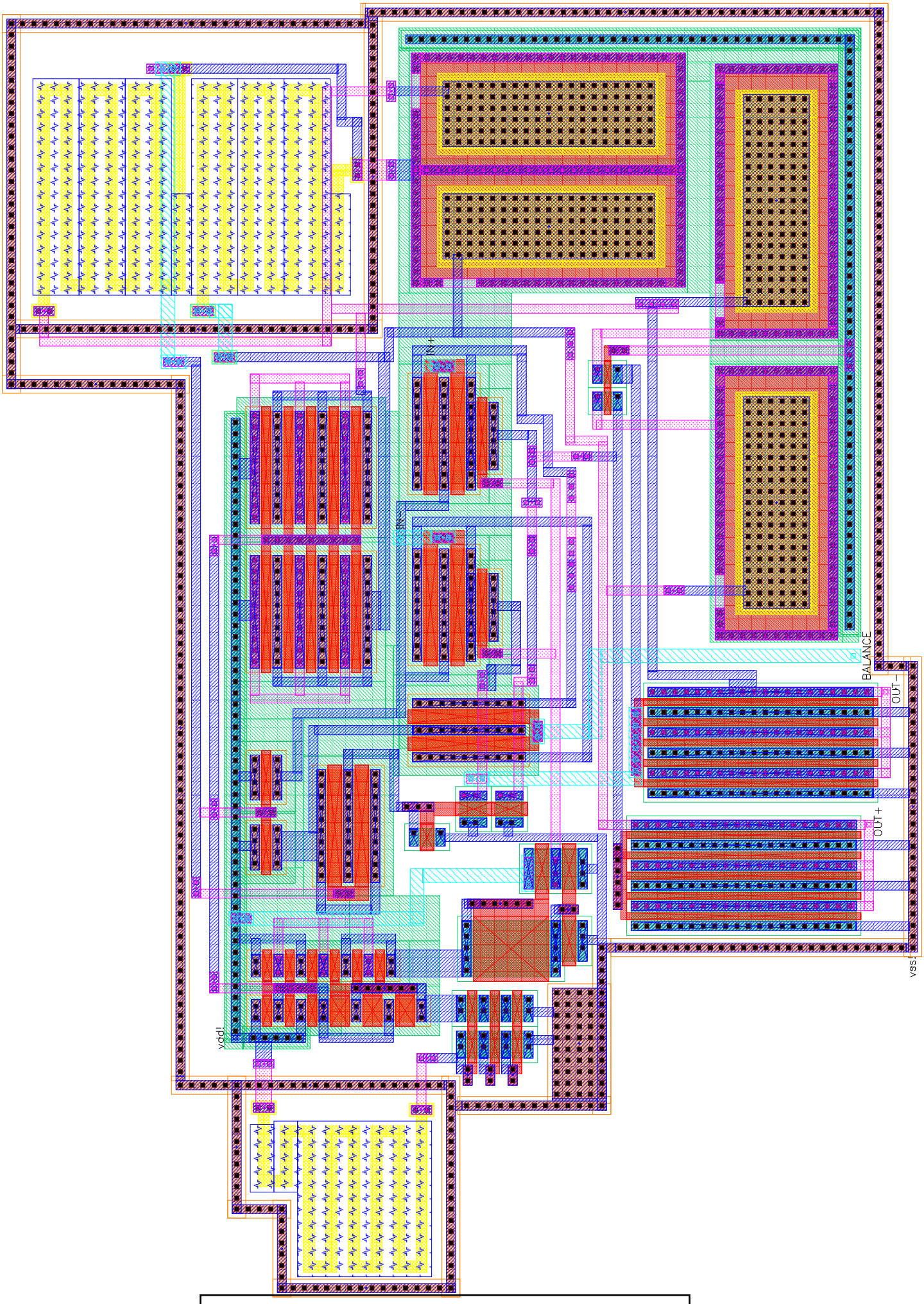


Figure B.1 -- Two Stage Differential Op-amp Layout

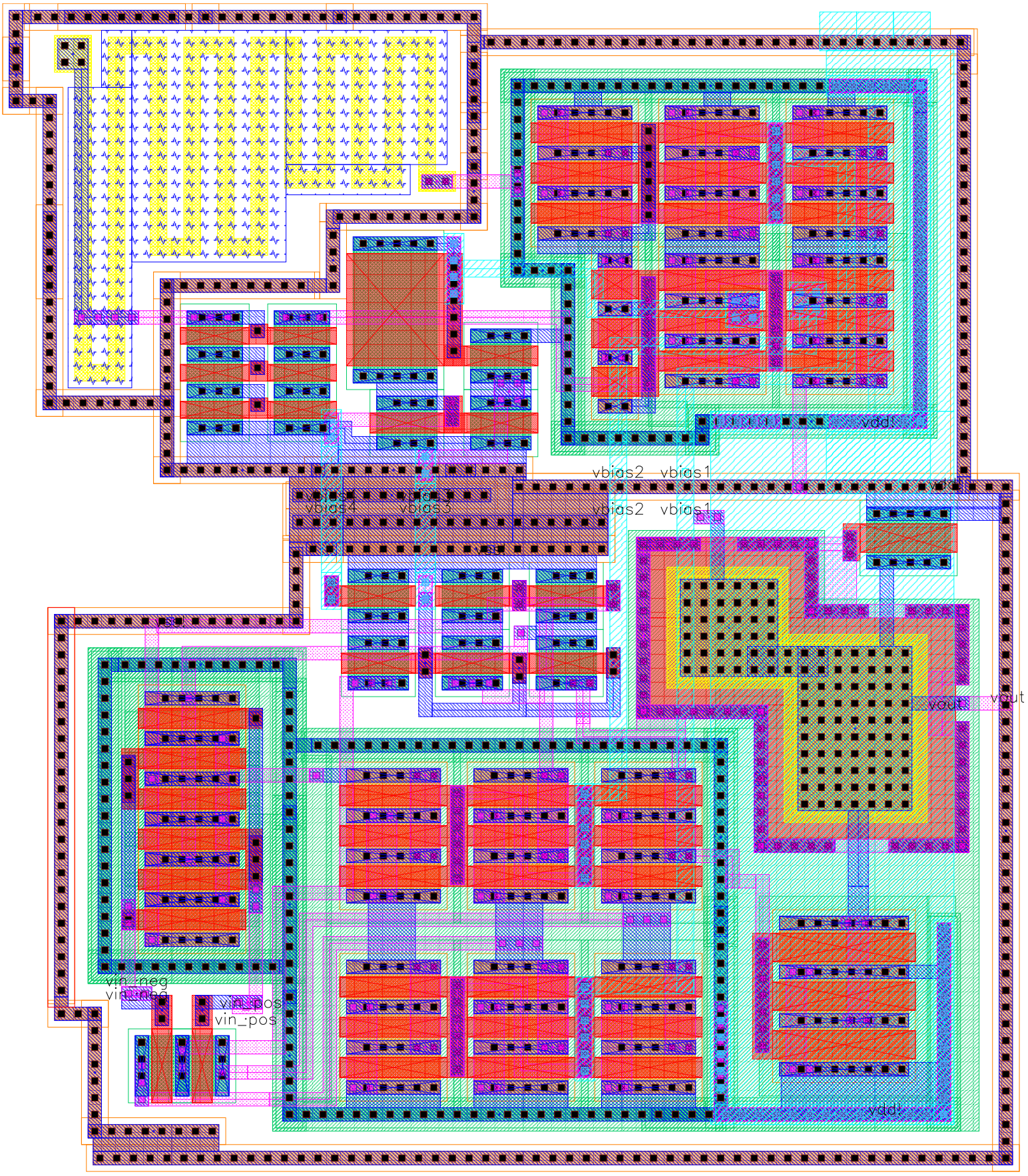


Figure B.2 -- Wide Swing Single Ended Op-amp Layout

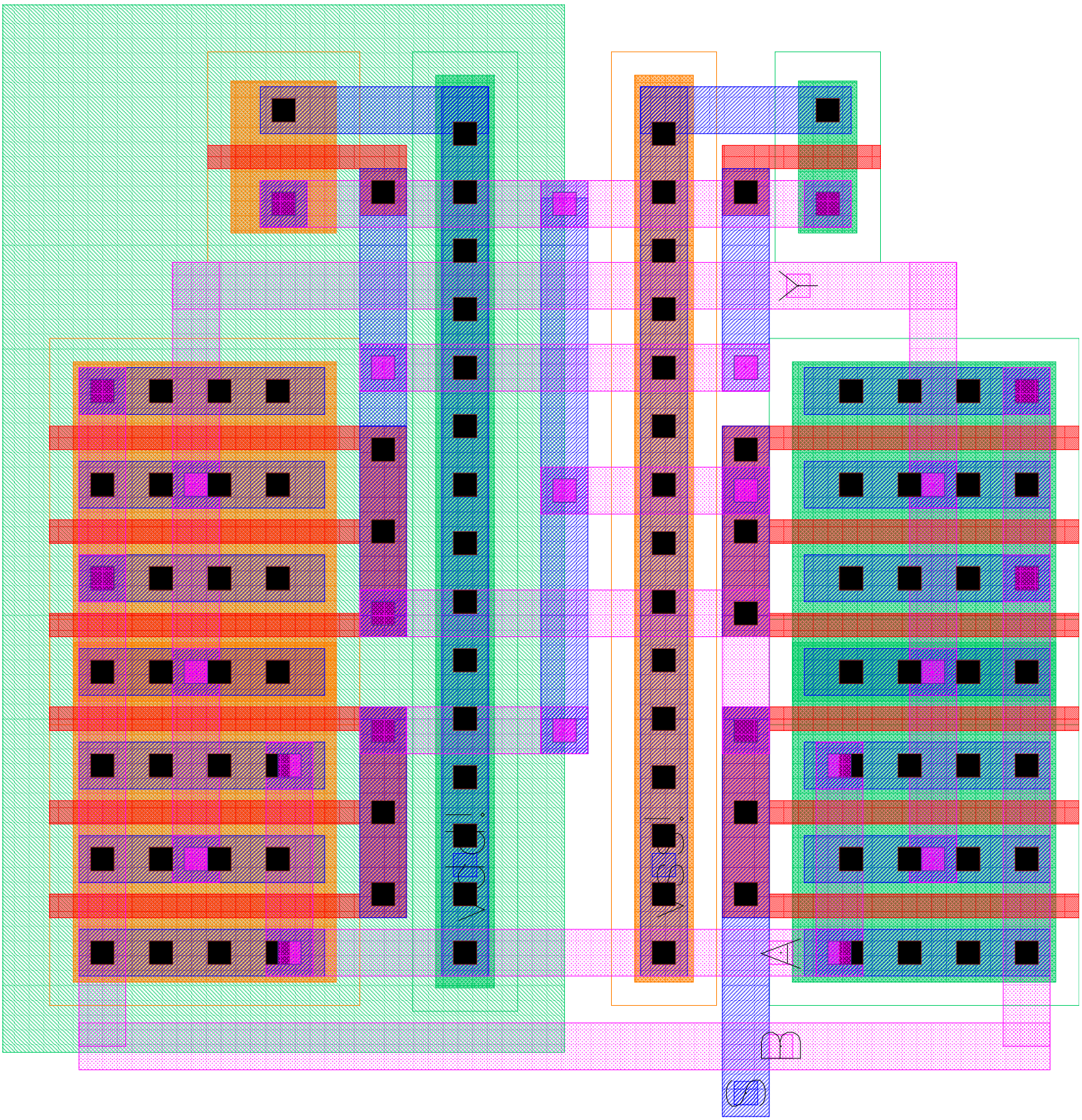


Figure B.3 -- 2 to 1 Multiplexer Layout

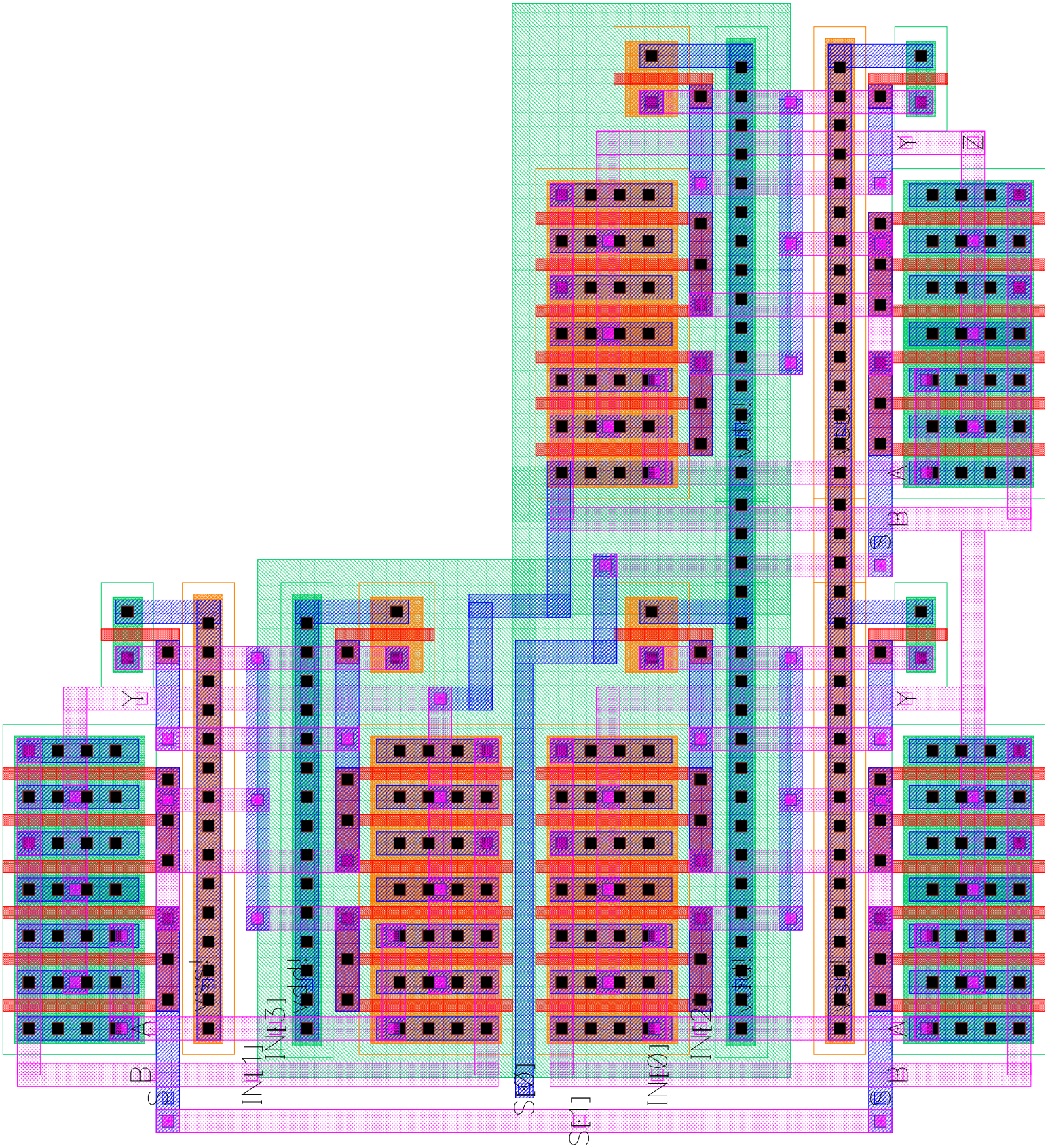


Figure B.4 -- 4 to 1 Multiplexer Layout

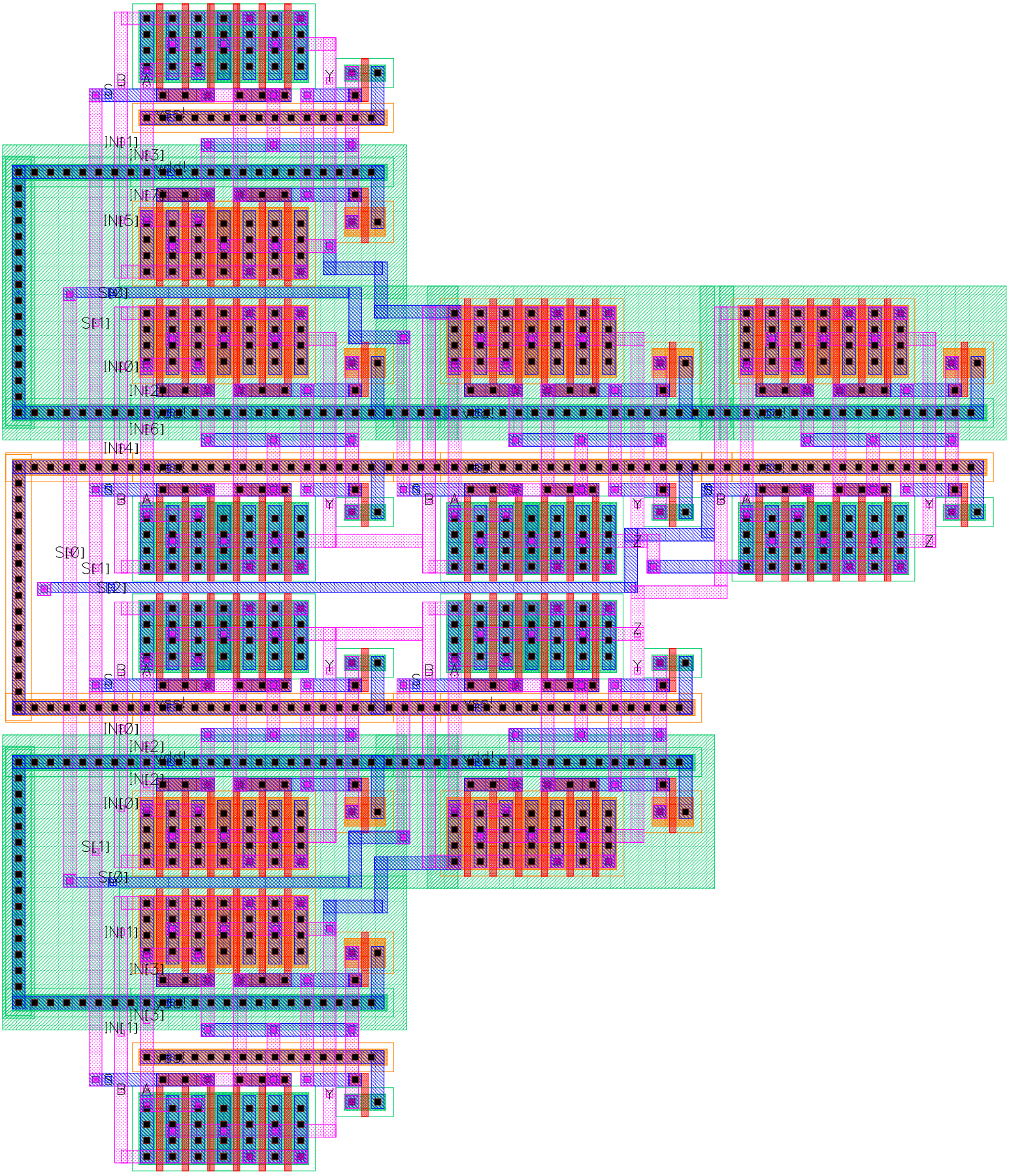


Figure B.5 -- 8 to 1 Multiplexer Layout

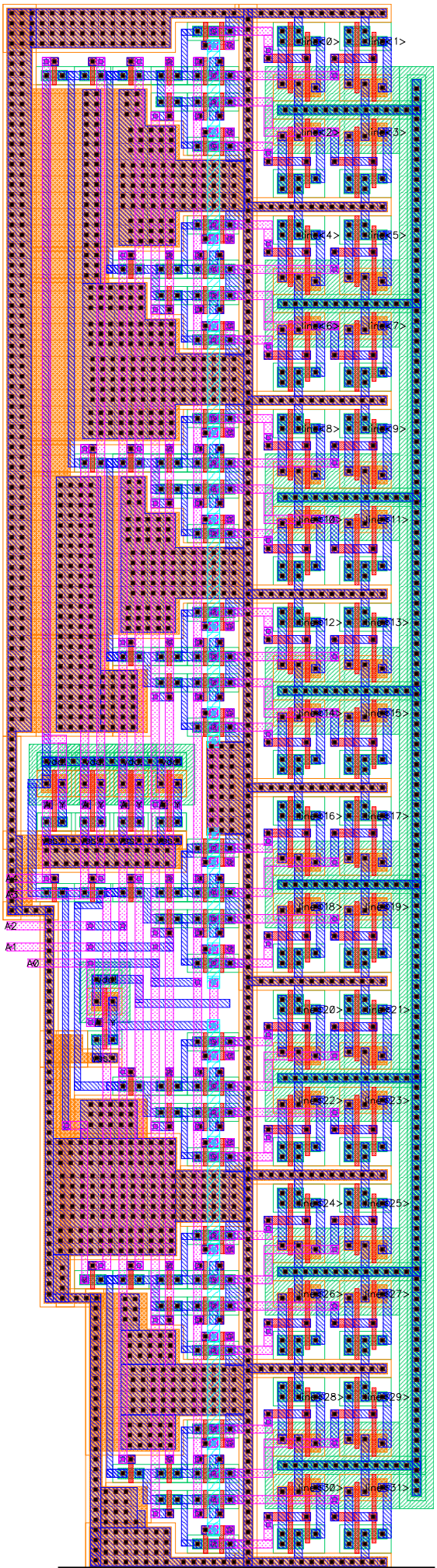


Figure B.6 -- Line Driver Layout

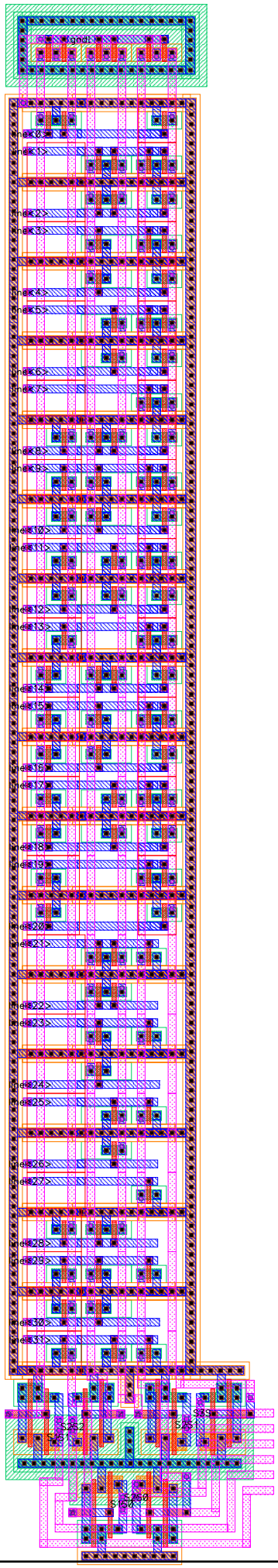


Figure B.7 -- Volume Control ROM Layout

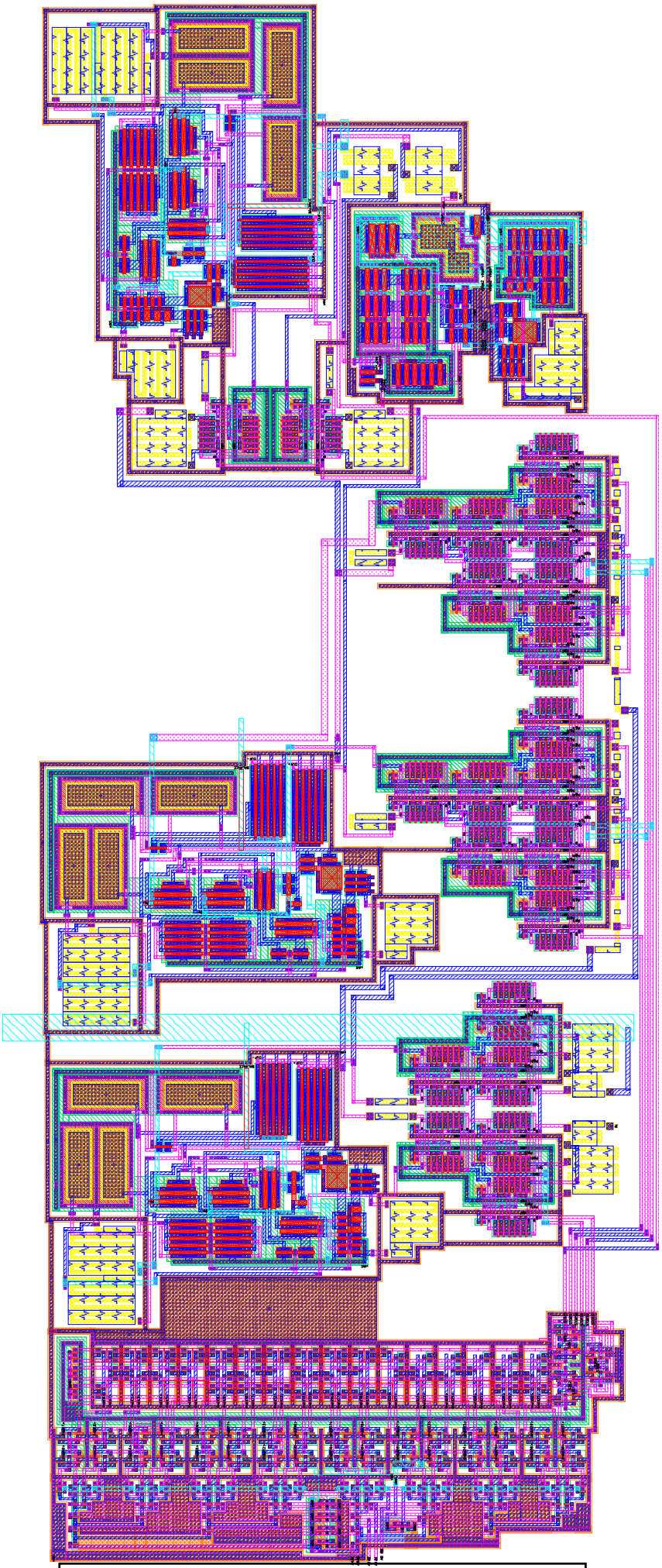


Figure B.8 -- Volume Control Preamp Layout

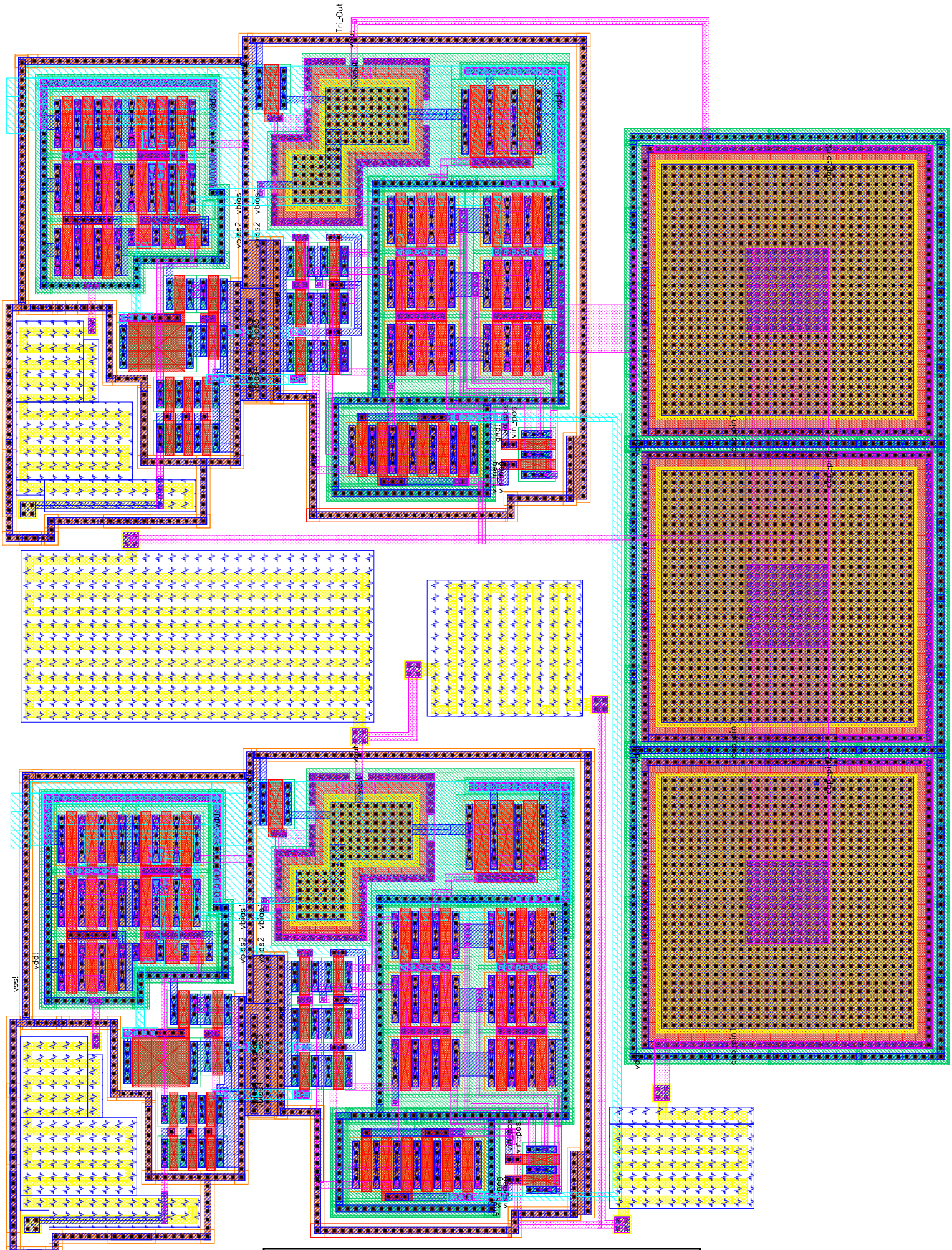


Figure B.9 -- Triangle Wave Generator Layout

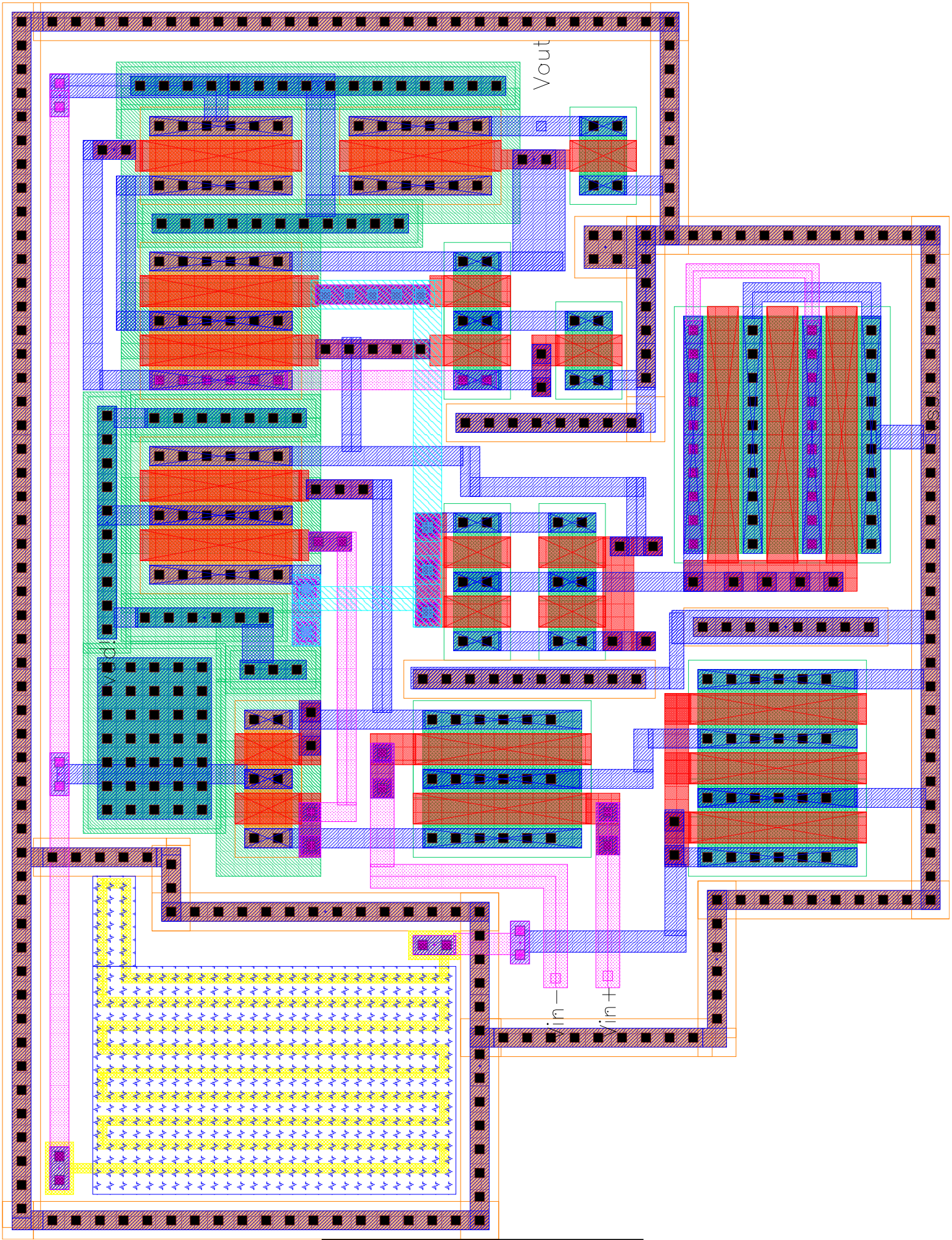


Figure B.10 -- Comparator Layout

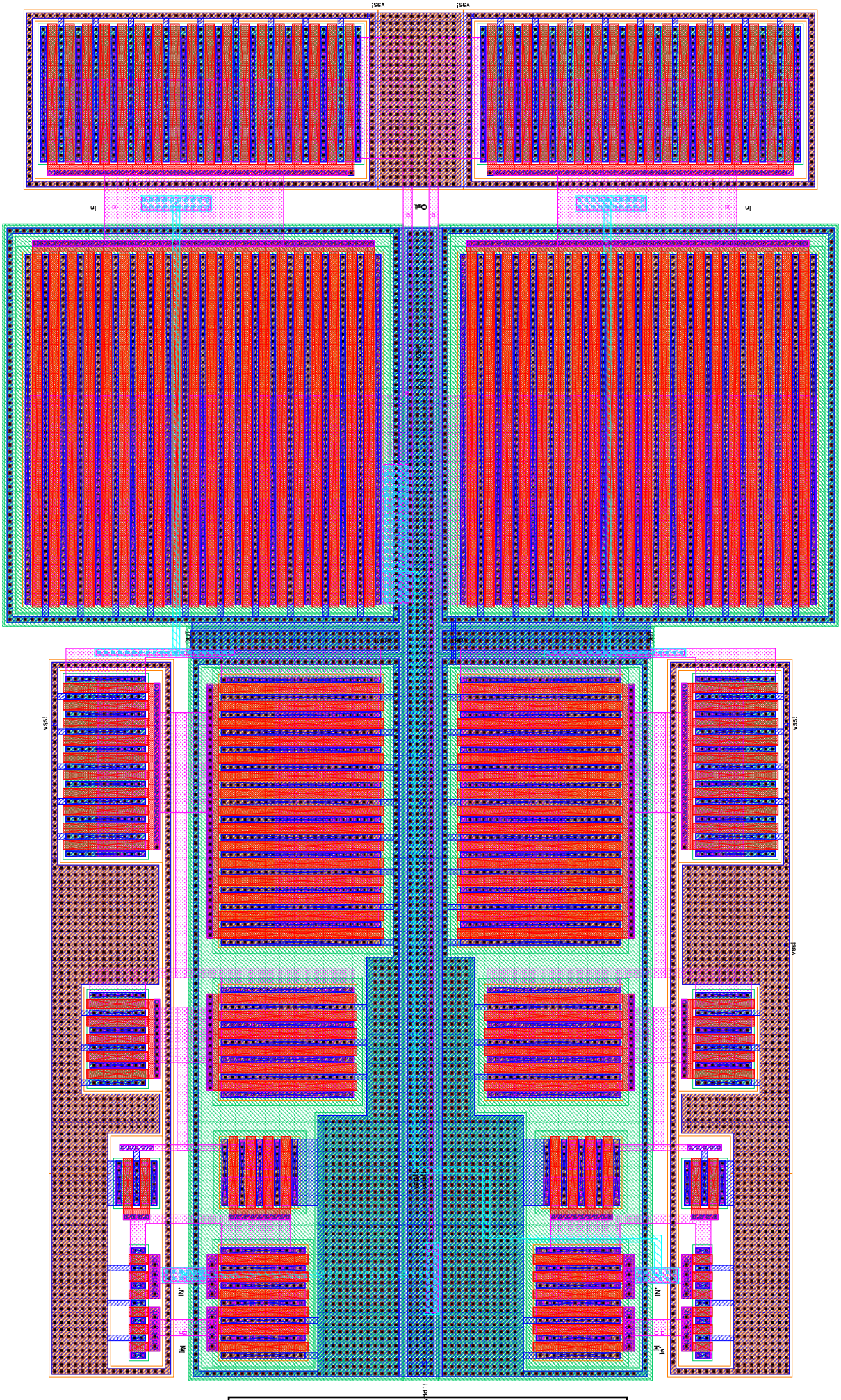
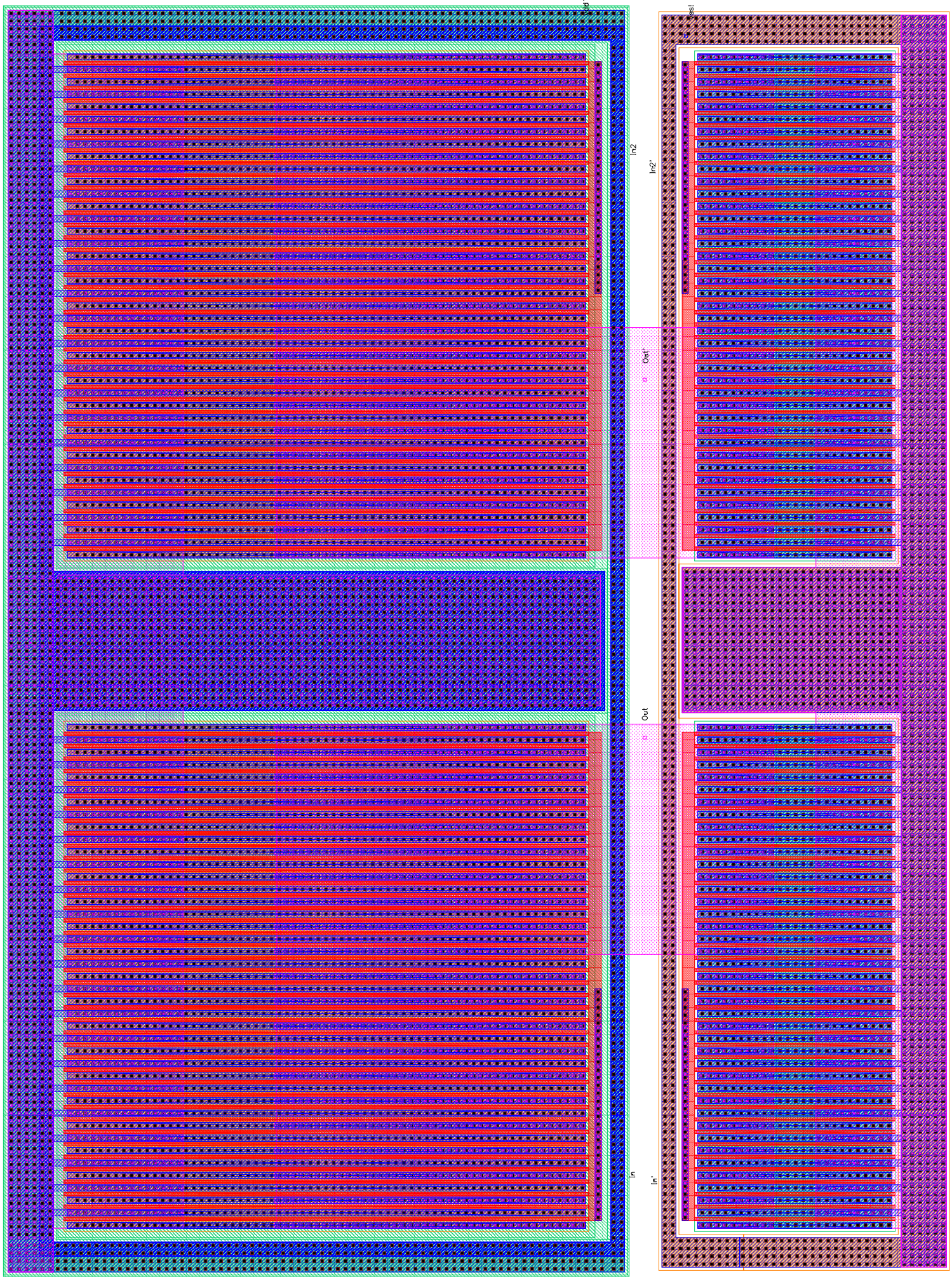


Figure B.11 -- H-Bridge Delay Layout


Vdd!
Vss!
In2
In2'
Out'
Out
In
In'

Appendix C
Entire Chip Layout

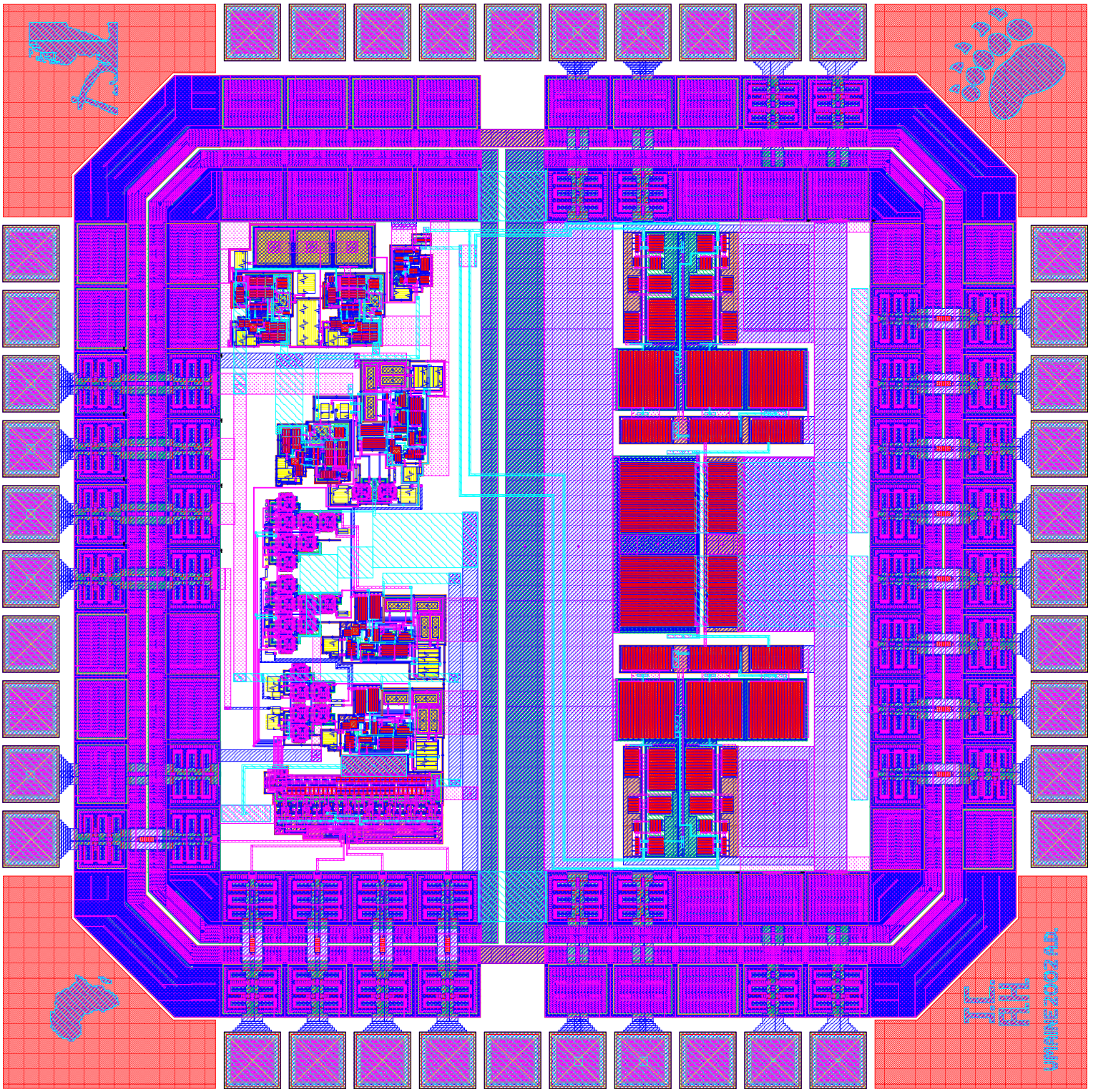


Figure C.1 -- Entire Chip Layout

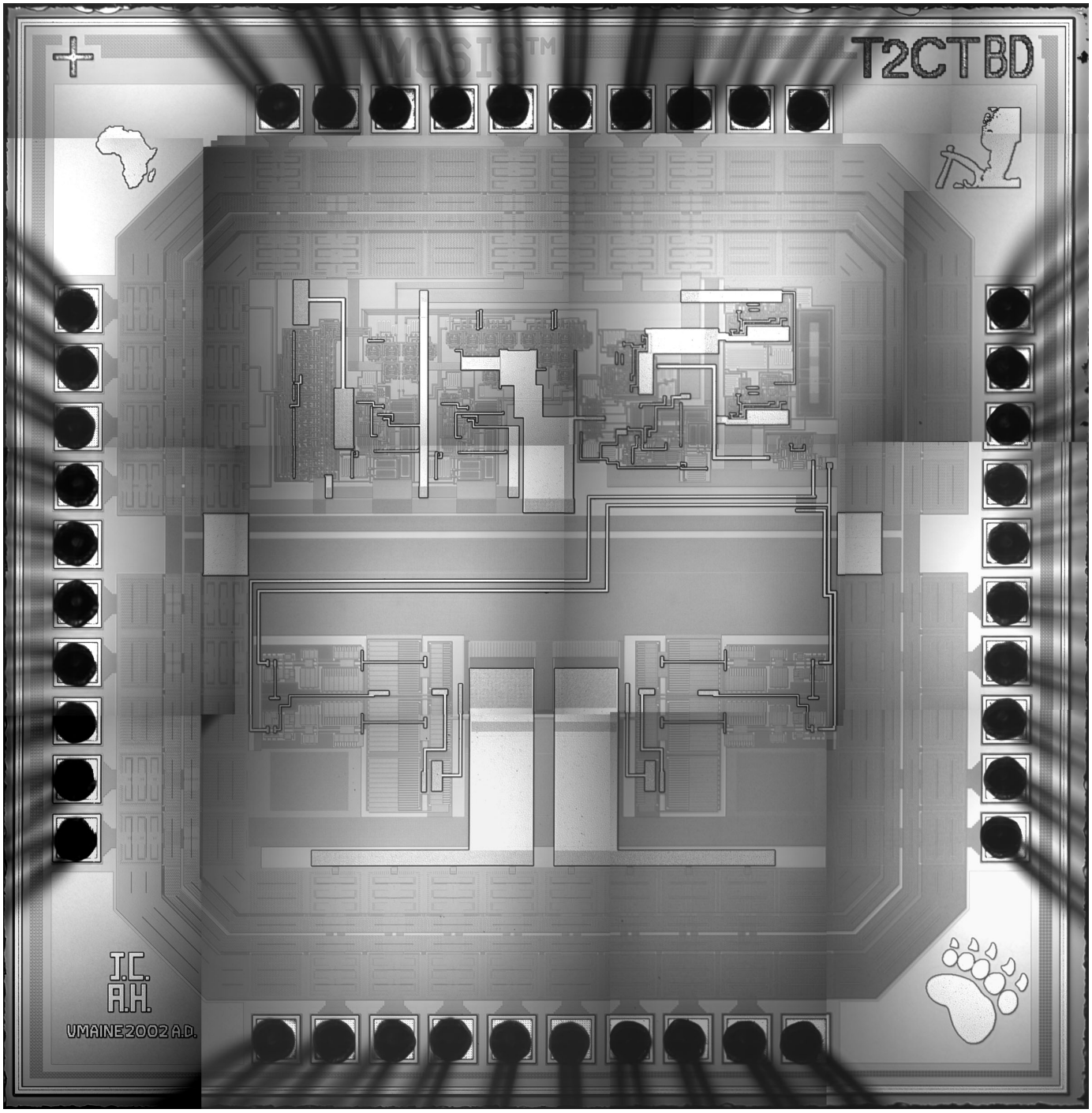


Figure C.2 – Microphotograph Collage